DESIGN AND VERIFICATION OF LOW POWER AND HIGH SPEED CARRY SELECT ADDER USING VERILOG

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Abstract—There is a vast usage of binary addition in digital circuits as it is the basic arithmetic operation and it became indispensable in most of the digital systems counting ALU, microprocessors and DSP. Adders are the fundamental building blocks in digital integrated circuit based designs. Ripple Carry Adder (RCA) gives the most solid design but takes more computation time. The time crucial applications employ Carry Look-ahead scheme (CLA) is used to derive fast results but they lead to increase in area. Carry Select Adder is a concession between RCA and CLA in terms of area and delay. This paper shows a great vision on the design analysis of carry select adder based on Multiplexer using Verilog. The delay (9.069ns), power (20.98mW) is minimized and total coverage is 100%. The proposed architecture of carry select adder is simulated and verified in ModelSim10.1e, synthesized in Xilinx ISE14.7, and power analyzed in Quartus II9.1.

Keywords—Carry select adder, Verilog, Power, delay, Modelsim10.1e, Xilinx ISE14.7, QuartusII9.1, Fulladder, Carry ripple adder, multiplexer.

I. Introduction

Devices like digital computers, processors, microprocessors often use arithmetic operations. Among those arithmetic operations addition is most commonly used. Also it serves as a edifice block for synthesis all other arithmetic operations. In digital adders, the speed of the adders is limited to propagate a carry through the adder. In elementary adder the sum of each bit position is generated sequentially only after the previous bit position has been summed and carry is propagated to next adder. The major speed limitation in any adder is in the production of carries. The carry select adder is used in many computational systems to overcome the problem of carry propagation delay. Power consumption is a major factor in very large scale integrated (VLSI) circuit. The central electronic circuit used for addition is adder. Adders are fundamental for wide variety of digital system. In existing adders the fast adding and consumption of low power is still challenging.

II. Proposed work

The design of 4-bit carry-select adder consists of two ripple carry adders and five multiplexers in that four are used for sum calculation and one for carry output. Adding two n-bit numbers with a carry-select adder is done with two adders in order to perform the calculation twice, one time with the assumption of the carry being zero and the other assuming one. After the two results are calculated, by using multiplexers the correct sum and carry is selected once the correct carry is known. The number of bits in each carry select block can be uniform, or variable. When variable, the chunk size should have a delay, from addition inputs "a" and "b" to the carry out, equal to that of the multiplexer chain leading into it, so that the carry out is calculated just in time. The delay is derived from standardized sizing, where the superlative number of fulladder elements per block is equal to the square root of the number of bits being added, since that will defer an equal number of Mux delays. However, the carry select adder is not area efficient because it uses multiple pairs of Ripple Carry Adders to generate partial sum and carry by considering carry input and then the final sum and carry are selected by the multiplexers.

This design has efficiently decreased the delay there by increasing the speed making it a high speed carry select adder. The factor which are advantageous in adders are as follows:

- High speed
- Low power consumption

### III. Synthesis Results

![Technology view map of carry select adder](image1)

**Figure 2:** Technology view map of carry select adder.

![Top module of carry select adder](image2)

**Figure 3:** Top module of carry select adder.

![RTL schematic of carry select adder](image3)

**Figure 4:** RTL schematic of carry select adder.

- Considering one Look up table of full adder:

![LUT Schematic of full adder](image4)

**Figure 5:** LUT Schematic of full adder.

![LUT Equation of full adder](image5)

**Figure 6:** LUT Equation of full adder.
IV. Synthesis report

Delay analysis:
Timing Summary:
Speed Grade: -4
Maximum combinational path delay: 9.069ns

Timing Detail:
All values displayed in nanoseconds (ns)
Timing constraint: Default path analysis
Total number of paths / destination ports: 49 / 5

Delay: 9.069ns (Levels of Logic = 6)
Source: b<1> (PAD)
Destination: co (PAD)

Device utilization summary:
Selected Device: 3s500efg320-4

- Number of Slices: 5 out of 4656 (0%)
- Number of 4 input LUTs: 9 out of 9312 (0%)
- Number of IOs: 14
- Number of bonded IOBs: 14 out of 232 (6%)

Total memory usage is 232188 kilobytes

Final report:
RTL Top Level Output File Name: carry_select_adder.ngr
Top Level Output File Name: carry_select_adder
Output Format: NGC
Optimization Goal: Speed
Keep Hierarchy: No

Design Statistics
# IOs: 14

Cell Usage:
# BELS: 11
# LUT3: 5
# LUT4: 4
# MUXF5: 2
# IO Buffers: 14
# IBUF: 9
# OBUF: 5

Power analysis:

- Total Thermal Power Dissipation: 323.95 mW
- Core Dynamic Thermal Power Dissipation: 0.00 mW
- Core Static Thermal Power Dissipation: 302.97 mW
- I/O Thermal Power Dissipation: 20.98 mW
- Power Estimation Confidence: Low, user-provided insufficient toggle rate data

Figure 9: Power analysis in QuartusII 9.1.
The I/O Thermal power dissipation is 20.98 mW when compared to previously proposed papers.
V. Simulation results

The results are obtained by simulating the verilog code in ModelSim 10.1e. In the above figure, the inputs are \( a=1110 \), \( b=1011 \) and \( \text{cin}=0 \) and the output \( \text{sum}=1001 \) and \( \text{carry}=1 \).

VI. Verification Result

The above figure shows the verification report of total coverage area of instances.

VII. Conclusion

The proposed design of carry select adder is simulated in ModelSim10.1, synthesized in Xilinx ISE 14.7 and power analysis is done using Quartus II9.1. The source code is written in Verilog. As we know Delay, Power and area are the major factors in VLSI design that limits the performance of any circuit. This paper concentrates more on power and speed by presenting a simple approach to reduce the delay and power of Carry select adder architecture, which helps in increasing the computational level of calculations. This proposed carry select adder has delay 9.06ns, power 20.98mw and total coverage achieved is 100%.

References


