QCA DESIGN OF ENCODER AND DECODER FOR OPTICAL COMMUNICATION

R.Swathy[1], Dr.Preeta Sharan[2]
[1]Student, [2]Professor
[1,2]Dept. of ECE, The Oxford College of Engineering,
Bommanahalli, Bangalore-560068
[1]swathyramachandra@gmail.com, [2]sharanpreeta@gmail.com

***Abstract*- A decoder and encoder is vital segments of memory, for address translating and encoding. The extent of Complementary Metal Oxide Semiconductor (CMOS) transistor continues contracting to build the thickness on contributes agreement with Moore's Law. The scaling influences the gadget execution because of requirements like warm dissemination and power utilization. A Quantum dot Cellular Automata (QCA) is a contrasting option to CMOS.QCA offers higher speed, bring down power utilization and higher thickness. It is another transistor-less calculation in nanotechnology. In this venture propose a combinational gate based decoder and encoder using Quantum dot Cellular Automata (QCA) engineering. It gives least power consumption and region minimization. A communication system can be implemented as quantum dot cellular automata. Optical communications involves encoder and decoder that can be used to generate and recognize appropriate code sequences. Hence the design of encoder and decoder is done using QCA design which ensures decrease in power and region usage.**

I. INTRODUCTION

Complementary metal-oxide-semiconductor (CMOS) innovation is in wild use in current-day semiconductor manufacture. In any case, there is a conundrum in CMOS that power expended increments with increment in speed. Be that as it may, a few applications require more speed and less power. New innovations like carbon nanofield impact transistor and quantum dot cell automata (QCA) have the ability to furnish more mix and speed alongside less power utilization and high parallel preparing. QCA is the most innovative nanotechnology in today's world which is called as Quantum Cellular Automata. In QCA, digital circuits are designed using quantum dots which are very small semiconductor particles, only of several nanometers in size. QCA has features like low power consumption, faster operational speed and reduced area when compared with CMOS designs. This is an alternative technology used for CMOS technology.QCA has a unique feature such as clockzones present in the QCA circuits. This allows the switching of the cells. The propagatedsignals are delayed because of the number of clock zones equal to number of cycles. QCA nanotechnology is a novel emerging technology, logic states are stored as electrons in a well and not stored as voltage.

An encoder is a computerized circuit that has two n input lines and n yield lines. Corresponding to the information esteem, parallel codes are generated by yield lines. A need encoder is an encoder circuit named so since it completes the need work, i.e., in the event that in excess of one sources of info are equivalent to 1 and in the meantime, priority will be given to the information having the most noteworthy need. Sweep flip-tumble contains a multiplexer (MUX) to choose either a typical task with information or output activity with check input. It has a control Contribution to choose either information or output input.

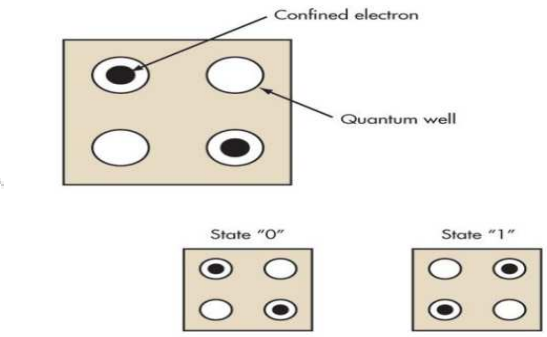

Fig.1. Quantum dot and polarization state

In communication systems, combinational and Sequential workmanship advanced rationale circuits are generally utilized. A pile of research work has been done on this theme and new strategies for investigating mistake location and rectification. This part gives an outline of the examination completed on different circuits and their applications in a few fields in writing. The part is extensively partitioned into areas ordering the QCA computerized circuits in light of the examination work done on combinational circuits, consecutive circuits, Reed Solomon mistake

control codes, Pseudo Random Generator for clamor flag age. The part additionally incorporates a concise survey of the accessible approval systems. And this encoder and decoder is used in optical fiber communication. The below block diagram shows the optical fiber communication. In optical fiber communication encoder and decoder circuit can be designed using qca technique. The block diagram contains information, encoder ,optical source, optical fiber cable, optical detector, and decoder circuit.

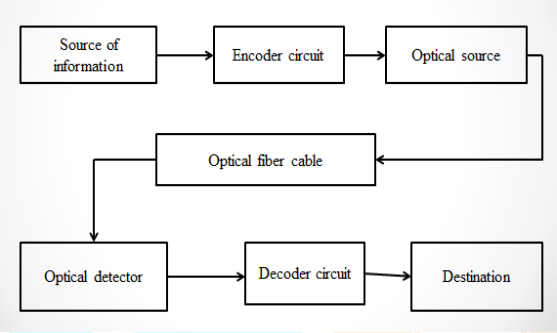

Fig.2. Optical communication system

II. *PROPOSED DESIGN*

The proposed design contains Encoder and Decoder circuits. In computerized electronic undertakings, the encoder and decoder assume a critical part. It is utilized to change over the information starting with one frame then onto the next shape. For the most part, these are habitually utilized as a part of the correspondence frameworks like media transmission, systems administration, and exchange the information from one end to the opposite end. Similarly it is additionally utilized as a part of the computerized space for simple transmission of information, set with the codes and after that transmitted. Toward the finish of the beneficiary, the coded information are gathered from the code and after that prepared to display.. The energy dissipation of the proposed design is calculated by the following equation.

The energy dissipation of the proposed designs is calculated by the equation,

$$Ediss \leq [\frac{2\gamma new}{Ek}\left(\frac{po}{pold}\gamma old - \frac{pn}{pnew}\gamma new\right) + \frac{EkPnew}{2}(pn - po)$$

The power dissipation of the design is calculated by,

$$Pdiss \leq \frac{Ediss}{\tau}$$

The encoder is a gadget or a transducer or a circuit. The encoder will change over the data starting with one arrangement then onto the next configuration i.e. like electrical signs to counters or a PLC. The input flag of the encoder will decide the position, check, speed, and heading. The control gadgets are utilized to send the order to a specific capacity. In the advanced hardware, the twofold decoder is a combinational rationale circuit that changes over the double number to the related example of yield bits. These are utilized as a part of various applications like seven section show, memory address unraveling. The capacity of the paired decoder is acquired if the given info mix has happened.The below figure shows design of encoder and decoder using qca technique.

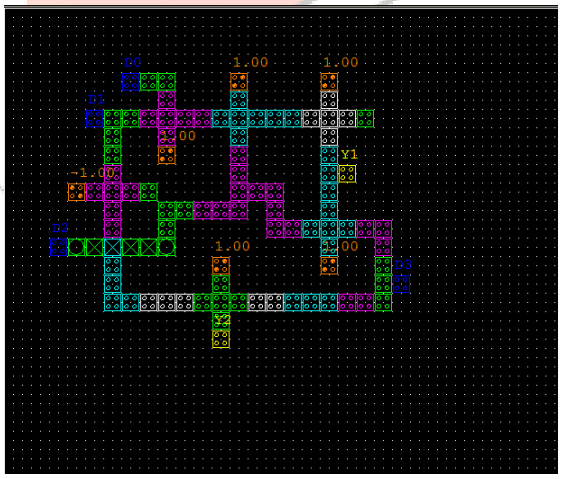

Fig.3. Layout of 4:2 Encoder

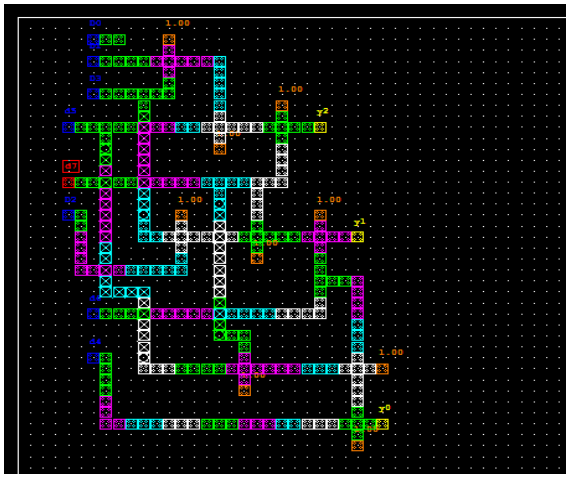

Fig.4. Layout of 8:3 Encoder

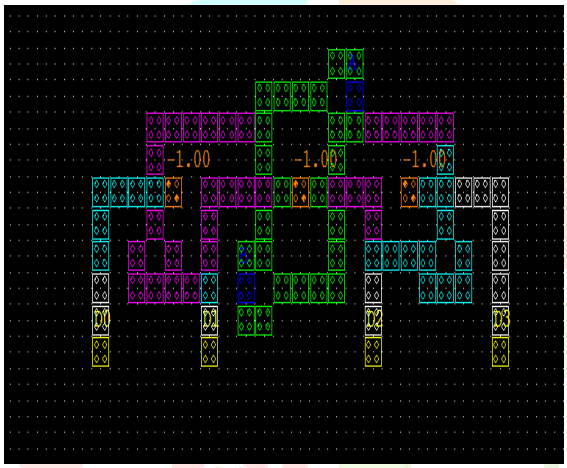

Fig.5. Layout of 2:4Decoder

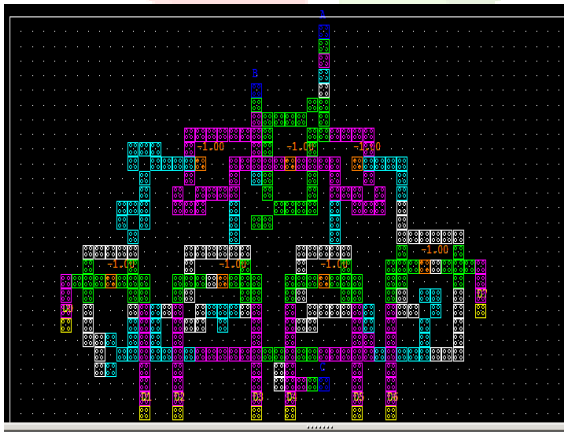

Fig.6. Layout of 3:8 Decoder

III. RESULTS AND DISCUSSIONS

In this part the design of encoder and decoder compared with power area and speed of proposed system with previous design. The results shows of power consumption is less designed using QCA technique. The simulation results of encoders and decoders of Verilog code is shown.

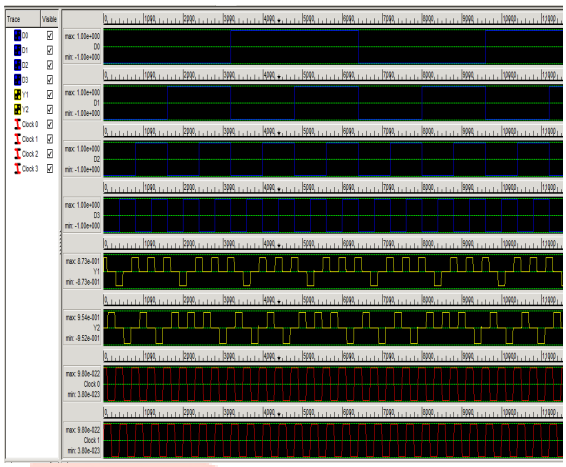

Fig.7. QCA simulation results of 4:2 Encoder.

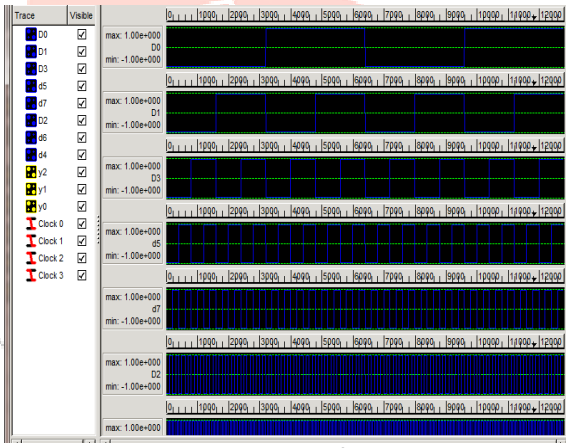

Fig.8. QCA simulation results of8:3 Encoder.

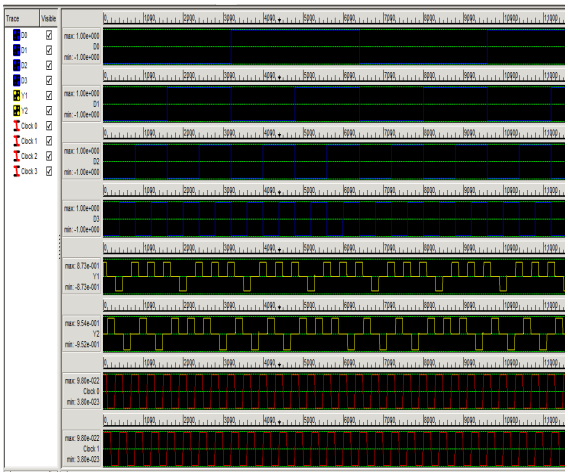

Fig.9. QCA simulation results of 2:4Decoder.

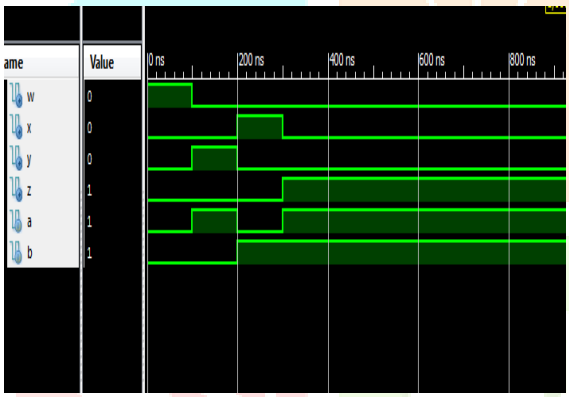

Fig.10.: simulation resut of 2to4 Decoder.

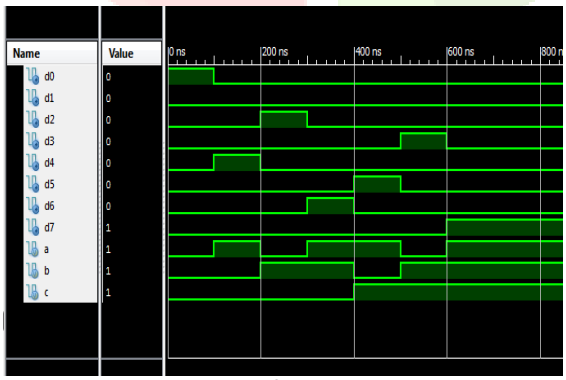

Fig.11. simulation resut of 3to8 Decoder.

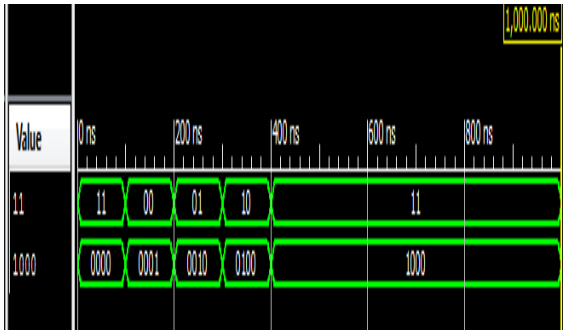

Fig.12. Simulation result of 4to2

Encoder.

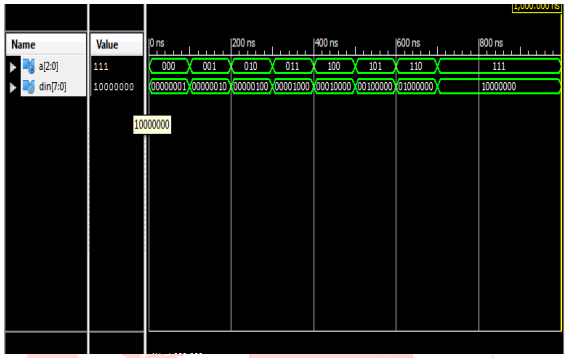

Fig.13. Simulation result of 8to3 Encoder

IV CONCLUSION

In this paper the region and multifaceted nature are the significant issues in the circuit design. QCA are a promising, rising nano-innovation in light of single electron impacts in quantum spots and atoms. Such gadgets display a little element measure, high clock recurrence and ultra low power utilization. QCA gives an elective method for registering in which the rationale states ("0" and "1") are characterized by the situation of electrons. Productive arrangement has as of late been proposed for a few number juggling circuits, for example, adders, multipliers and comparators. The outline of double comparator in view of QCA is spoken to which utilizes the current QCA greater part entryways for actualizing the double comparator. In this outline we attempt to decrease the improvement parameters like complexity, area and power consumption. The proposed outlined of encoder and decoder for optical fiber correspondence contrasted and past one regarding multifaceted nature (number larger part doors utilized), speed, region and control utilization this gives the proposed plan of comparator in QCA is more proficient than the earlier outline.

Design	QCA design	CMOS design
4:2 Encoder	1.1361x10^15/τ	32x10^-3
8:3 Encoder	0.4024x10^15/τ	27.12x10^-3
2:4 Decoder	1.1846x10^15/τ	32.03x10^-3
3:8 Decoder	0.3542x10^15/τ	40.78x10^-3

Table 1. Comparison of power dissipation

Design	QCA design(nm^2)	CMOS design(nm^2)
4:2 Encoder	13	18607.95
8:3 Encoder	43	20785.02
2:4 Decoder	9	17560.82
3:8 Decoder	43	22540.65

Table 2. Comparison of area

REFERENCES

[1]Lim, Lee Ai, et al. ―SEQUENTIAL CIRCUIT DESIGN USING QUANTUM DOT CELLULARAutomata(QCA)Circuits and systems (ICCAS), 2012 IEEE InternationalConference on. IEEE, 2012.

[2]H. Thapliyal, N. Ranganathan, S. Kotiyal, ―DESIGN OF TESTABLE REVERSIBLE SEQUENTIAL CIRCUITS, IEEE Trans. on VLSI Systems., vol.21,pp. 1201-1209, 2013.

[3] S. Hashemi, K. Navi, ―REVERSIBLE MULTIPLEXER DESIGN IN QUANTUM-DOT CELLULAR AUTOMATA, Quantum Matter, vol. 3, pp. 523-528, 2014.

[4]. D. De, S.Bhattacharaya, K.P. Ghatak,―QUANTUM DOTS AND QUANTUM CELLULAR AUTOMATA: RECENT TRENDS AND APPLICATIONS, Nova Science Publishers, Inc., USA, 2013.

[5]. M. Kianpour and R. Sabbaghi-Nadooshan, ―A NOVEL QUANTUM-DOTCELLULAR AUTOMATA X-BIT × 32- BIT SRAM", IEEE Transaction on VLSI, 2015.

[6] M. Kianpour and R. Sabbaghi-Nadooshan, ―A CONVENTIONAL DESIGN FOR CLB IMPLEMENTATION OF A FPGA IN QUANTUM-DOT CELLULAR AUTOMATA (QCA), in Proc. IEEE Int. Symp. Nanoarch, July 2012.

[7] S. Angizi, S. Sarmadi, S. Sayedsalehi, K. Navi, ―DESIGN AND EVALUATION OF NEW MAJORITY GATE-BASED RAM CELL IN QUANTUM-DOT CELLULAR AUTOMATA, Microelectron. J. 46 (2015) (Elsevier).

[8] Arvind Kumar Mishral ,Debiprasad Priyabrata Acharya ,Pradip Kumar Patra―NOVEL DESIGN TECHNIQUE OF ADDRESS DECODER FOR SRAM2014 IEEE International Conference on Advanced Communication Control and Computing Technologies (ICACCCT)

[9] Himanshu Thapliyal, Nagarajan Ranganathan and Saurabh Kotiyal ―DESIGN OF TESTABLE REVERSIBLE SEQUENTIAL CIRCUITS" IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 21, NO. 7, JULY 2013 .