# INVESTIGATION OF COMMON MODE VOLTAGE IN 5-LEVEL DIODE CLAMPED MLI USING CARRIER BASED SPWM TECHNIQUES

Mohd Esa<sup>1</sup>, J.E.Muralidhar<sup>2</sup>

<sup>1</sup>M.E Student, Department of EEE, MJCET, Hyderabad

<sup>2</sup>Associate Professor, Department of EEE, MJCET, Hyderabad

<sup>1</sup>zmohdesa@gmail.com

Abstract: The main aim of this paper is to investigate the Common Mode Voltage (CMV) and Total Harmonic Distortion (THD) in five level Diode Clamped Inverter using Carrier based SPWM techniques. The common mode voltage exists between neutral point of star connected load and system ground. Various Carrier based SPWM techniques used to analyze CMV and THD in this paper are Phase Disposition (PD) strategy, Phase Opposition Disposition (POD) strategy, Alternative Phase Opposition Disposition (APOD) strategy, Carrier Overlap Phase Disposition (COPD) Strategy, Carrier Overlap Phase Opposition Disposition (COAPOD) strategy.RL load is connected to inverter circuit for analysis purpose and Simulation is performed using MATLAB/Simulink Software.

IndexTerms: CMV, DCMLI, SPWM Techniques

## I. INTRODUCTION

Common mode voltage is the voltage between neutral point of load and system ground [1] (or) voltage between star point of load and D.C. midpoint (or) The common mode voltage (CMV) of the three-phase system is defined as the voltage potential difference between the star point of the load network and the mid-point of the D.C. link capacitors[2].CMV always exists in PWM converters regardless of number of levels and legs because of its switching operation. The high frequency and high amplitude CMV produced by PWM inverter causes common mode current (CMC) via parasitic capacitor components between converter, loads, cables and ground respectively. This CMC could be a source of consequent electromagnetic interference (EMI) noise & it may result in mal operation of converter control system [3].CMV produced by PWM inverters induces shaft voltages on the rotor, when this shaft voltage exceeds voltage limit of the lubricant in the bearings, results in large bearing currents, and this cause's premature failure of bearings of induction motor [4]. Multilevel inverter is one of the options to reduce this problem [5]. This paper is an attempt to investigate CMV in 5-level Diode clamped Inverter using carrier based SPWM techniques.





Fig.2(a).Line voltage waveform for 5-level DCMLI



Fig.2(b).Phase voltage waveform for 5-level DCMLI

Fig.1.Five level DCMLI

## **II. CARRIER BASED SPWM TECHNIQUES**

To control the output voltage of inverter different modulation strategies exists [6]. The main modulation techniques are Sinusoidal Pulse Width Modulation (SPWM) [7], Space Vector Pulse Width Modulation and Selective Harmonic Elimination Pulse Width Modulation (SHEPWM). SPWM is simplest of all the above techniques. It was introduced by Schonung and Stemmler in 1964[8]. In carrier based SPWM technique for MLI, (m-1) triangular carriers are compared with one sinusoidal modulating signal. Where m is output level of inverter. Thus for five level inverter four carriers are required [9]. The carrier based SPWM techniques are classified according to non-overlapping carrier SPWM strategies and overlapping Carrier SPWM strategies.

Non overlapping carrier based SPWM Techniques are classified as follows

- 1. *Phase Disposition (PD):* All the carrier signals of same frequency, amplitude and phase, but having different DC offset occupy levels one above the other are compared with a single sinusoidal modulating signal. All carriers above and below zero reference are in same phase in PD SPWM technique [10].
- 2. *Phase Opposition Disposition (POD):* This method also contains carrier signals one above the other with same frequency, amplitude but differ in phase, the carrier signals above reference zero voltage are in 180 degree out of phase with the carrier signals below the zero reference voltage [10].
- 3. Alternative Phase Opposition Disposition (APOD): In APOD-SPWM technique the carrier signal of same amplitude are phase displaced from each other by 180° from its neighboring carrier signals.

Overlapping carrier based SPWM Techniques are classified as follows

- 1. *Carrier Overlapped Phase Disposition (COPD):* Carriers in this technique overlapped each other such that overlapping carrier distance between each carrier is half of the amplitude of carrier signal. In COPD all overlapped carriers are in same phase.
- 2. Carrier Overlapped Phase Opposition Disposition (COPOD): Carriers are divided equally into two groups according to positive/negative average levels. In this type two groups are opposite in phase with each other while keeping in phase within the group.
- 3. Carrier Overlapped Alternative Phase Opposition Disposition (COAPOD): Amplitude of carriers are overlapped with neighbouring carriers phase shifted by 180 degrees from each other.

#### **III. RESULTS & DISCUSSIONS**

A 5-level diode clamped inverter using PD, POD, APOD, COPD, COPOD, COAPOD SPWM techniques is simulated in MATLAB Simulink. Figure 3 and figure 4 shows simulation results for PD SPWM and POD SPWM Controlled 5-level inverter. In PD SPWM controlled 5-level DCMLI the rms value of CMV is 40.33 V and THD of 39.30% is observed in phase voltage. In POD SPWM controlled 5- level DCMLI the rms value of CMV is 18.76 and THD of 38.53% is observed in phase voltage.





Fig.4.POD-SPWM Controlled five level DCMLI (a) Carrier arrangement (b) Phase Voltage (c) CMV waveform (d) Harmonic Spectrum Figure 5 and figure 6 shows simulation results for APOD SPWM and COPD SPWM Controlled 5-level inverter. In APOD SPWM controlled 5-level DCMLI the rms value of CMV is 31.14 V and THD of 39.34% is observed in phase voltage. In COPD SPWM controlled 5- level DCMLI the rms value of CMV is 56.89 and THD of 43.45% is observed in phase voltage



Figure 7 and figure 8 shows simulation results for COPOD and COAPODSPWM Controlled 5-level inverter. In COPOD SPWM controlled 5-level DCMLI the rms value of CMV is 31.46 V and THD of 39.56 % is observed in phase voltage. In COAPOD SPWM controlled 5- level DCMLI the rms value of CMV is 21.35 and THD of 37.57 % is observed in phase voltage







Table 2 shows CMV and %THD of 5-level Diode Clamped Inverter for 440V input DC voltage, 50Hz System frequency, 1000 Hz switching frequency. Load resistance and Inductance of 100 Ohms and 50e-3 Henry are considered for analysis.

Method	CMV(V)	THD (%)
PD	40.33	39.30
POD	18.76	38.53
APOD	31.14	39.34
COPD	56.89	43.45
COPOD	31.46	39.56
COAPOD	21.35	37.57

Table 2: CMV and %THD of 5-level DCMLI from different SPWM Methods

Figure 9 shows variation of CMV and %THD for various SPWM Techniques. It can be clearly observed that POD SPWM controlled 5-level DCMLI has less CMV when compared to other SPWM techniques and THD is less in COAPOD controlled 5-level DCMLI.



Fig.9. Variation of CMV and %THD for various SPWM Techniques

## **IV. CONCLUSION**

Five level Diode clamped inverter using Phase Disposition, Phase Opposition Disposition, Alternative Phase Opposition Disposition, Carrier Overlapped Phase Disposition, Carrier Overlapped Phase Opposition Disposition and Carrier Overlapped Alternative Phase Opposition Disposition SPWM techniques is simulated in MATLAB/Simulink Software. Simulation results evidently shows that 5-level DCMLI using POD SPWM technique produces less CMV and COAPOD SPWM technique produces less %THD in phase voltage. Shaft voltage and Bearing currents are also less in POD SPWM technique since they depends on CMV.Thus POD SPWM technique is considered as best option for better operation of IM drives from above discussed techniques.

## REFERENCES

- P. G. Shewane, S. Gaigowal, B. Rane, "Multicarrier Based SPWM Modulation for Diode Clamped MLI to reduce CMV and THD", Power, Automation and Communication [INPAC-2014], International Conference at Amravati on 6-8 OCT.2014, pp. 50-54, DOI:10.1109/INPAC.2014.6981134, IEEE.
- [2] E. Un and A. M. Hava, "A Near-State PWM Method With Reduced Switching Losses and Reduced Common-Mode Voltage for Three-Phase Voltage Source Inverters," Industry Applications, IEEE Transactions on, vol. 45, pp. 782-793, 2009.
- [3] Min Zhang, "Investigation of Switching Schemes for Three-phase Four-Leg Voltage Source Inverters", A thesis submitted for the degree of Doctor of Philosophy June, 2013, School of Electrical and Electronic Engineering, Newcastle University
- [4] Anuradha V.Jadhav and Mrs.P.V.Kapoor, "Reduction of common mode voltage using Multilevel Inverter", Energy Efficient Technologies for Sustainability [ICEETS], pp.586-590, 06 October 2016,DOI:10.1109/ICEETS.2016.7583822,IEEE.

## www.ijcrt.org © 2017 IJCRT | National Conference Proceeding NTSET Feb 2018 | ISSN: 2320-2882 National Conference On Trends In Science, Engineering & Technology by Matrusri Engineering College & IJCRT

- [5] M.M.Renge and H.M.Suryawanshi, "Multilevel Inverter to Reduce Common Mode Voltage in AC Motor Drives Using SPWM Technique." pp.21-27, Journal of Power Electronics, Vol. 11, No. 1, January 2011.
- [6] Muhammad H. Rashid, "Power Electronics Hand book", fourth edition, Butterworth-Heinemann, pp.399-400.
- [7] Mohd Esa and Mohd Abdul Muqeem Nawaz, "THD analysis of SPWM & THPWM Controlled Three phase Voltage Source Inverter", International Research Journal of Engineering and Technology (IRJET), vol. 04, no. 10, pp. 391-398, 2017.
- [8] J.Y. Lee, and Y.Y. Sun, "A New SPWM Inverter with Minimum Filter Requirement", International Journal of Electronics, Vol. 64, No. 5, pp.815-826, 1988.
- [9] McGrath, B.P.; Holmes, D.G.; "Multicarrier PWM strategies for multilevel inverters," Industrial Electronics, IEEE Transactions on, vol.49, no.4, pp. 858- 867, Aug 2002 DOI:10.1109/TIE.2002.801073.
- [10] Mohd Esa, Mohd Abdul Muqeem Nawaz and Syeda Naheed," Harmonic Analysis of Three level Flying Capacitor Inverter ", International Research Journal of Engineering and Technology (IRJET), vol. 04, no. 10, pp. 1687-1694, 2017.

