IJCRT.ORG ISSN : 2320-2882

INTERNATIONAL JOURNAL OF CREATIVE RESEARCH THOUGHTS (IJCRT)

An International Open Access, Peer-reviewed, Refereed Journal

Design and Analysis of a Low-Power Full Adder in 90-nm CMOS Using Transistor-Level Optimization

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Abstract

This paper presents a transistor-size-optimized one-bit static complementary metal–oxide–semiconductor (CMOS) full adder implemented in a 90-nm process. The design retains the robust complementary pull-up and pull-down topology of a conventional 28-transistor full adder while assigning device widths according to path criticality. Output-driving devices are strengthened to reduce transition time, whereas selected internal devices are minimized to reduce switched capacitance and leakage. The circuit was developed in Cadence Virtuoso using the GPDK090 design kit and evaluated with the Spectre simulator at a nominal supply voltage of 1 V. The reported flow includes schematic-level functional verification for all eight input combinations, transient analysis, layout implementation, design-rule checking, layout-versus-schematic verification, parasitic extraction, and post-layout validation. The source simulation results report an average power consumption of 0.313 µW and an average propagation delay of 8.21 ps, corresponding to a power–delay product of approximately 2.57 aJ. The static CMOS topology provides full-swing outputs and strong noise margins, making the cell a candidate for low-power arithmetic datapaths. To support reproducibility, this manuscript also identifies the testbench parameters and device dimensions that must be reported in the final submission.

Keywords - full adder, low-power VLSI, static CMOS, 90-nm technology, transistor sizing, Cadence Virtuoso, propagation delay, power–delay product.

1. Introduction

Energy efficiency is a central constraint in contemporary digital integrated circuits, particularly in battery-operated embedded platforms, Internet-of-Things nodes, wearable electronics, and edge-computing devices. Arithmetic units often dominate the active datapath of these systems, and the performance of the full-adder cell directly affects the power, delay, and area of adders, multipliers, accumulators, and arithmetic logic units.

A one-bit full adder combines three binary inputs - A, B, and carry-in (CIN) - to produce a sum bit and carry-out (COUT). Because many arithmetic structures cascade a large number of full-adder cells, small improvements at cell level can accumulate into meaningful system-level gains. However, aggressive reductions in transistor count may introduce degraded logic levels, limited driving capability, reduced noise margin, or sensitivity to process and loading conditions.

Conventional static CMOS logic remains attractive because it provides complementary pull-up and pull-down networks, rail-to-rail outputs, negligible static current in the ideal steady state, and strong robustness. Its main disadvantages are the relatively high device count and the capacitance associated with internal nodes. This work therefore investigates transistor sizing as an optimization mechanism that preserves static-CMOS reliability while reducing switching energy and critical-path delay.

The proposed design is implemented in the Cadence Virtuoso environment using GPDK090. The source results report 0.313 µW average power and 8.21 ps average propagation delay at a 1 V supply. Unlike a purely schematic study, the intended flow includes layout, DRC, LVS, parasitic extraction, and post-layout simulation. The present manuscript organizes the work in a form suitable for journal submission and explicitly separates reported results from experimental parameters that still require author confirmation.

2. Literature Review

Full-adder design has been explored using static CMOS, transmission gates, complementary pass-transistor logic, double-pass logic, gate-diffusion-input structures, and hybrid combinations. Reduced-device implementations can lower switched capacitance and, under suitable loading, improve delay. Their benefits can diminish when the cells are cascaded because pass devices may exhibit threshold-related voltage loss, output restoration may be required, and weak internal nodes may be sensitive to fan-out and process variation.

Zimmermann and Fichtner compared CMOS and pass-transistor logic styles and highlighted the trade-off between device count, signal integrity, power, and speed. Bui et al. and Lin et al. investigated compact 10-transistor full adders aimed at lowering energy and delay. These designs established the value of XOR/XNOR optimization, but compact architectures must be evaluated carefully under realistic drive and loading conditions.

Classical work on parallel adders by Brent and Kung and on area-efficient adders by Han and Carlson demonstrates that cell-level delay and carry-driving capability influence complete arithmetic structures. Standard texts on CMOS design further show that device sizing changes effective resistance, parasitic capacitance, short-circuit current, and rise/fall balance. Consequently, sizing cannot be treated independently of input slew, output capacitance, process corner, temperature, and layout parasitics.

The present work differs from transistor-count-reduction approaches by retaining a 28-transistor static-CMOS structure and optimizing individual device widths. The objective is not solely to minimize one metric, but to achieve a practical balance among power, delay, full-swing operation, noise immunity, and layout correctness.

3. Research Gap and Contributions

Many reported full-adder designs emphasize either low power or high speed but do not provide a complete physical-design verification flow. Moreover, performance values are frequently compared across different technologies, supply voltages, input patterns, output loads, and measurement definitions, which can make direct ranking unreliable. A reproducible study should therefore report both the circuit topology and the exact testbench conditions.

The contributions of this work are as follows:

- A 28-transistor static-CMOS one-bit full adder implemented in a 90-nm process.
- Path-aware PMOS and NMOS sizing intended to reduce switched capacitance while strengthening critical output paths.
- Schematic verification, transient simulation, layout implementation, DRC, LVS, parasitic extraction, and post-layout validation in Cadence Virtuoso/Spectre.
- Evaluation using average power, propagation delay, and power–delay product.
- A reproducibility-oriented reporting framework that identifies the device and testbench parameters required for defensible comparison.

4. Proposed Full-Adder Design

4.1 Logic Function

The one-bit full adder accepts inputs A, B, and CIN and generates SUM and COUT. Its Boolean functions are

$$SUM = A \oplus B \oplus C_{in} \quad (1)$$

$$C_{out} = AB + AC_{in} + BC_{in} \quad (2)$$

$$C_{out} = AB + C_{in}(A \oplus B). \quad (3)$$

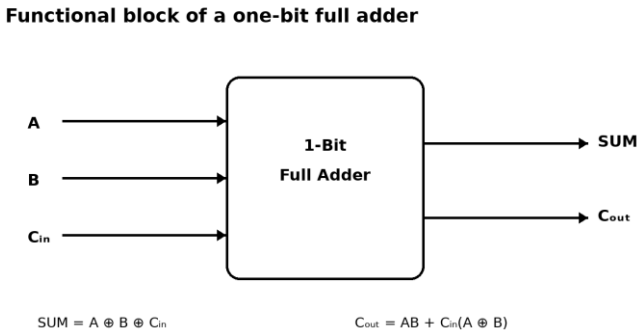

Fig. 1. Functional block and Boolean expressions of the one-bit full adder.

A	B	CIN	SUM	COUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 1. Truth table of the one-bit full adder.

4.2 Static-CMOS Topology

The proposed circuit uses complementary PMOS pull-up and NMOS pull-down networks. For each stable input combination, one network connects the output to a supply rail while the complementary network is off. This structure provides full voltage swing and good static noise margin without requiring level-restoration stages.

The source design retains a conventional 28-transistor organization. The exact decomposition of the XOR/XNOR and carry networks, along with transistor labels, must be visible in the final schematic so that the reported sizing strategy can be independently reproduced.

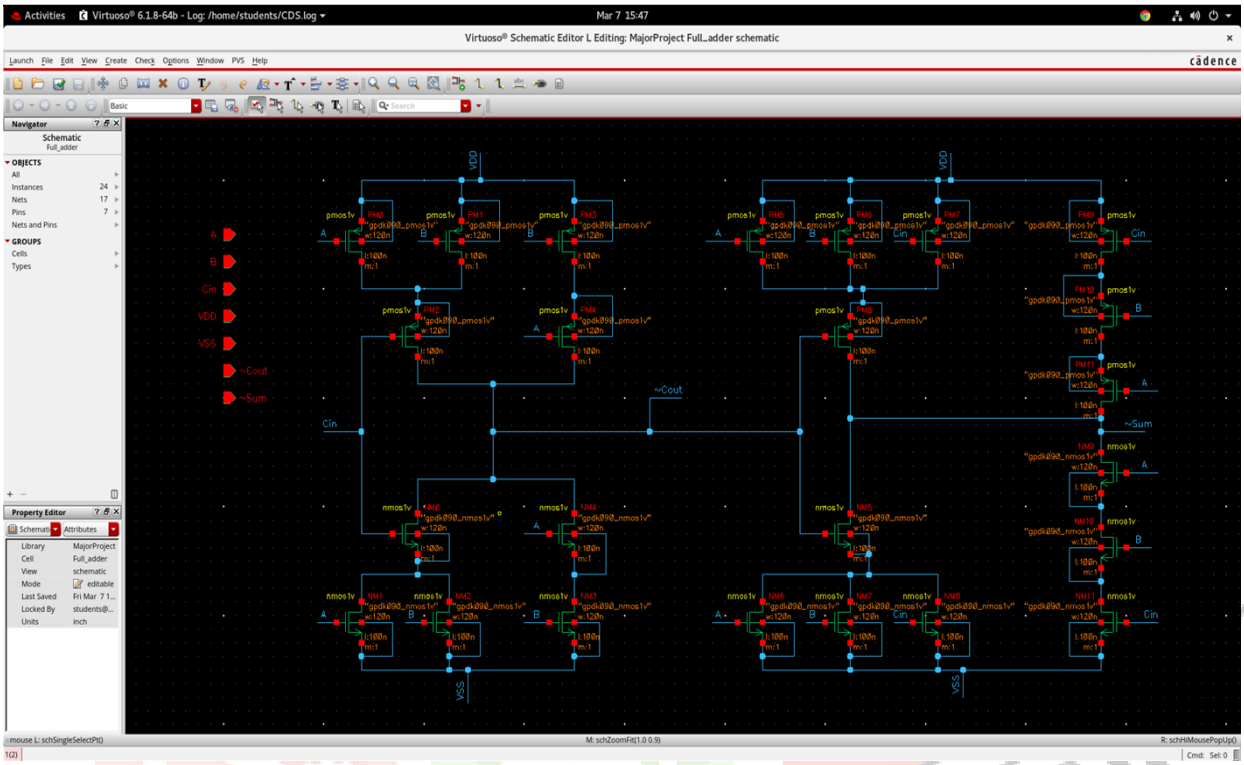

Fig. 2. The optimized transistor-level schematic and final W/L annotations.

4.3 Transistor-Level Optimization

Uniform minimum-size devices do not necessarily minimize energy or delay. Devices in series stacks have higher effective resistance, while excessively wide devices increase diffusion and gate capacitance. The optimization strategy used in this work is summarized below:

- Increase the width of output-driving devices and devices on the measured critical path.
- Use smaller devices on noncritical internal nodes to limit parasitic capacitance and leakage.
- Adjust the PMOS-to-NMOS width ratio to balance low-to-high and high-to-low transition times.
- Avoid unnecessary upsizing of nodes with high switching activity.
- Validate the final dimensions after parasitic extraction rather than relying only on schematic-level delay.

For publication, Table 2 must be completed with every unique transistor group. Reporting only the optimization concept is insufficient for independent replication.

Device group	Function	Sizing rationale
Input/XOR network	Internal logic	Low capacitance with valid full-swing operation
Carry-generation network	Critical carry path	Reduced COUT delay
SUM output driver	Output drive	Balanced SUM rise/fall transitions
COUT output driver	Output drive	Required fan-out and load drive

Table 2. Transistor dimensions to be reported in the final paper.

4.4 Design and Verification Flow

The implementation flow starts from electrical specifications, proceeds through schematic capture and device sizing, and ends with post-layout verification. The sequence used in this work is shown in Fig. 3.

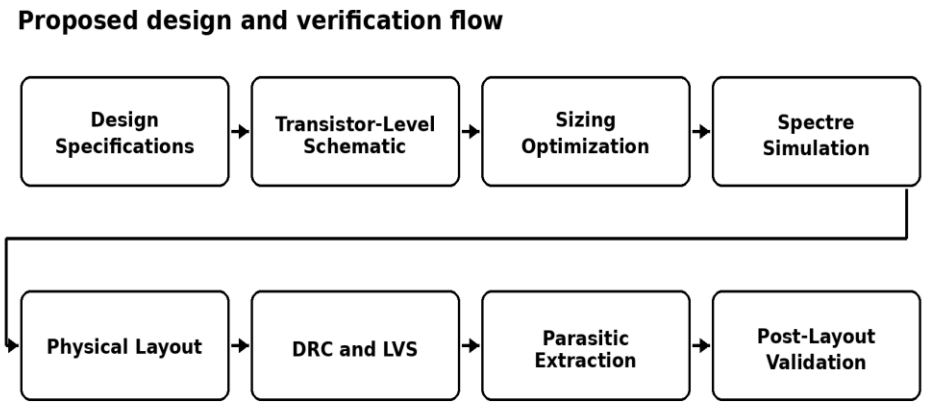

Fig. 3. Proposed schematic-to-post-layout design and verification flow.

5. Experimental Setup and Measurement Method

The source material identifies the process, design environment, simulator, and nominal supply voltage. Several additional parameters are required to make the power and delay results reproducible. They are retained as explicit completion fields in Table 3.

Parameter	Value / required author input
Technology/design kit	GPDK090, 90-nm CMOS
EDA platform	Cadence Virtuoso Custom IC Design
Simulator	Cadence Spectre
Supply voltage	1.0 V
Process corner	[insert: TT/SS/FF/FS/SF]
Temperature	[insert: °C]
Input pattern	All eight A–B–CIN combinations
Input frequency/period	[insert]
Input rise and fall time	[insert]
Output load capacitance	[insert: fF]
Simulation duration and time step	[insert]
Power measurement interval	[insert steady-state window]
Delay threshold	Recommended: 50% VDD input to 50% VDD output
Reported result type	[confirm: schematic or post-layout]

Table 3. Simulation and measurement conditions.

Average power should be measured over an integer number of complete input-pattern periods after initial transients have settled. Propagation delay should be reported separately for low-to-high and high-to-low output transitions and then averaged using a clearly stated definition. The final paper should also identify whether the 8.21 ps value is the maximum, arithmetic mean, or mean of tPLH and tPHL across selected transitions.

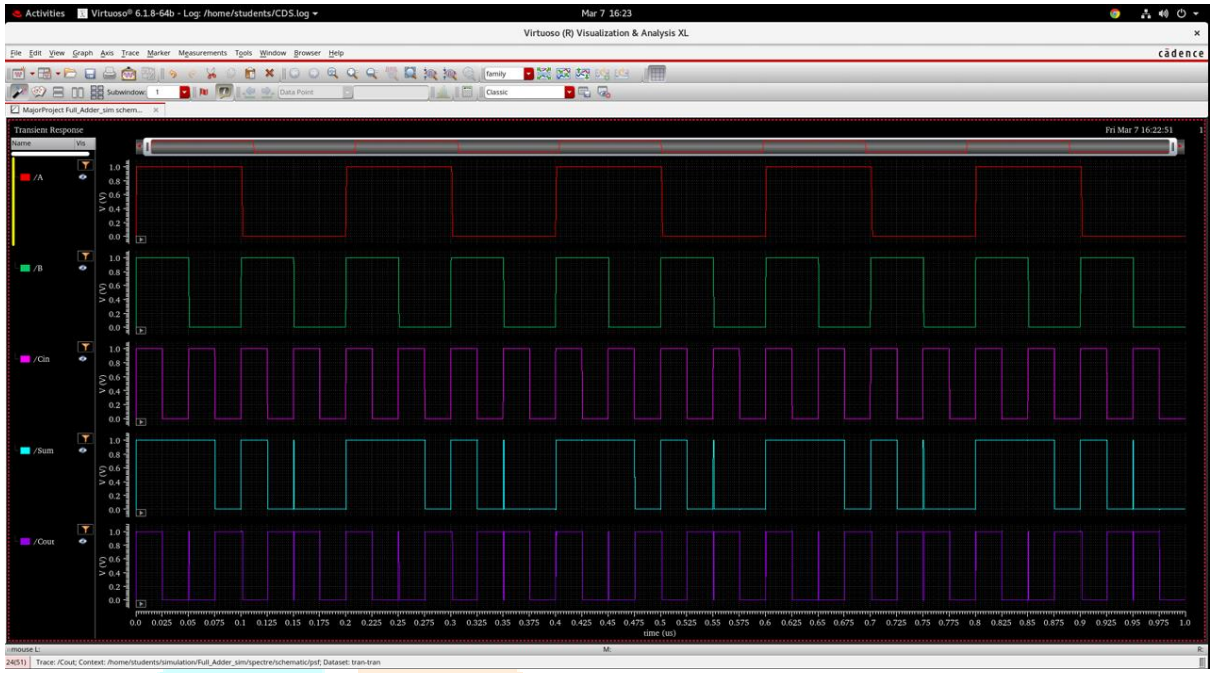

Fig. 4. Input/output transient waveforms and delay cursors.

6. Results and Discussion

6.1 Functional Verification

The source simulations applied all eight combinations of A, B, and CIN. The reported SUM and COUT outputs followed the truth table in Table 1 and exhibited full-swing logic levels. The final manuscript should support this statement with the waveform export in Fig. 4 and should report the observed minimum high level, maximum low level, and any transient glitches under the stated load.

6.2 Power, Delay, and Power–Delay Product

The source material reports an average power consumption of 0.313 µW and an average propagation delay of 8.21 ps. Using these reported values, the power–delay product is

$$PDP = Pavg \times tpd \quad (4)$$

$$PDP = (0.313 \times 10^{-6}\ W)(8.21 \times 10^{-12}\ s) \approx 2.57 \times 10^{-18}\ J = 2.57\ aJ. \quad (5)$$

Metric	Reported value	Interpretation
Average power	0.313 µW	Confirm measurement window and whether extracted parasitics were included.
Average propagation delay	8.21 ps	Confirm transition set, output, load, threshold, and averaging method.
Power–delay product	2.57 aJ	Calculated from the two reported values.

Table 4. Reported performance metrics of the proposed full adder.

6.3 Physical Verification

The reported physical-design flow includes successful DRC and LVS verification followed by parasitic extraction and post-layout simulation. These steps are essential because interconnect and diffusion parasitics can alter both switching delay and dynamic power. The final paper should report the layout area, number of DRC errors, LVS status, extraction view used, and the difference between pre-layout and post-layout metrics.

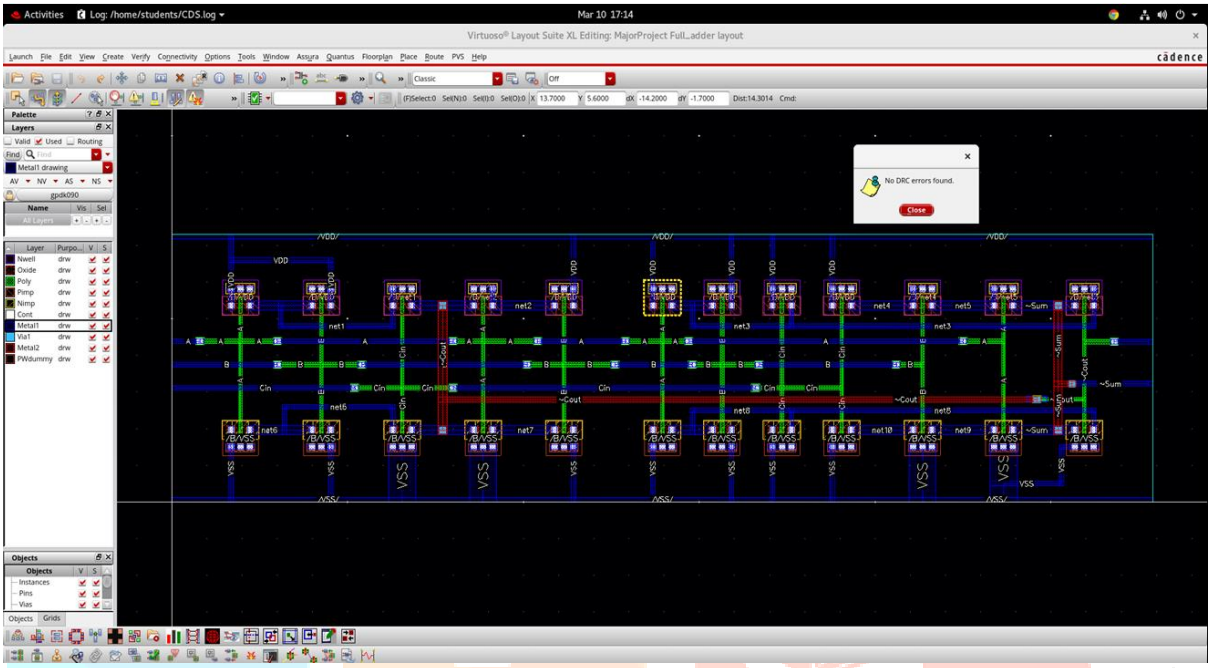

Fig. 5. Final layout, area annotation, and DRC/LVS evidence.

6.4 Comparative Evaluation

The source draft provides the indicative comparison shown in Table 5. Because the cited ranges are not yet tied to individually verified references and may have been obtained under different loads, supply conditions, input slews, or measurement definitions, the table must not be presented as a strict like-for-like benchmark until each value is traced to its source and normalized where possible.

Parameter	Conventional CMOS	Hybrid full adder	Proposed static CMOS
Technology	90 nm	90 nm	90 nm
Supply voltage	1 V	1 V	1 V
Average power	1.20–1.76 µW	0.67–0.90 µW	0.313 µW
Propagation delay	12–18 ps	9–12 ps	8.21 ps
Voltage swing	Full	Partial in some designs	Full
Noise immunity	High	Architecture dependent	High
Physical verification	Not consistently reported	Limited/varies	DRC and LVS reported

Table 5. Indicative comparison retained from the source draft; replace with fully cited matched-condition data.

Subject to confirmation under matched conditions, the reported values suggest that sizing optimization can lower the energy of a robust static-CMOS cell without resorting to a reduced-swing pass-transistor topology. The principal strength of the method is therefore its compatibility with full-

swing operation and a standard custom-layout flow. The principal limitation is that the present evidence does not yet include the complete device table, layout area, PVT sweep, Monte Carlo analysis, or a fully normalized comparison dataset.

7. Limitations and Reproducibility Requirements

Before journal submission, the authors should address the following limitations within the manuscript rather than only in supplementary correspondence:

- Provide the complete 28-transistor schematic with all W/L values and identify the baseline sizing used before optimization.
- Report process corner, temperature, input slew, output capacitance, input frequency, simulation length, and power-measurement window.
- Separate schematic and post-layout power, delay, and PDP values.
- Report SUM and COUT delays individually, including tPLH, tPHL, worst-case delay, and the averaging rule.
- Add PVT and, preferably, Monte Carlo results to demonstrate robustness against process and mismatch variation.
- Rebuild the literature-comparison table from traceable publications under the closest available matched conditions.
- Report layout area and the percentage change in area caused by transistor upsizing.

8. Conclusion

This work presents a low-power one-bit full adder implemented using a 28-transistor static-CMOS topology in a 90-nm process. The proposed method uses transistor-level sizing to strengthen critical output paths and reduce unnecessary internal capacitance while preserving full-swing static-CMOS operation.

The design was developed in Cadence Virtuoso and the reported flow includes Spectre simulation, layout generation, DRC, LVS, parasitic extraction, and post-layout validation. The source results report 0.313 µW average power and 8.21 ps average propagation delay at 1 V, yielding a calculated PDP of approximately 2.57 aJ.

These results indicate the potential of path-aware sizing as a practical optimization technique for low-power arithmetic cells. A defensible final publication, however, must include the complete transistor dimensions, exact measurement conditions, layout area, pre-/post-layout comparison, and traceable matched-condition literature data. With those additions, the work can provide a useful full-swing building block for adders, multipliers, DSP datapaths, embedded processors, and energy-constrained edge systems.

9. Future Work

Future work should evaluate the optimized cell across supply-voltage and temperature ranges, process corners, and Monte Carlo variations. The design can then be embedded in ripple-carry, carry-look-ahead, carry-save, and multiplier structures to assess scalability under realistic interconnect and fan-out. Further comparisons may include multi-threshold CMOS, power gating, adaptive voltage scaling, FinFET or gate-all-around technologies, and emerging devices, provided that all alternatives are evaluated with a consistent testbench and measurement methodology.

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