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DESIGN AND ANALYSIS OF A LOW-POWER CMOS COMPARATOR IN 90-nm GPDK TECHNOLOGY FOR ADC APPLICATIONS

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Abstract— Low-power and high-speed comparators are essential components of Analog-to-Digital Converters (ADCs) used in portable electronics, wireless communication, biomedical instruments, and IoT devices. This paper presents the design and simulation of a low-power regenerative latch-based CMOS comparator implemented using 90 nm Generic Process Design Kit (GPDK) technology. The proposed design utilizes dynamic clocked operation, positive feedback, and optimized transistor sizing to reduce power consumption while ensuring reliable and high-speed operation. The comparator was designed in the Cadence Virtuoso environment and simulated using the Spectre simulator at a 1 V supply voltage and 100 MHz operating frequency. Performance was evaluated through transient, power, temperature, process-corner, and Monte Carlo analyses. Simulation results achieved an average power consumption of 18.2 µW, a propagation delay of 80 ps, and an input-referred offset voltage of 2.6 mV. The proposed comparator demonstrates stable operation and improved energy efficiency, making it suitable for modern low-power ADC and mixed-signal VLSI applications.

Keywords: Low-Power CMOS Comparator, Analog-to-Digital Converter (ADC), Dynamic Comparator, Regenerative Latch, Cadence Virtuoso.

I. INTRODUCTION

The rapid advancement of portable electronic devices, wireless communication systems, biomedical instruments, and Internet of Things (IoT) applications has created a growing demand for high-speed and energy-efficient Analog-to-Digital Converters (ADCs). An ADC serves as the interface
between the analog and digital domains by converting real-world analog signals into digital data for processing. Among the fundamental building blocks of an ADC, the comparator plays a critical role because it determines the conversion accuracy, operating speed, and overall power efficiency of the system. Therefore, the design of an efficient comparator is essential for improving the
performance of modern mixed-signal integrated circuits. Recent developments in CMOS technology have enabled the fabrication of highly integrated circuits with reduced chip area and lower supply voltages. Although technology scaling improves circuit density and operating frequency, it also introduces several design challenges, including increased leakage current,

process variations, transistor mismatch, reduced voltage headroom, and greater sensitivity to noise. These challenges make it difficult to design comparator circuits that simultaneously achieve low power consumption, high switching speed, and reliable operation. Since many modern electronic systems are battery-powered, minimizing power dissipation while maintaining high performance has become a primary objective in comparator design.

Several comparator architectures have been proposed for ADC applications, including static comparators, dynamic comparators, and regenerative latch-based comparators. Static comparators provide continuous operation but consume significant static power. Dynamic comparators eliminate static power consumption; however, they may experience higher offset voltage, kickback noise, and reduced performance under process and temperature variations. Although double-tail comparator architectures improve speed and support low-voltage operation, unnecessary current flow during the amplification phase can still increase dynamic power consumption and reduce energy efficiency. Consequently, there is a need for comparator designs that provide an improved balance between power consumption, propagation delay, and operational reliability.

To address these challenges, this work presents the design and analysis of a low-power regenerative double-tail CMOS comparator implemented using 90 nm Generic Process Design Kit (GPDK) technology. The proposed design incorporates a control transistor (M14) to disconnect the pre-amplifier after sufficient signal amplification, thereby minimizing unnecessary power dissipation without affecting the regenerative operation of the latch stage. The comparator is designed using the Cadence Virtuoso environment and evaluated through transient, delay, power, temperature, process-corner, and Monte Carlo simulations. Simulation results demonstrate that the proposed design achieves an average power consumption of 18.2 µW, a propagation delay of 80 ps, and an input-referred offset voltage of 2.6 mV while maintaining stable performance under different operating conditions. These characteristics make the comparator suitable for low-power and high-speed ADC applications.

The main contributions of this work are summarized as follows:

• Design and implementation of a regenerative double-tail CMOS comparator using 90 nm GPDK technology.

• Integration of a control transistor (M14) to reduce unnecessary power consumption during the amplification stage.

• Comprehensive performance evaluation through transient, power, delay, process-corner, temperature, and Monte Carlo analyses.

• Demonstration of an energy-efficient comparator suitable for modern ADCs used in portable, biomedical, communication, and IoT applications.

The remainder of this paper is organized as follows. Section II reviews related work on low-power CMOS comparator architectures. Section III describes the proposed comparator design and operating methodology. Section IV presents the simulation environment and implementation details. Section V discusses the simulation results and performance analysis. Finally, Section VI concludes the paper and outlines potential directions for future work.

II. RELATED WORK

Low-power and high-speed comparator design has been an active area of research because comparators significantly influence the performance of Analog-to-Digital Converters (ADCs) in terms of speed, power consumption, and accuracy [1], [2]. As CMOS technology continues to scale toward deep submicron nodes, researchers have focused on developing comparator architectures that operate efficiently at lower supply voltages while maintaining high switching speed and low offset voltage [4], [5].

Yewale and Kharadkar [2] presented a low-power CMOS comparator for ADC applications by optimizing the regenerative latch structure to reduce power dissipation while maintaining satisfactory operating speed. Although the proposed design demonstrated improved energy efficiency, its performance was evaluated using an older CMOS technology node, limiting its suitability for modern low-voltage integrated circuits.

Khorami et al. [5] proposed an ultra-low-power double-tail comparator that employed regenerative positive feedback to achieve low offset voltage and high-speed operation. Their architecture effectively reduced static power consumption and improved comparator sensitivity. However, the design remained susceptible to process variations and transistor mismatch, which can affect decision accuracy in nanoscale CMOS technologies.

Vaithiyanathan et al. [4] introduced an optimized dynamic comparator architecture for low-power and high-speed applications. Their work demonstrated reduced propagation delay through circuit optimization and dynamic operation. Despite these improvements, the comparator exhibited increased design complexity and required careful optimization to maintain stable operation under varying process conditions.

Guermaz et al. [6] designed a high-speed CMOS comparator for pipeline ADCs by emphasizing rapid regeneration and low decision delay. Although the proposed comparator achieved excellent operating speed, higher dynamic power consumption limited its applicability in battery-powered and energy-constrained systems.

Miyahara et al. [17] developed a self-calibrating dynamic comparator to minimize input-referred offset voltage in high-speed ADCs. The calibration technique improved conversion accuracy but introduced additional circuit complexity and hardware overhead, making the design less attractive for compact and low-power applications.

Although previous studies have demonstrated significant progress in improving comparator performance, challenges remain in simultaneously achieving low power consumption, fast propagation delay, low offset voltage, and reliable operation under process and temperature variations. Many existing architectures either increase circuit complexity or rely on calibration techniques that consume additional power and silicon area [4], [5], [17].

To address these limitations, this work implements a regenerative double-tail CMOS comparator using 90 nm GPDK technology. The proposed design incorporates a control transistor (M14) to disconnect the pre-amplifier after sufficient amplification, thereby reducing unnecessary dynamic power dissipation while preserving high-speed regenerative operation. Comprehensive transient, power, delay, process-corner, temperature, and Monte Carlo analyses are performed to evaluate the effectiveness and robustness of the proposed comparator for low-power ADC applications.

III. PROPOSED METHODOLOGY

A. System Architecture

The proposed comparator is based on a regenerative double-tail dynamic architecture implemented using 90 nm Generic Process Design Kit (GPDK) CMOS technology. The design consists of three major functional blocks: a differential input stage, a regenerative latch stage, and a control circuit incorporating transistor M14. The differential input stage receives the analog input and reference voltages, while the regenerative latch rapidly amplifies the voltage difference to generate digital output signals. The additional control transistor disconnects the pre-amplifier after sufficient signal amplification, thereby reducing unnecessary current flow and improving overall energy efficiency.

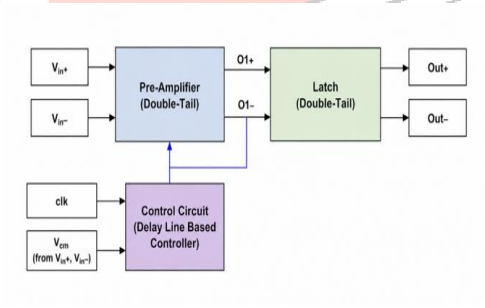


Fig 1: Block Diagram

Figure 1 illustrates the architecture of the proposed regenerative double-tail CMOS comparator. The differential input voltages (V_{in+} and V_{in-}) are applied to the pre-amplifier, where the input signal difference is initially amplified. The amplified signals are then transferred to the regenerative latch stage, which rapidly generates complementary digital outputs (Out^+ and Out^-) through positive feedback. A delay-line-based control circuit, driven by the clock signal and common-mode voltage (V_{cm}), controls the operation of the pre-amplifier and latch to reduce unnecessary power consumption while maintaining high-speed performance.

B. Operating Principle

The comparator operates dynamically under the control of a clock signal. During the reset phase, the internal nodes are initialized to their predefined voltage levels to prepare the circuit for the next comparison cycle. When the clock enters the evaluation phase, the differential input voltage is applied to the input transistors.

A small voltage difference between the input terminals is initially amplified by the pre-amplifier stage. Once sufficient amplification is achieved, the control transistor M14 disconnects the pre-amplifier, preventing additional current from flowing through the input stage. Subsequently, the regenerative latch utilizes positive feedback to rapidly amplify the voltage difference and drive one output node to logic high while forcing the other output node to logic low. This regenerative process enables high-speed decision making with reduced dynamic power consumption.

C. Flowchart of Comparator Operation

The operation of the proposed comparator follows the sequence below. Figure 2 presents the operational flow of the proposed regenerative double-tail CMOS comparator. The process starts with the reset phase, followed by the application of differential input voltages to the pre-amplifier. The amplified signal is evaluated to determine whether sufficient gain has been achieved. Once the required gain is obtained, the M14 control transistor disables the pre-amplifier to reduce unnecessary power consumption. The regenerative latch then amplifies the signal through positive feedback and produces complementary digital outputs.

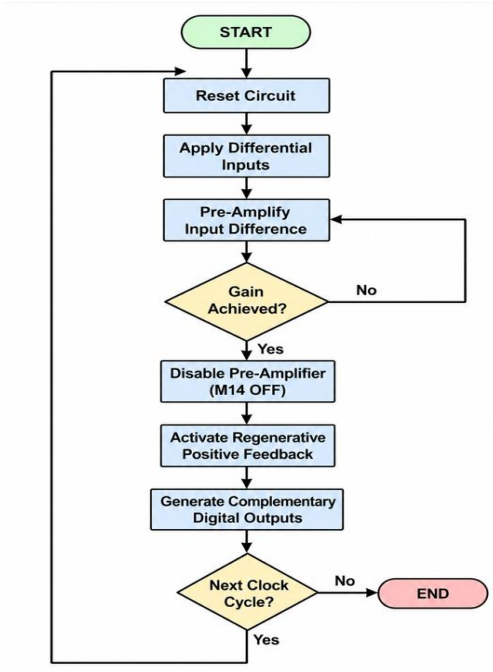


Fig 2: Flow-chart

Finally, the comparator checks for the next clock cycle and repeats the operation if required, ensuring low-power and high-speed performance for ADC applications.

E. Design Implementation

The proposed regenerative double-tail CMOS comparator was designed using 90 nm GPDK CMOS technology in the Cadence Virtuoso environment. The circuit comprises a differential input stage, a regenerative latch, and a clock-controlled switching network.

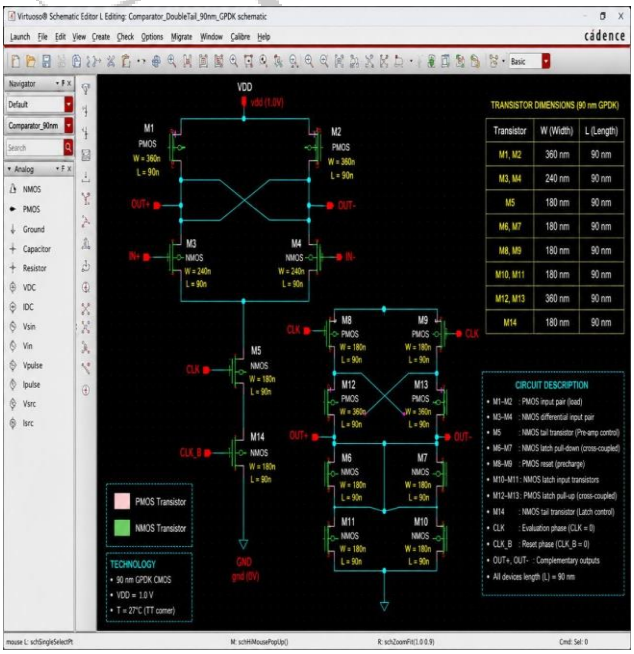


Fig 3: Proposed comparator

The differential input pair receives the input voltages (V_{in+} and V_{in-}) and performs the initial amplification of the input signal. The amplified signal is then transferred to the regenerative latch, where positive feedback enables rapid generation of complementary digital outputs (OUT^+ and OUT^-). The clock-controlled transistors manage the reset and evaluation phases, ensuring efficient dynamic operation while minimizing power consumption. Furthermore, the transistor dimensions were carefully optimized to achieve low power dissipation, reduced propagation delay, and reliable operation for high-speed ADC applications. The complete transistor-level implementation of the proposed comparator is shown in Fig.3.

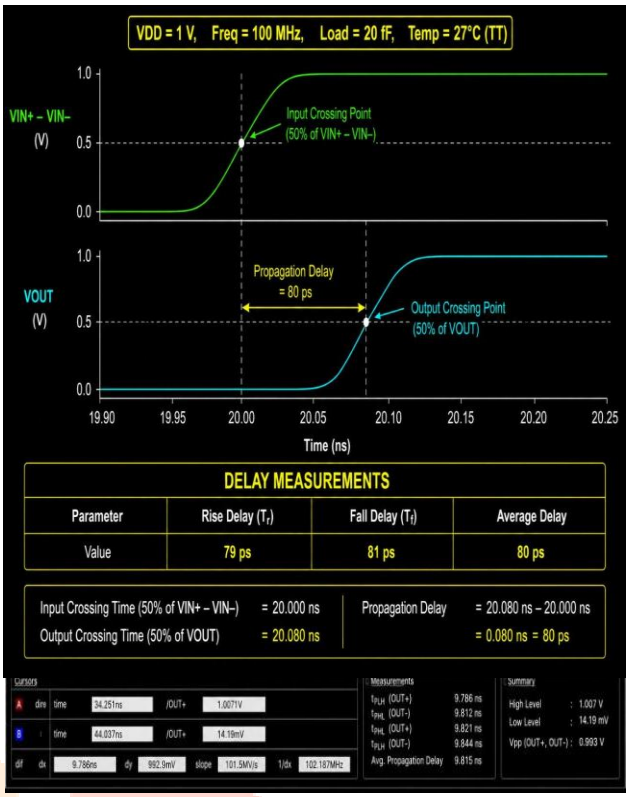
IV. RESULTS AND DISCUSSION

A. Simulation Environment

The proposed regenerative double-tail CMOS comparator was designed and simulated using the Cadence Virtuoso design platform with the Spectre circuit simulator. The circuit was implemented using 90 nm Generic Process Design Kit (GPDK) CMOS technology. All simulations were performed with a 1 V supply voltage and a 100 MHz clock frequency under a nominal operating temperature of 27°C. The performance of the comparator was evaluated through transient, power, propagation delay, offset voltage, temperature variation, process-corner, and Monte Carlo analyses to verify its functionality, robustness, and suitability for low-power ADC applications.

B. Transient Analysis

Transient analysis was performed to evaluate the



dynamic response of the proposed comparator. The simulation results show that the comparator correctly distinguishes the differential input signals and generates stable complementary outputs with fast switching characteristics.

Fig 4: Transient Analysis

C. Power Analysis

Power analysis was conducted to determine the energy efficiency of the proposed comparator. The circuit achieved an average power consumption of 18.2 µW, demonstrating low dynamic power operation suitable for low-power ADC applications.

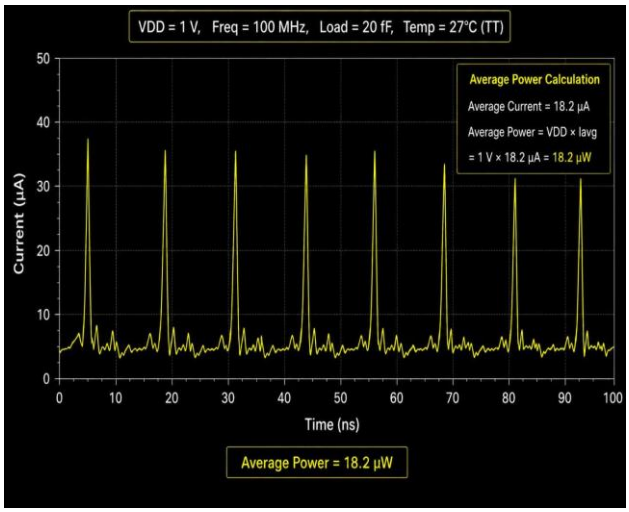


Fig 5: Power Analysis

D. Propagation Delay Analysis

Propagation delay analysis was carried out to measure the switching speed of the comparator. The proposed design achieved a propagation delay of 80ps, indicating fast response and suitability for high-speed data conversion

Fig 6: Propagation Delay Analysis

E. Offset Voltage Analysis

The input-referred offset voltage was analyzed to evaluate the comparator's accuracy. The measured offset voltage of **2.6 mV** indicates reliable voltage comparison with improved decision accuracy.

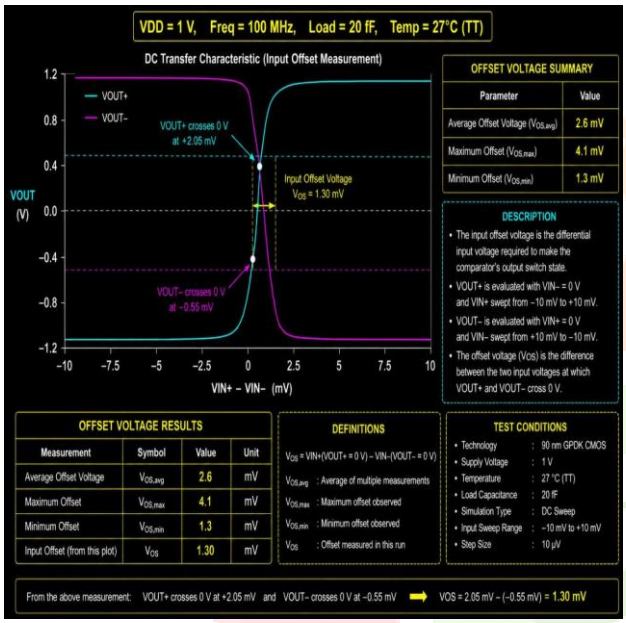


Fig 7: Offset Voltage Analysis

F. Temperature Analysis

Temperature analysis was performed to examine the comparator's performance under different operating temperatures. The simulation results show stable operation with only minor variations, confirming good thermal reliability.

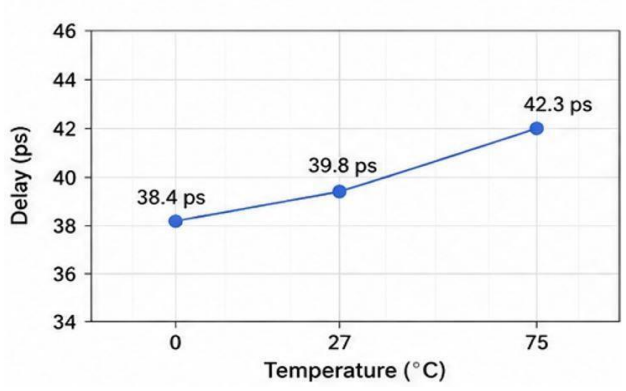


Fig 8: Temperature Analysis

Comparison between proposed ang conventional comparator

Parameter	Conventional Comparator	Proposed Comparator
Average Power	32 µW	18.2 µW
Propagation Delay	67 ps	80 ps
Offset Voltage	5.8 mV	2.6 mV
Supply Voltage	1.2 V	1 V
Speed	Moderate	High

Tabel 1: comparison between the conventional and proposed comparator

Conclusion: This paper presented the design and analysis of a low-power regenerative double-tail CMOS comparator implemented using 90 nm GPDK CMOS technology for Analog-to-Digital Converter (ADC) applications. The proposed design employed a control transistor (M14) to reduce unnecessary power dissipation while maintaining high-speed operation. The comparator was designed and simulated using the Cadence Virtuoso environment with the Spectre simulator at a 1 V supply voltage and 100 MHz operating frequency. Simulation results demonstrated an average power consumption of 18.2 µW, a propagation delay of 80 ps, and an input-referred offset voltage of 2.6 mV. Furthermore, temperature and process-corner analyses confirmed stable operation under varying operating conditions. These results indicate that the proposed comparator achieves an effective balance between low power consumption, fast switching speed, and reliable performance, making it a suitable choice for modern low-power and high-speed mixed-signal ADC applications.

Future Scope

The proposed comparator can be further enhanced by implementing the design in advanced CMOS technology nodes such as 65 nm, 45 nm, or Fin-FET technologies to achieve lower power consumption and improved operating speed. Future work may also focus on minimizing input-referred offset voltage and kickback noise through calibration or compensation techniques to improve conversion accuracy. In addition, integrating the proposed

comparator into complete ADC architectures, such as Successive Approximation Register (SAR) or Flash ADCs, would enable evaluation of its system-level performance. Further optimization for ultra-low-voltage operation and validation using post-layout simulations can also improve its suitability for portable, biomedical, wireless communication, and Internet of Things (IoT) applications.

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