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SAPON-BASED 4T2M SRAM CELL FOR ENERGY-EFFICIENT MEMORY APPLICATIONS

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Abstract—Static Random Access Memory (SRAM) plays a vital role in modern digital systems due to its fast data access and compatibility with high-performance processors. However, continuous CMOS technology scaling has increased leakage current and standby power consumption, limiting its suitability for low-power applications. This work proposes a SAPON-based 4T2M SRAM architecture that integrates four CMOS transistors with two memristors to improve energy efficiency while maintaining reliable memory functionality. The memristors provide non-volatile data storage, and the SAPON leakage reduction technique minimizes standby leakage current without affecting normal read and write operations. The proposed design is implemented and evaluated using the Cadence Virtuoso design environment with Spectre simulation. Simulation results demonstrate that the proposed SRAM cell reduces power consumption from 404 nW to 379 nW compared with a conventional 6T SRAM cell. Although the propagation delay increases from 10.06 ns to 15.13 ns, the architecture maintains correct functionality and offers improved energy efficiency, making it suitable for IoT devices, embedded systems, and other low-power VLSI applications.

Keywords: SRAM, 4T2M SRAM, Memristor, SAPON Technique, Leakage Power Reduction, Low-Power VLSI, Cadence Virtuoso, Spectre Simulation, IoT Applications.

I. INTRODUCTION

Static Random Access Memory (SRAM) is one of the most widely used memory technologies in modern digital systems because of its high operating speed, low access latency, and seamless integration with microprocessors. It is commonly employed as cache memory in processors, embedded controllers, communication systems, and Internet of Things (IoT) devices, where rapid data access is essential for overall system performance. The increasing demand for compact, energy-efficient, and high-performance electronic devices has made SRAM a fundamental component in contemporary very large-scale integration (VLSI) design. Despite its advantages, conventional CMOS-based SRAM faces several challenges as semiconductor technology continues to scale toward nanometer dimensions. The reduction in transistor size increases leakage current, process variations, and power density, which adversely affect memory reliability and energy efficiency. In particular, standby leakage power has become a major contributor to the total power consumption of SRAM arrays because cache memories remain idle for a significant portion of system operation. These issues are especially critical in battery-powered

systems, such as wearable devices, wireless sensor networks, portable medical equipment, and IoT applications, where minimizing energy consumption is a primary design objective.Leakage power has emerged as one of the most significant limitations in advanced CMOS technologies. As supply voltage and threshold voltage are reduced to improve performance, various leakage mechanisms, including subthreshold leakage and gate oxide leakage, become increasingly dominant. Consequently, conventional SRAM cells require continuous electrical power to preserve stored data, resulting in unnecessary energy dissipation during standby operation. Although several leakage reduction techniques have been proposed, many of them introduce additional design complexity or degrade circuit performance. Therefore, developing an SRAM architecture that effectively reduces leakage power while maintaining reliable operation remains an important research challenge. Emerging non-volatile memory technologies have attracted considerable attention as potential alternatives to conventional storage elements. Among these technologies, the memristor has gained significant interest because of its simple structure, programmable resistance states, excellent scalability, and ability to retain information even when the power supply is removed. Unlike traditional SRAM cells that depend entirely on transistor-based storage, memristors store data in the form of resistance levels, eliminating the need for continuous refresh power. Furthermore, memristors can be integrated with existing CMOS fabrication processes, enabling the development of compact hybrid memory architectures that combine the high-speed operation of CMOS transistors with the energy-efficient storage capability of non-volatile devices.To further improve power efficiency, this work incorporates the SAPON (Self-Adaptive Power Optimization Network) leakage reduction technique into the proposed memory architecture. The SAPON technique minimizes standby leakage current by suppressing unnecessary current paths during idle operation while allowing normal read and write operations to proceed without significant performance degradation. The combination of SAPON with memristor-based storage provides an effective approach for reducing static power consumption while preserving stable memory functionality. Motivated by the increasing need for low-power memory solutions in portable and embedded electronic systems, this paper proposes a SAPON-based 4T2M SRAM cell that combines four CMOS transistors with two memristors. The proposed hybrid architecture utilizes CMOS transistors for read and write operations, whereas the memristors provide non-volatile data storage with reduced standby power consumption. The architecture is designed using CMOS technology and evaluated through circuit-level simulation using the Cadence Virtuoso environment with the Spectre simulator. The major contribution of this work is the development and performance evaluation of a low-power hybrid SRAM architecture that integrates memristor technology with the `SAPON leakage reduction technique. Simulation results demonstrate that the proposed design reduces power consumption from 404 nW to 379 nW while maintaining reliable read and write functionality. Although a moderate increase in propagation delay is observed, the overall improvement in energy efficiency makes the proposed SRAM cell a promising candidate for future low-power VLSI systems, embedded memories, and IoT applications.

II. LITERATURE SURVEY

Static Random Access Memory (SRAM) has been the focus of extensive research due to its significant role in high-speed cache memories and embedded computing systems. As CMOS technology continues to scale, maintaining low power consumption, high stability, and reliable memory operation has become increasingly challenging. Oniciuc and Andrei investigated the influence of random dopant fluctuations on the static noise margin of conventional 6T SRAM cells and demonstrated that process variations can considerably affect memory reliability in nanoscale technologies **[1]**. Chua introduced the memristor as the fourth fundamental passive circuit element, establishing the theoretical basis for non-volatile memory devices capable of retaining data without continuous power supply [2]. This concept has motivated researchers to

investigate hybrid memory architectures that combine CMOS circuits with memristive devices to improve energy efficiency. Several researchers have proposed different SRAM architectures to reduce leakage power while maintaining stable read and write operations. Jadon and Akashe developed a hybrid CMOS–memristor 4T non-volatile SRAM cell that demonstrated the feasibility of combining memristors with CMOS technology to reduce standby power consumption while preserving memory functionality [3]. Similarly, Ho *et al.* introduced a memristive SRAM architecture consisting of seven transistors and one memristor, illustrating the advantages of non-volatile storage in reducing leakage current and improving power efficiency [9]. Sharif *et al.* further proposed a compact memory architecture based on four CMOS transistors and two memristors, highlighting the potential of hybrid memory structures for reducing hardware complexity while maintaining reliable operation [10]. These studies confirm that integrating memristors with CMOS technology provides an effective direction for developing next-generation low-power memory systems. Conventional CMOS SRAM optimization has also received considerable attention. Hamzaoglu *et al.* proposed dual-threshold voltage SRAM cells with single-ended bit-line sensing to improve cache performance while lowering power dissipation in deep-submicron technologies [5]. Banu and Gupta optimized a 6T SRAM cell using the Cadence Virtuoso environment by carefully selecting transistor dimensions to minimize standby leakage without affecting normal memory operation [6]. Murali Mohan Babu *et al.* compared multiple SRAM topologies by evaluating power consumption, propagation delay, and static noise margin, concluding that optimized transistor configurations can improve stability and reduce leakage current [8]. Likewise, Mittal and Tomar analyzed the performance of 6T, 7T, 8T, and 9T SRAM architectures, demonstrating that additional transistors enhance read/write reliability and memory stability but also increase silicon area and implementation complexity [7]. Recent research has also explored compact SRAM architectures for low-power Internet of Things (IoT) applications. Prasad *et al.* presented a 5T SRAM cell optimized for reduced silicon area and lower power consumption through statistical analysis of process variations and memory performance [4]. Although the proposed architecture achieved improvements in area efficiency and power reduction, it remained dependent on volatile CMOS storage and therefore required continuous standby power to preserve stored information. Overall, the existing literature demonstrates significant progress in SRAM design through transistor optimization, leakage reduction techniques, and hybrid memory structures. However, many reported architectures either remain fully CMOS-based or focus primarily on non-volatile storage without incorporating an effective standby leakage reduction mechanism. Motivated by these limitations, the proposed SAPON-based 4T2M SRAM architecture integrates four CMOS transistors with two memristors and employs the SAPON leakage reduction technique to minimize standby power while maintaining reliable read and write operations. This combination provides an energy-efficient solution suitable for low-power VLSI systems, embedded memories, and IoT applications.

III. METHODOLOGY

A. Functionality 6T SRAM Cell

The conventional six-transistor (6T) static random access memory (SRAM) cell is widely employed in cache memories because of its high operating speed, low access latency, and compatibility with CMOS technology. The memory cell consists of two cross-coupled CMOS inverters that form a bistable latch and two NMOS access transistors controlled by the word line (WL). The complementary bit lines (BL and $B\bar{L}$) are used to perform read and write operations. During a write operation, the desired logic value is applied to the bit lines while the word line is enabled, allowing the access transistors to transfer data to the internal storage nodes. During the read operation, the stored information is sensed through the bit lines without modifying the stored data. Although the 6T SRAM cell provides reliable functionality

and high-speed operation, it continuously consumes standby power because the stored data are maintained using CMOS feedback inverters. As CMOS technology scales into nanometer dimensions, leakage current becomes a major contributor to static power dissipation, making conventional SRAM less suitable for energy-constrained applications.

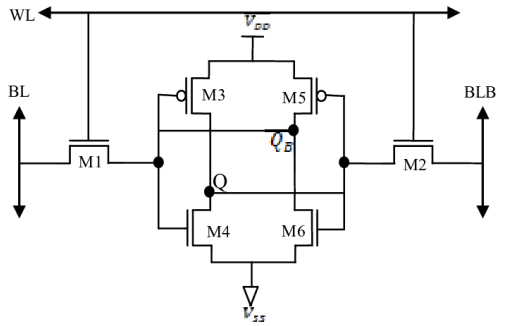

Fig. 1. Conventional 6T SRAM Cell

B. Proposed SAPON-Based 4T2M SRAM Cell

To overcome the limitations of conventional SRAM, a hybrid SAPON-based 4T2M SRAM architecture is proposed. The proposed memory cell combines four CMOS transistors and two memristors to achieve lower standby power while preserving reliable memory functionality. Unlike the conventional 6T SRAM, the proposed design replaces the pull-up PMOS transistors with memristive devices that store information in programmable resistance states.

The proposed cell consists of four NMOS transistors (T1–T4) and two memristors (M1 and M2). Transistors T1 and T2 function as access transistors controlled by the word line, connecting the storage nodes to the complementary bit lines during read and write operations.

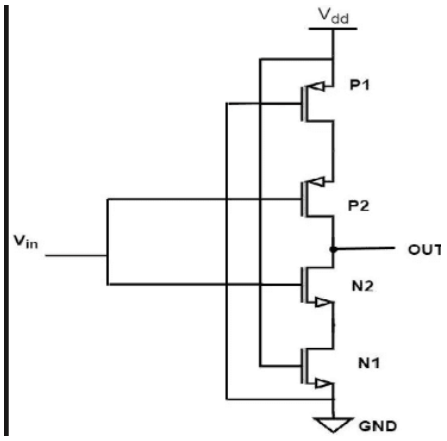

Fig. 2. Proposed SAPON-Based 4T2M SRAM Cell

Transistors T3 and T4 maintain the internal feedback path required for stable logic operation. The memristors are connected between the storage nodes and the power supply, replacing the conventional pull-up network. Depending on the stored logic value, each memristor is programmed into either a Low Resistance State (LRS) or a High Resistance State (HRS), enabling non-volatile data storage with significantly lower standby power.

The proposed architecture incorporates the SAPON (Self-Adaptive Power Optimization Network) leakage reduction technique to minimize static power consumption. During standby operation, SAPON suppresses unnecessary leakage current through the CMOS transistors while the memristors preserve the stored information without continuous power. This hybrid approach improves overall energy efficiency without affecting normal read and write operations.

C. Working principle

The proposed SRAM cell operates in three different modes: write, read, and standby. During the write operation, the word line is activated, enabling the access transistors. The input data applied to the complementary bit lines is transferred to the storage nodes, causing one memristor to switch to the low-resistance state while the other changes to the high-resistance state, according to the stored logic value. Once programming is completed, the word line is deactivated, isolating the memory cell from the bit lines. During the read operation, the word line is enabled again to connect the storage nodes to the bit lines. The stored logic value is detected by sensing the resistance states of the memristors through the access transistors without disturbing the stored data. This ensures reliable read functionality while maintaining data integrity. During standby mode, the word line remains disabled, disconnecting the memory cell from the bit lines. The memristors retain their programmed resistance states without requiring continuous electrical power. Simultaneously, the SAPON technique suppresses leakage current

through the CMOS transistors, resulting in a considerable reduction in static power dissipation.

D. SAPON Leakage Reduction Technique

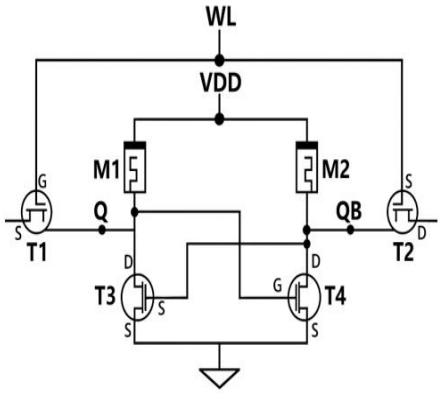

Fig. 3. Circuit Diagram of the Proposed SAPON-Based 4T2M SRAM Architecture

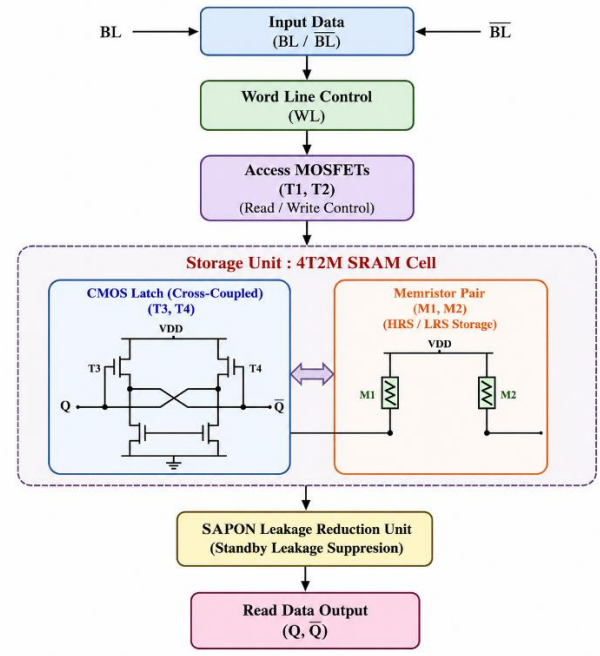

Fig. 4 Block Diagram of the Proposed SAPON-Based 4T2M SRAM Architecture

The SAPON leakage reduction technique is integrated into the proposed memory architecture to improve standby energy efficiency. In conventional CMOS SRAM cells, leakage current flows continuously through the transistor network even when the memory is idle, leading to unnecessary power loss. The SAPON approach minimizes these leakage paths during standby operation while preserving normal circuit functionality during active read and write operations. The combination of CMOS switching devices, memristive storage elements, and the SAPON technique provides an effective low-power memory solution. The memristors retain stored data without continuous bias voltage, whereas SAPON reduces leakage through inactive CMOS transistors. Consequently, the proposed architecture achieves improved energy efficiency while maintaining reliable memory operation. Simulation results demonstrate that the proposed SRAM architecture reduces power consumption from 404 nW to 379 nW. Although the propagation delay increases from 10.06 ns to 15.13 ns, the reduction in standby power and the addition of non-volatile storage make the proposed design highly suitable for low-power VLSI systems, embedded memories, Internet of Things (IoT) devices, wearable electronics, and portable computing applications.

RESULTS

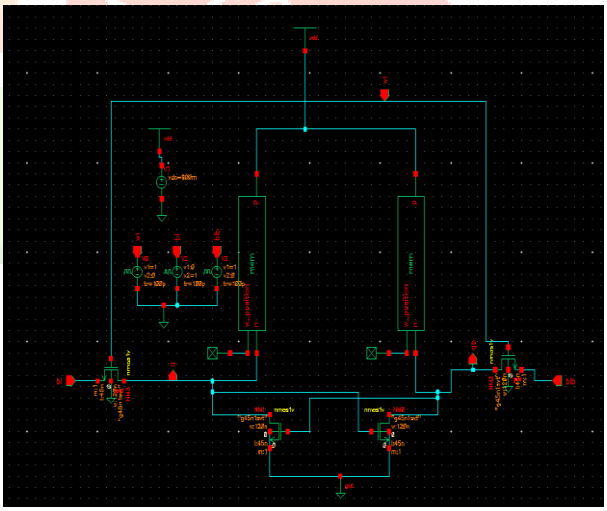

Fig. 5.1. Proposed architecture of a level shifter using 45 nm technology

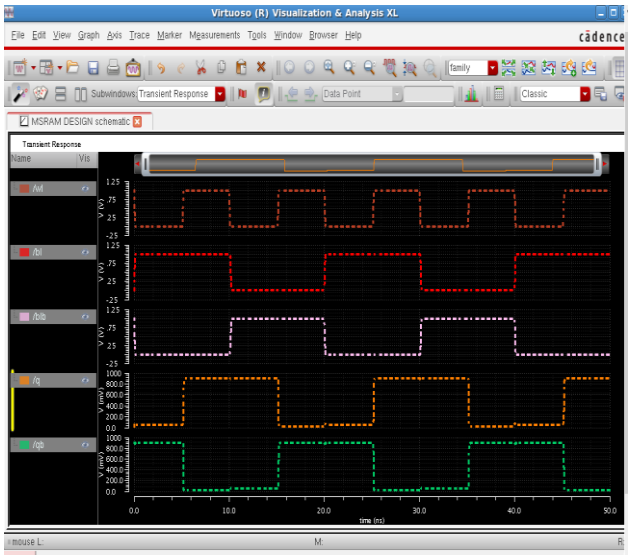

Fig 5.1.2: output waveforms

The transient simulation results confirm that the proposed SAPON-based 4T2M SRAM cell performs correct read and write operations, with all output waveforms accurately following the applied input signals. The obtained waveforms demonstrate stable switching behavior and reliable memory functionality while maintaining low-power operation.

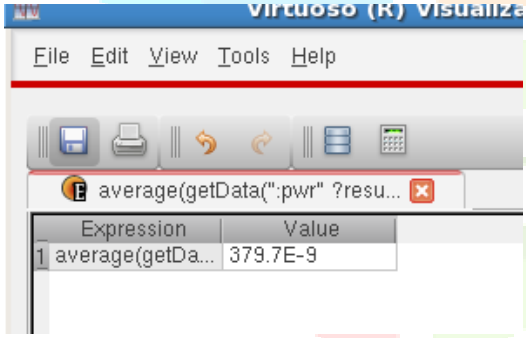

Fig. 5.1.3: Power Consumption

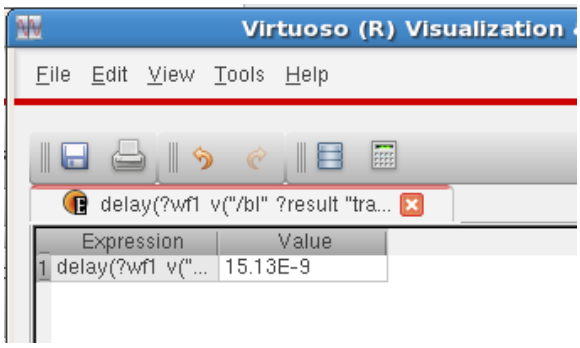

Fig 5.1.4: Dela

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net24


Circuit inventory:
                 nodes 12
                 bsim4 4
       bsource_b538d7 4
             Memristor 2
               vsource 4
```

Fig. 5.1.5: Mos count

Comparison Table

	Base	Extension
MOS count	**6**	**8**
Delay(ns)	**10.06**	**15.13**
Power(nw)	**404**	**378**

Table1: comparison table of base and extension.

VI. CONCLUSION

The proposed SAPON-based 4T2M SRAM architecture integrates CMOS transistors with memristor technology to achieve an energy-efficient memory design for low-power VLSI applications. The incorporation of the SAPON technique effectively reduces standby leakage power while preserving reliable read and write operations. Simulation results obtained using Cadence Virtuoso show that the proposed design decreases power consumption from 404 nW to 378 nW compared with the conventional 6T SRAM cell. Although the propagation delay increases from 10.06 ns to 15.13 ns, the architecture maintains stable memory functionality. The hybrid design provides an effective balance between low power consumption and reliable performance through the use of non-volatile memristive storage. Therefore, the proposed SRAM cell is a promising solution for IoT devices, embedded memories, portable electronics, and future energy-efficient VLSI systems

VII. FUTURE SCOPE

The proposed SAPON-based 4T2M SRAM architecture can be further enhanced by optimizing the read and write operations to reduce delay while maintaining low power consumption. Future research may investigate the implementation of the design using advanced CMOS technology nodes and emerging device structures to improve scalability, speed, and energy efficiency. The proposed memory cell can also be extended to large-scale SRAM arrays and cache memory systems to evaluate its performance in practical computing environments. In addition, comprehensive reliability studies under process variations, temperature fluctuations, and device aging conditions can be carried out to ensure stable operation. The integration of advanced leakage reduction methods, adaptive power management techniques, and error correction mechanisms may further improve the overall performance and reliability of the memory architecture. Owing to its hybrid CMOS–memristor structure and reduced standby power, the proposed design has significant potential for future applications in low-power embedded systems, Internet of Things (IoT) devices, edge computing platforms, and energy-efficient artificial intelligence hardware, making it a promising solution for next-generation memory technologies.

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