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VEDIC FUSED FLOATING POINT MULTIPLIER DESIGN USING ADAPTIVE HOLD LOGIC AND RAZOR FLIPFLOP IN FPGA TECHNOLOGY

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Abstract

Digital Signal Processing (DSP) applications demand high-speed and energy-efficient arithmetic units, particularly for multiplication-intensive operations such as Fast Fourier Transform (FFT) and Discrete Cosine Transform (DCT). Conventional multiplier architectures often suffer from increased delay, power consumption, and hardware complexity. This work presents an optimized design of a floating-point fused dot product (FDP) unit using a Vedic multiplier integrated with Adaptive Hold Logic (AHL) and Razor flip-flops. The proposed architecture is implemented on an FPGA platform and evaluated in terms of delay, power, and area. Results demonstrate a significant reduction in latency and hardware utilization compared to conventional designs, making the proposed system suitable for modern high-performance DSP applications.

1. Introduction

Multiplication is a fundamental operation in digital systems, especially in DSP applications such as filtering, transformation, and signal analysis. However, traditional multiplier architectures introduce substantial delay and consume significant hardware resources, which can degrade overall system performance.

To address these limitations, modern design approaches focus on optimizing speed, power, and area simultaneously. Techniques such as Modified Booth encoding and Wallace tree structures have been widely used to improve multiplication efficiency. However, increasing parallelism often leads to higher complexity, routing overhead, and power consumption.

This paper proposes an efficient multiplier design that integrates:

- **Vedic multiplication technique**
- **Adaptive Hold Logic (AHL)**
- **Razor flip-flop for error detection**

The objective is to achieve high performance with reduced latency and improved energy efficiency.

2. Background and Related Work

2.1 VLSI Design Challenges

As VLSI technology advances, circuits operate at higher speeds and smaller geometries. This introduces several challenges:

- Signal propagation delay becomes critical
- Power consumption increases with frequency
- Heat dissipation becomes difficult
- Circuit reliability decreases due to aging effects

These challenges necessitate innovative design techniques that balance performance and efficiency.

2.2 Hardware Description Languages

Traditional programming languages are not suitable for hardware modeling due to their sequential execution nature. Digital systems operate in parallel, requiring specialized languages like VHDL and Verilog.

VHDL enables:

- Structural and behavioral modeling
- Simulation and synthesis
- Parallel execution representation

2.3 FPGA Technology

Field-Programmable Gate Arrays (FPGAs) provide flexibility by allowing post-manufacturing configuration. They consist of:

- Configurable Logic Blocks (CLBs)
- Programmable interconnections
- Embedded resources (memory, DSP blocks)

Although slower than ASICs, FPGAs are widely used due to:

- Reduced development time
- Reconfigurability

- Lower design cost

2.4 Existing Systems

Floating-point Fused Multiply-Add (FMA) units are commonly used in DSP systems to reduce computation time. However:

- They consume high area and power
- Parallel implementations increase complexity
- Serial implementations reduce speed

The fused dot product operation:

$Y=A\times B+C\times D$ $Y=A\times B+C\times D$

is widely used but inefficient in traditional architectures due to multiple rounding and intermediate steps.

3. Proposed System

3.1 Overview

The proposed system introduces a **fused dot product unit** using:

- Vedic multiplier
- Adaptive Hold Logic (AHL)
- Razor flip-flops

This design aims to:

- Reduce latency
- Improve throughput
- Minimize hardware usage

3.2 Vedic Multiplier

The Vedic multiplier is based on the **Urdhva-Tiryagbhyam (Vertical and Crosswise)** method.

Key advantages:

- Faster computation
- Reduced partial products
- Regular structure

A hierarchical design approach is used:

- 2×2 → 4×4 → 8×8 → 16×16 multiplier

This reduces complexity and improves scalability.

3.3 Razor Flip-Flop

Razor flip-flops detect timing errors caused by critical path delays.

Components:

- Main flip-flop
- Shadow latch
- XOR comparator
- Multiplexer

Function:

- Detect incorrect outputs
- Trigger re-execution when needed

This improves reliability without significantly increasing overhead.

3.4 Adaptive Hold Logic (AHL)

AHL dynamically adjusts system operation based on circuit conditions.

Features:

- Monitors timing violations
- Detects aging effects
- Adjusts execution cycles

Benefits:

- Maintains performance over time
- Reduces unnecessary delays
- Enhances system stability

3.5 Proposed Architecture

The architecture includes:

- Vedic multiplier core
- Razor flip-flops for error detection
- AHL for adaptive control

This combination enables:

- Variable latency operation
- Efficient resource utilization
- Improved performance under varying conditions

4. Implementation and Tools

The design is implemented using:

- **Verilog HDL**
- **Xilinx ISE Design Suite**
- **ModelSim Simulator**

Simulation Steps

1. Design entry
2. Compilation
3. Simulation
4. Debugging
5. Performance analysis

ModelSim provides:

- Waveform analysis
- Debugging tools
- Multi-language support

5. Results and Discussion

Performance Comparison

Parameter	Existing FDP	Proposed System
Slice Registers	684	346
LUTs	2448	1250
Occupied Slices	846	526
Delay (ns)	35.587	2.168
Power (mW)	15	50

Analysis

- **Delay Reduction:** Significant improvement (~90%)
- **Area Efficiency:** Nearly 50% reduction in resources
- **Power Trade-off:** Slight increase due to additional logic

Overall, the proposed system achieves:

✓ Higher speed

✓ Lower hardware usage

✓ Better scalability

6. Applications

The proposed design is suitable for:

- FFT and DCT processing
- Image and video processing
- Wireless communication systems
- Real-time DSP applications

7. Conclusion

This paper presents an optimized FPGA-based design of a floating-point fused dot product unit using a Vedic multiplier integrated with Adaptive Hold Logic and Razor flip-flops. The proposed system significantly reduces delay and hardware utilization compared to conventional approaches.

Future work may focus on:

- Power optimization
- ASIC implementation
- Higher precision designs