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Design And Analysis Of 7t Sram Cell Using Swing Restoration Inverter For Low Power Apllications

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ABSTRACT

In this paper, SRAM cell topologies have been implemented on 22nm technology node with Tanner tool. Read power and write power dissipation, read delay, write delay, of all considered topologies have been determined out. Read and write actions of each SRAM cells have also been examined. Static Random Access Memory (SRAM) is a memory that is designed to provide high speed and low power applications. As the technology is shrinking down, the power supply is also scaled down which decreases the noise margin of the SRAM cells. The reduced noise margin further makes more leakage power in the SRAM cells. The main objective of this project is to deal with the power dissipation which occurs normally in the conventional Static Random Access Memory (SRAM) cells during the read and write operation. This problem can be solved by applying dual-threshold-voltage for 7T SRAM Cells. The respective power dissipation and delay of these cells are calculated and compared.

1. INTRODUCTION

In last four decades Moore's law has promptly improving VLSI design act through CMOS technology scaling. Usually at every 18 to 24 months in an integrated circuit the number of transistor becomes double. This trend of technology scaling has worked very aggressively in semiconductor industry but in recent past years the pace of this scaling has been slowing down. Dynamic Power and static power drastically reduces due to scaling of supply voltage. Lowering the supply voltage increases the delay so to maintain the drive current the threshold voltage VTH must be decreases in same proportion. For the designing of SRAMs minimum feature size matters but CMOS technology scaling increases severe constraints these includes process variations, transistor degradation due to ageing. MOSFET based memory concept was commercialized in seventies. The first DRAM chip with 2k- bits was commercialized in year 1971 but the DRAM working does not matched with the working of processor because DRAM is more power hungry and its access time is also long.

The DRAM nature is dynamic so it needs that the memory should be refresh periodically for not to lose the data of memory cells. The processor required a new type of memory referred to as "cache memory" to keep frequently used data and in faster on chip memory. SRAMs matched with the

performance of processors but it has less storage capacity due to limited area and its cost also high. A wide range of Micro- electronics, multimedia and System on Chip applications, SRAMs continue to be a crucial component. To meet the performance requirement SoC applications and processors demands more on chip memory. Now a days, SRAM is universally used memory technology. Low power, fast access SRAM is very much needed for system on chip (SoC) technologies.

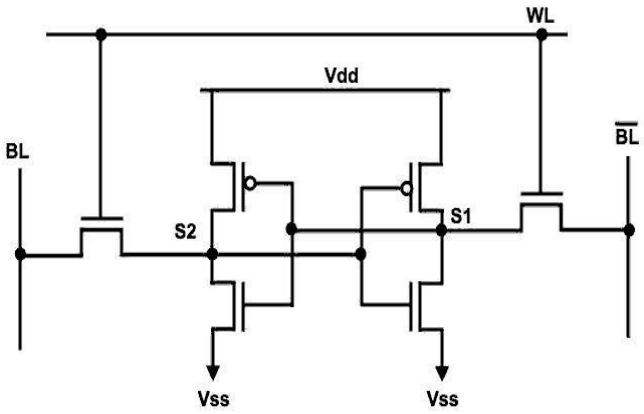

Figure 1: 6T SRAM CELL

When the dimensions of features in a cell are very small, its stability can be greatly affected. This paper introduces a specific configuration of a seven-transistor (7T) SRAM cell which aims to examine the transistor sizes for optimal power efficiency. In addition to this, new techniques for pre-charging and balancing the bit line during writing operations in the 7T SRAM cell are proposed to maximize power savings while the cell is in standby mode within an SRAM array. The results of CADENCE simulations support the effectiveness of the suggested approach, showing a significant 45% reduction in power consumption. These findings highlight the potential for improving power efficiency in SRAM technology through innovative design strategies.

2. A STRANDARD 6T SRAM CELL CIRCIUT ON TANNER

Proposed 6T cell introduced along with optimal transistor sizing method.

- Effect of process variation on power consumption and stability and examined. 7TSRAM cell shows high tolerance to process variations.

Write amplifier used to pre-charge bit lines after write operation in traditional 6T SRAM cell design 6T SRAM utilizes 6 transistors to store a single bit of data. 2 cross coupled inverters and 2 access transistors make up the 6T SRAM cell Both bit lines return to high state after write operation.

3. 6T SRAM's DISADVANTAGES

6T SRAM cell is larger in size and consumes more power compared to resistive load SRAMs. Cell is prone to sensitivity to noise and soft errors due to high resistances. The 6T SRAM cell is less efficient and more susceptible to errors compared to resistive load SRAMs.

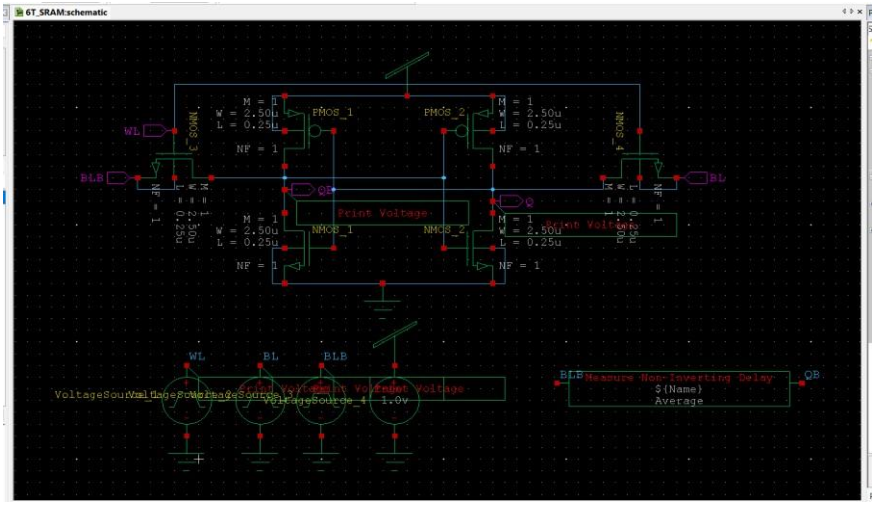

Fig 2: Standard 6T SRAM on TANNER

4. PROPOSED 7T SRAM CELL CIRCUIT ON TANNER :

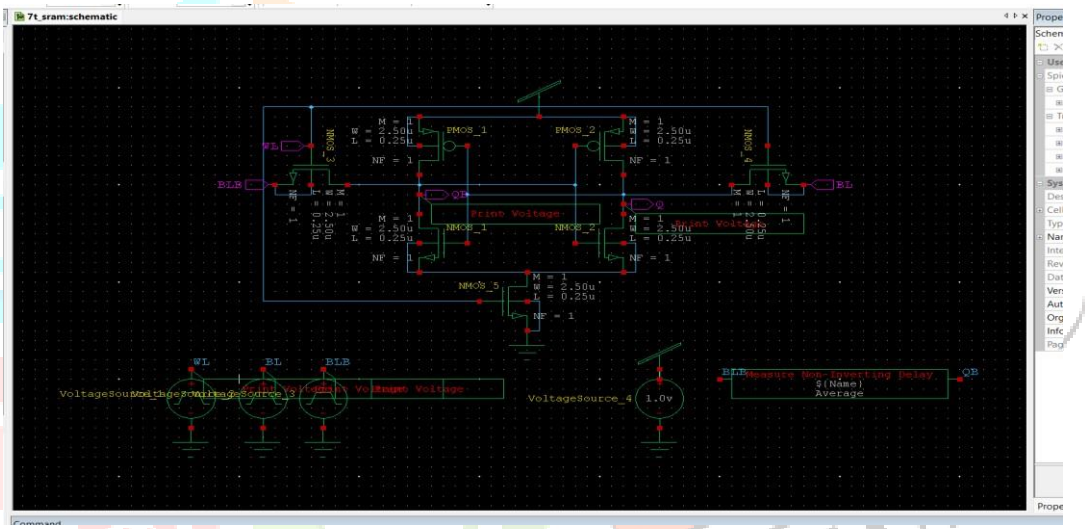

Fig 3: Implemented 7T SRAM using TANNER

The (seven transistor) 7T SRAM circuit is made up of 2 CMOS cross-coupled transistors. An additional NMOS transistor is connected to write line, along with two pass NMOS transistors connected to the bit and bit bar lines. Access transistors N3&N4 are connected to write and read lines for writing and reading operations. The 7T SRAM cell utilizes a feedback connection prior to the write process. The activation or deactivation of feedback connections can be achieved using the N5 transistor. The 7T SRAM circuit includes additional transistors for writing and reading operations, as well as a feedback connection controlled by the N5 transistor.

4.1 Write Operation

Initiating the write operation involves deactivating the N5 transistor to disconnect feedback connection. Activating N3 and deactivating N4 results in the bit line bar carrying the opposite of input data. Activating N5 and deactivating WL establishes a new feedback connection for storing fresh data. Resetting the bit line bar to "0" enables storage of "1" in the cell. No discharge of the bit line is required for storing "0" in the cell.

Summary: The process involves manipulating transistors to write and store data efficiently in the cell.

4.2 Read Operation:

During read operation, both read and word lines are activated. Transistor N5 remains active during read operation.

Traditional (six transistor) 6T SRAM cell array & newly proposed 7T SRAM cell array was simulated Innovative 7T SRAM array shows 45% reduction on power consumption. Power usage variation in seven transistor SRAM cell is lower than in 6T SRAM cell Output waveforms of 6T and 7T SRAM circuits shown in respective figures. Findings suggest efficiency improvements in 7T SRAM technology

4.3 ADAVANTAGES IN 7T S-RAM

- The 7T S-RAM cell is stable during
- The 7T SRAM has adequate static noise
- The cell consists of 7 transistors
- Only a single bit-line, word-line & read line are utilized
- While writing to the memory BL & WL are active
- RL remains inactive during writing
- The seven transistor S-RAM cell operates efficiently

The 7T SRAM cell is a stable and efficient memory cell with 7 transistors and specific control lines for reading and writing.

5. RESULTS AND ANALYSIS

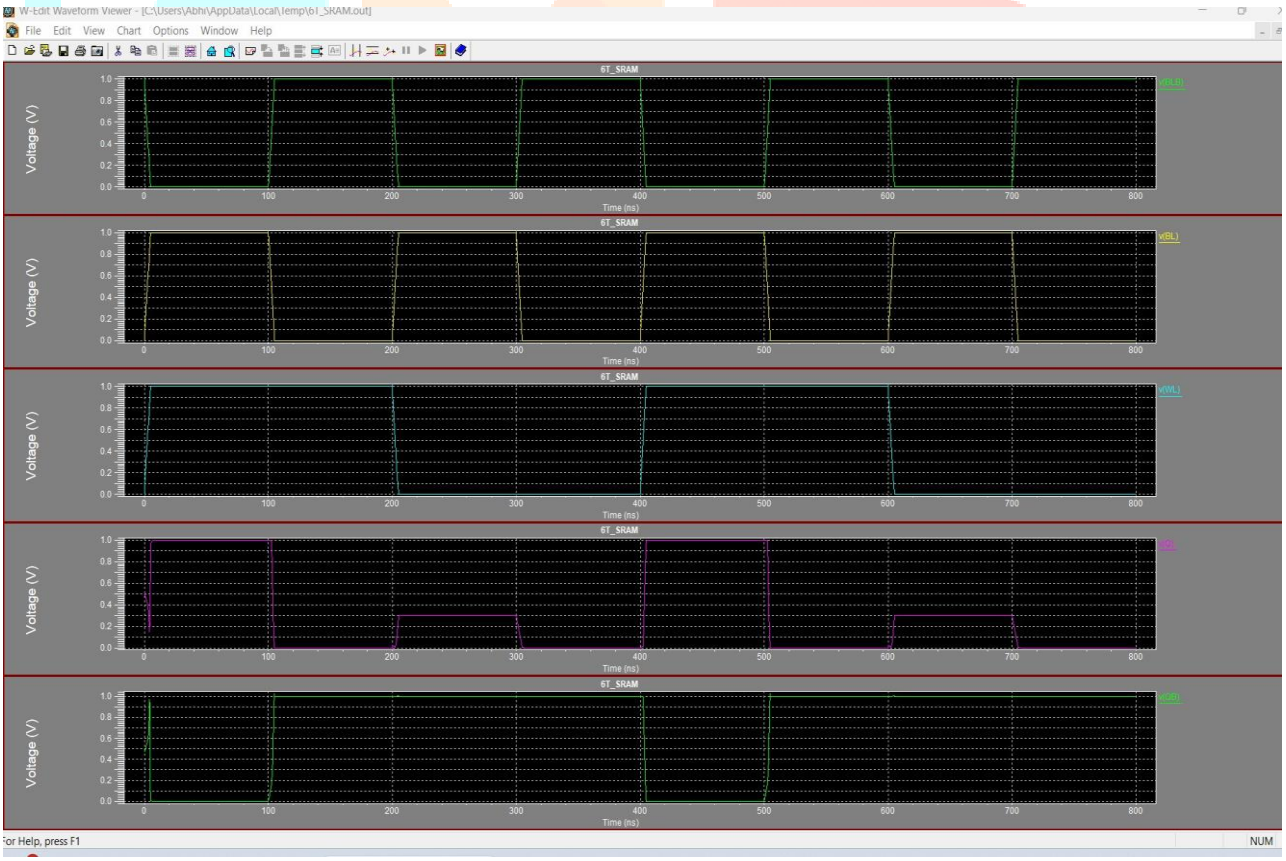

Fig 4:6T SRAM read/write operation timing diagram

```
 7.000000e-007   9.9994e-001   3.0098e-001   0.0000e+000   1.0000e+000   2.6470e-015
 7.050000e-007   1.0002e+000   8.7672e-004   0.0000e+000   7.9936e-015   1.0000e+000
 7.075000e-007   9.9999e-001   9.3940e-006   0.0000e+000   0.0000e+000   1.0000e+000
 7.324999e-007   1.0000e+000   4.8114e-007   0.0000e+000   0.0000e+000   1.0000e+000
 8.000000e-007   1.0000e+000   4.5411e-007   0.0000e+000   0.0000e+000   1.0000e+000

* BEGIN NON-GRAPHICAL DATA

Power Results
vdd gnd from time 0 to 1e-006
Average power consumed -> 1.377556e-007 watts
Max power 5.468433e-005 at time 4.72004e-009
Min power 7.467301e-010 at time 4.54987e-007


* END NON-GRAPHICAL DATA


* BEGIN NON-GRAPHICAL DATA

MEASUREMENT RESULTS

TRAN_Measure_Delay_2 = 1.3097e-009

* END NON-GRAPHICAL DATA
*

* Parsing                    0.01 seconds
* Setup                      0.01 seconds
* DC operating point         0.00 seconds
* Transient Analysis         0.01 seconds
* Overhead                   0.65 seconds
* ------------------------------------------
* Total                      0.68 seconds

* Simulation completed

* End of T-Spice output file
```

Status Input Out Start Date Elap

Fig 5:Power and Delay Analysis from T-Spice Simulation

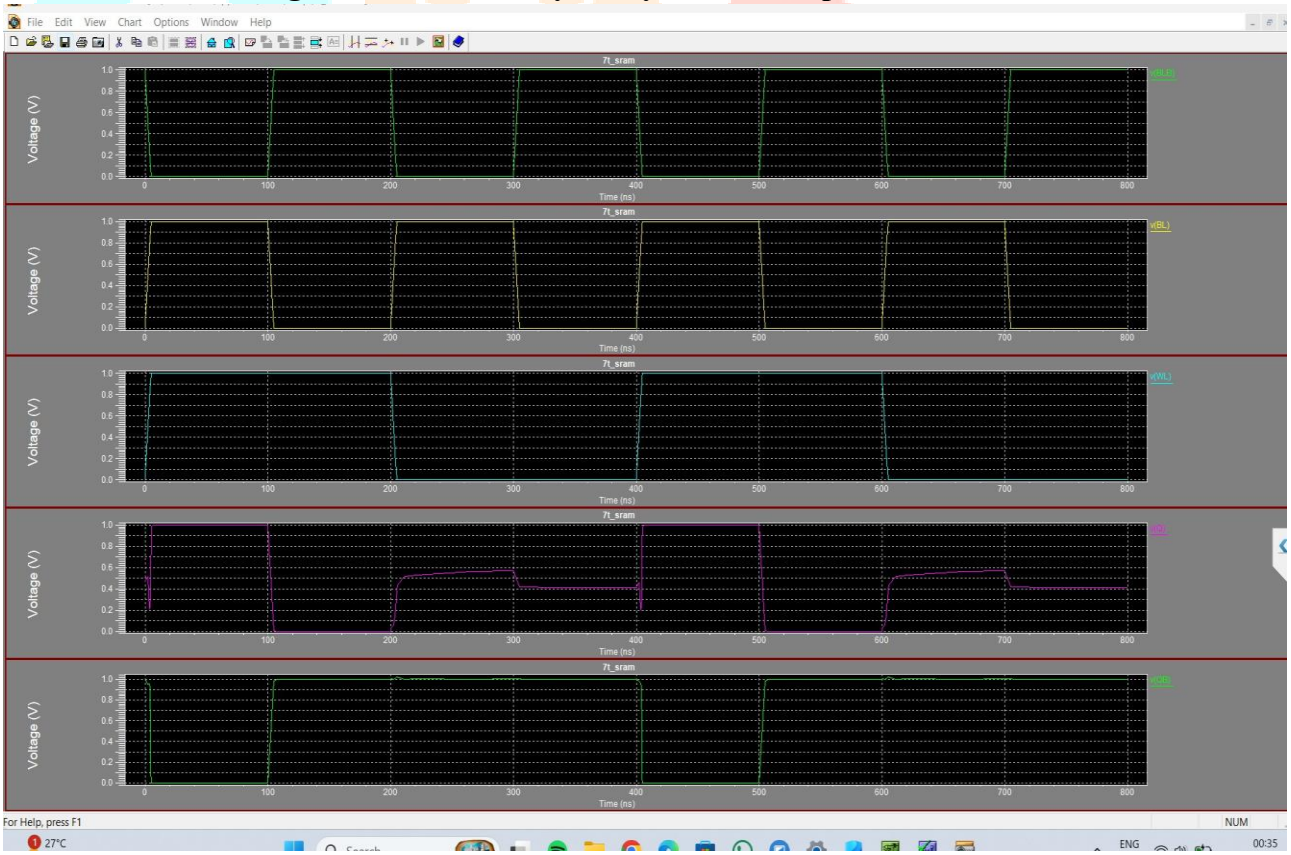

Fig 6:7T SRAM read/write operation timing diagram

```
6.063769e-007  1.0168e+000  4.4247e-001  0.0000e+000  1.0000e+000  0.0000e+000
6.109667e-007  9.9906e-001  5.1412e-001  0.0000e+000  1.0000e+000  0.0000e+000
6.210174e-007  1.0041e+000  5.3157e-001  0.0000e+000  1.0000e+000  0.0000e+000
6.661457e-007  9.9898e-001  5.6082e-001  0.0000e+000  1.0000e+000  0.0000e+000
7.000000e-007  1.0024e+000  5.7140e-001  0.0000e+000  1.0000e+000  2.6470e-015
7.050000e-007  1.0084e+000  4.1636e-001  0.0000e+000  7.9936e-015  1.0000e+000
7.075000e-007  1.0013e+000  4.1451e-001  0.0000e+000  0.0000e+000  1.0000e+000
7.324999e-007  1.0000e+000  4.1403e-001  0.0000e+000  0.0000e+000  1.0000e+000
8.000000e-007  9.9997e-001  4.1401e-001  0.0000e+000  0.0000e+000  1.0000e+000

* BEGIN NON-GRAPHICAL DATA

Power Results
vdd gnd from time 0 to 1e-006
Average power consumed -> 1.169487e-007 watts
Max power 5.882185e-005 at time 4.73502e-009
Min power 4.128846e-012 at time 0


* END NON-GRAPHICAL DATA


* BEGIN NON-GRAPHICAL DATA

MEASUREMENT RESULTS

TRAN_Measure_Delay_2 = 4.4859e-010

* END NON-GRAPHICAL DATA
*

* Parsing                    0.01 seconds
* Setup                      0.00 seconds
* DC operating point         0.01 seconds
* Transient Analysis         0.01 seconds
* Overhead                   1.36 seconds
* ------------------------------------------
* Total                      1.39 seconds
```

Status	Input ...	Out...	Start Date...	Elap...
finished	7t_s...	7t...	March 3...	00:...

Fig 7:Power and Delay Analysis from T-Spice Simulation

5.1 COMPARISON OF PARAMETERS OF 6T AND 7T SRAM CELLS:

Parameter	6T SRAM CELL	PROPOSED 7T SRAM CELL
Average power	1.377556×10^{-7} W	1.169487×10^{-7} W
Maximum Power	5.468433×10^{-5} W	5.882185×10^{-5} W
Time of Max Power	4.72004 ns	4.73502 ns
Minimum Power	7.467301×10^{-10} W	4.128846×10^{-12} W
Time of Min Power	454.987 ns	0 ns
Propagation delay	1.3097 ns	0.44859 ns
Total simulation Time	0.68 sec	1.39 sec

6. CONCLUSION

According to simulation results, compared to conventional 6T SRAM, the suggested 7T SRAM cell-based array uses less power.

Under typical process conditions and power savings are realized. The impact of process modifications on stability and power consumption is evaluated through analysis utilizing the CADENCE tool. The 7T SRAM array's proposed write circuitry architecture improves power efficiency. A study illustrates the possible advantages of using 7T SRAM technology in memory arrays. For a thorough examination of process changes in SRAM arrays, the CADENCE Tool is employed. technological developments in SRAM design to maximize stability and power economy. In comparison to conventional 6T SRAM,

simulation and analysis demonstrate enhanced power efficiency and stability in 7T SRAM cell-based arrays.

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