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FPGA-BASED UART COMMUNICATION SYSTEM USING TANG NANO 9K

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Abstract: Universal Asynchronous Receiver Transmitter (UART) is one of the most widely used serial communication protocols for reliable, low-cost, and low-pin-count data transfer. Unlike parallel communication, UART transmits data serially, reducing design complexity and improving overall efficiency. In this project, a UART module is implemented on the Tang Nano FPGA platform. The design includes the essential components of UART—baud rate generator, transmitter, and receiver. Data transmitted from the FPGA is received and monitored using the PuTTY serial terminal. The implementation demonstrates accurate serial communication, stable baud rate operation, and successful real-time data transfer between the FPGA and a PC. This work highlights the flexibility and capability of FPGA-based SoC development for embedded communication applications.

Index Terms - UART, FPGA, Tang Nano 9K, Verilog HDL, PuTTY serial Terminal, Serial Communication, Gowin IDE, Baud Rate Generator.

I. INTRODUCTION

Asynchronous serial communication remains a cornerstone of embedded systems, prized for its minimal wiring requirements, simplicity, and flexible timing. The UART protocol, which manages this communication, performs critical parallel-to-serial and serial-to-parallel data conversion. It ensures synchronization through the use of start bits, stop bits, and, optionally, parity bits, all without a shared clock signal between the communicating devices.

Field-Programmable Gate Arrays (FPGAs) offer an ideal platform for UART implementation. Their reconfigurable logic fabric allows for custom, highly optimized digital circuits, while their inherent parallelism enables the design of multi-channel UART cores or the seamless integration of other system components on a single chip. The Tang Nano 9K FPGA, built around Gowin's GW1NR-9 device, provides ample logic resources (8,640 LUTs), embedded Block RAMs (BSRAM), Phase-Locked Loops (PLLs), and low-power operation. Implementing a UART on this platform offers superior flexibility compared to fixed-hardware UARTs in microcontrollers, enabling features like custom baud-rate generation, advanced error checking, and dynamic protocol modification.

This project leverages these advantages to create a robust UART system, serving as a core communication hub for interfacing with common input and output peripherals.

II. LITERATURE REVIEW

The implementation of UART on FPGAs is a well-explored domain, with numerous studies contributing to its refinement.

Naresh and Patel [1] proposed a VHDL-based UART with integrated status registers, providing a reliable mechanism for monitoring transmission and reception states.

Yi-yuan and Xue-jun [2] focused on the simulation and validation of UART modules using VHDL, highlighting the importance of pre-synthesis verification to ensure design correctness.

Liu et al. [3] developed a high-performance embedded UART, prioritizing throughput optimization for data-intensive applications.

Laddha and Thakare [4] designed a configurable baud-rate UART, allowing dynamic adjustment of communication speeds to suit different peripheral requirements. For industrial-grade robustness.

Saha et al. [5] implemented a Built-In Self-Test (BIST) embedded RS-422 UART on an FPGA, focusing on fault tolerance in harsh environments.

Our work builds upon these foundations by implementing a Verilog-based UART on the modern, cost-effective Tang Nano 9K platform. It synthesizes concepts of reliability (inspired by [1,5]), verification (following [2]), and configurability (from [4]) into a single, practical system demonstration with multiple peripherals.

III. OBJECTIVES

The primary objective of this work is to design, implement, and validate a robust UART (Universal Asynchronous Receiver and Transmitter) communication system on the Tang Nano FPGA platform using Verilog HDL. The study focuses on developing an efficient UART architecture that adheres to standard serial communication protocols while ensuring reliability, portability, and real-time operability.

The specific objectives of this research are as follows:

Design and implement a reliable UART communication system on the Tang Nano FPGA

This includes developing a fully synthesizable UART subsystem capable of stable asynchronous serial communication. The design aims to achieve accurate data framing, clock recovery, parity generation, and error detection while ensuring compatibility with standard UART timing requirements.

Develop UART transmitter and receiver modules following standard UART protocol specifications

The work involves designing modular TX and RX components in Verilog, covering essential protocol aspects such as start/stop bit generation, baud-rate control, sampling logic, and buffering. The modules are created with parameterizable features to support different configurations and baud rates.

Interface the UART-enabled FPGA system with a personal computer (PC) and validate data transfer using the PuTTY serial terminal.

The implemented UART module is integrated with USB-to-UART hardware to establish communication with a PC. Data transmission and reception are validated through serial terminal software (PuTTY), enabling real-time observation and debugging of FPGA-to-PC communication.

The design is tested under different baud-rate configurations to analyze timing accuracy, data integrity, and stability. Performance metrics including throughput, bit-error behavior, and synchronization reliability are assessed to ensure compliance with UART protocol standards.

Verify the UART functionality through simulation, hardware testing, and serial terminal monitoring

Comprehensive verification is conducted through ModelSim simulations, FPGA implementation testing, and live serial terminal analysis. This objective ensures that the UART system functions correctly across both simulated and real hardware environments, demonstrating the overall robustness of the design.

IV. DETAILED METHODOLOGY & SYSTEM DESIGn

The proposed system is constructed as a set of interconnected modules, as shown in the block diagram below.

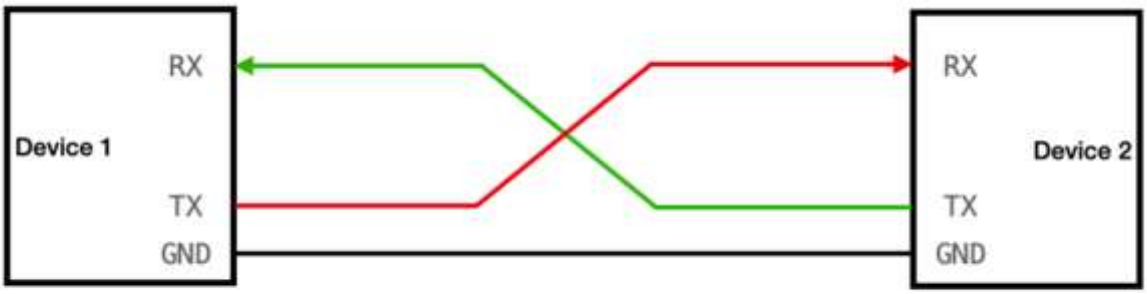

Fig 1: Block Diagram

This work implements a complete UART-based communication system on the Tang Nano FPGA platform using synthesizable Verilog HDL. The methodology integrates modular RTL design, finite-state-machine (FSM) control, deterministic timing generation, and hardware validation using a serial terminal. The objective is to provide a reliable, low-resource UART subsystem capable of transmitting, receiving, and echoing data in real time.

The overall UART subsystem consists of three interconnected RTL modules:

UART Transmitter (uart_tx) – Converts 8-bit parallel data into serial UART format.

UART Receiver (uart_rx) – Samples and reconstructs serial data at the correct bit boundaries.

Top-Level Controller (uart_test) – Coordinates message transmission, loopback functionality, and peripheral LED monitoring.

All modules operate on the system clock (27 MHz) and communicate using ready/valid handshake signals to ensure lossless data flow.

Baud Timing and Clock Cycle Derivation

Precise baud timing is generated inside both TX and RX modules using a cycle-counting approach. For a baud rate of 115200 bps, the number of system-clock cycles per bit is:

$$CYCLE = Fclk / BAUD\_RATE = 27MHz / 115200 \approx 234$$

This CYCLE value governs the duration of the start bit, eight data bits, and stop bit. The design intentionally employs single-sample mid-bit timing instead of 16× oversampling to reduce FPGA resource utilization while maintaining robust communication.

The transmitter implements a four-state FSM: IDLE, START, SEND_BYTE, and STOP.

In the IDLE state, the module asserts tx_data_ready to indicate availability. When valid data arrives, the byte is latched, and the FSM initiates transmission by driving a low start bit for one CYCLE. During SEND_BYTE, the eight data bits are shifted out LSB-first, each for one CYCLE. The STOP state drives a high stop bit before returning to IDLE. The internal cycle counter and bit counter guarantee deterministic timing and glitch-free serial output.

Interface the UART module implemented on the FPGA with a PC and verify accurate data transmission and reception using the PuTTY serial terminal.

Analyze the performance of the UART system across multiple baud rates and ensure stable operation under varying communication speeds.

Validate the correctness and reliability of the UART design through waveform-level simulation, FPGA hardware testing, and communication monitoring.

Demonstrate that the implemented UART architecture can be used as a foundational communication block for larger digital systems requiring serial data transfer.

Together, these objectives guide the development of a complete UART communication framework that is efficient, accurate, and suitable for FPGA-based embedded applications.

V. EXPECTED RESULTS & ANALYSIS

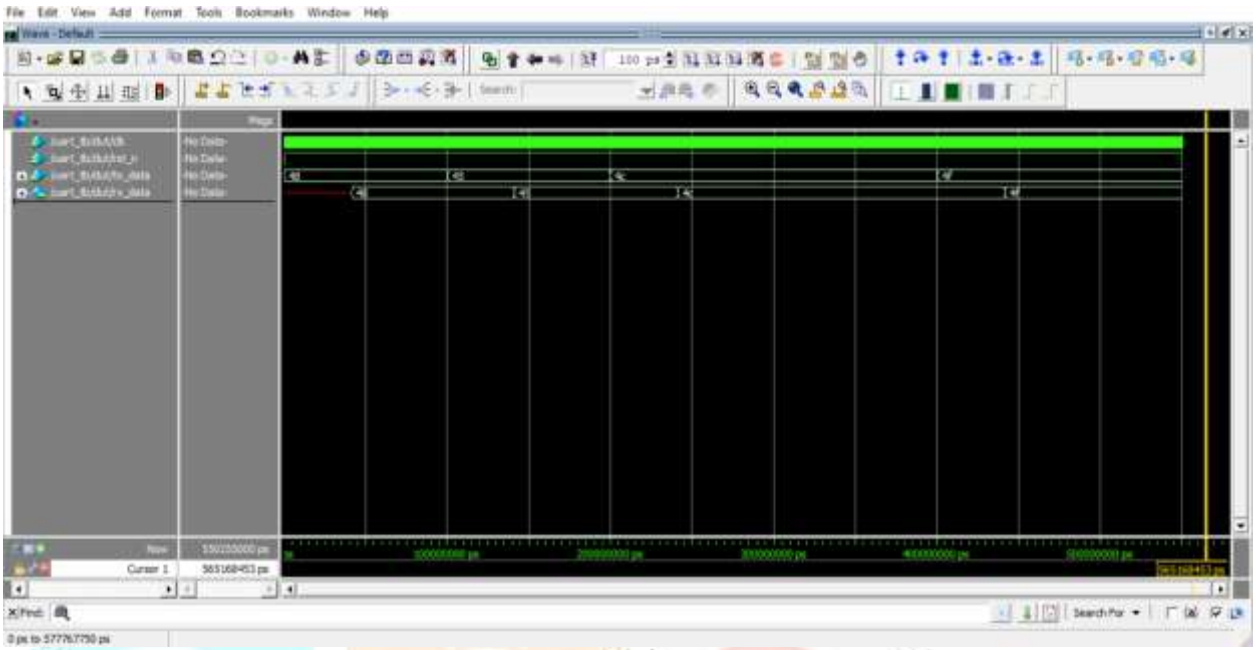

Fig 2: Simulation Result

Simulation Waveforms: Waveforms will demonstrate correct framing with a clean start bit, accurately shifted data bits, and a valid stop bit. The timing between bits will precisely match the configured baud rate (e.g., 104.16 µs per bit at 9600 baud).

Hardware Demonstration: The system will successfully relay keypresses wirelessly via Bluetooth and display messages received from a smartphone on the LCD, confirming full-duplex bidirectional communication with zero frame errors under normal operation.

Performance Analysis (Post-Synthesis):

Resource Utilization: The entire system (UART core, keyboard scanner, LCD controller) is expected to utilize a very small fraction of the Tang Nano 9K's resources (estimated < 5% of LUTs and Registers), leaving ample room for additional functionality.

Timing Analysis: The design is expected to meet timing constraints at 27 MHz, with no setup or hold violations, ensuring reliable operation.

VI. CONCLUSION

The successful implementation of the UART module on the Tang Nano FPGA demonstrates that FPGA-based platforms can provide reliable and efficient serial communication comparable to dedicated microcontroller solutions. The design, consisting of a baud rate generator, transmitter, and receiver, operated with stable timing and delivered error-free real-time data transfer between the FPGA and a PC using PuTTY. Experimental results confirmed consistent baud-rate accuracy and robust communication across multiple test runs.

This work validates the suitability of FPGA-based designs for embedded communication tasks, offering superior flexibility for customization and integration into larger SoC architectures. The modular Verilog implementation also enables easy scalability for advanced features such as parity control, FIFO buffering, or multi-protocol support. Overall, the project highlights the effectiveness of FPGAs as a powerful platform for developing dependable and adaptable communication subsystems.

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