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Low Power Consumption Of Cmos Full Adder Using Complementary Pass Transistor Logic

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***Abstract*—** The growing technology demands high speed, less power and small area processors. The adder circuit for example the ALU in CPU must offer high speed and low power for each calculation. Full adder circuit can be built using various metal-oxide semiconductor transistors. In this paper the work consists of a CMOS and a CPTL based full adder circuits implemented using 45nm technology. To ensure a good quality, low power consuming and less heat dissipation CPTL logic is preferable over a CMOS logic. The use of 4 terminal transistors helps to reduce error and delay at lower voltage and enrich the performance. Mobility of electrons and mobility of holes are having same width to get less power delay product.

***Index Terms*—Low Power, Delay, CPTL, Full Adder, Higher Efficiency.**

I. INTRODUCTION

A typical generic single-polysilicon silicon gate, p-well, n-substrate form a CMOS. As in the NMOS case, variants in this process such as a second metal layer, a second polysilicon layer, additional implants, oppositely doped structure, or metal gates are also well established. As the number of inputs to a multi-input logic gates grows, the power, delay, optimized output, vary by point of its nature. CMOS gate requires approximately twice as many transistors as an NMOS gate. To overcome, this disadvantage, conventional circuit with equal 14 NMOS and 14 PMOS transistors are used. A conventional full adder circuit is a digital logic circuit that can add bits with an additional carry-in bit, producing the sum of bits along with a carry-out bit. The full adder circuit with pull-up and pull-down networks uses total 28 transistors with standard Complementary Metal Oxide Semiconductor (CMOS) logic, providing robustness against voltage scaling and transistor sizing, which are essential to provide reliable operation at low voltage with arbitrary transistor sizes. It consists of three input bits A, B, Cin and two output bits Sum, Cout/Carry that are represented as the bit parameter. According to Moore's Law, the speed of technology development is directly proportional to the increase in number of transistors with increase in other parameters of circuits. In this paper 45nm technology is used by considering the speed and propagation of the technology. Power reduction is very essential in VLSI circuit designing process, especially the reduction in power delay product (PDP) is very important for a good digital circuit and this can be achieved by improving various parameters like width-to length (W/L) ratio [1].

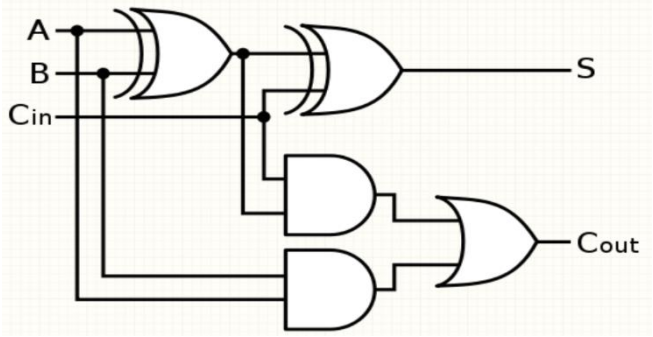

Fig.1 Full Adder Gate Logic Circuit

$$\text{Sum} = A \oplus B \oplus Cin \qquad (1.1)$$

$$\text{Carry} = (A.B) + (Cin.(A \oplus B)) \qquad (1.2)$$

Figure 1 denotes the logic AND, EXOR and OR gates, that gives the conventional circuit of the constructed diagram used in this paper. By employing a pass transistor logic circuit, the delay produced by this circuit is increased while consuming less power. The degree to which a signal resembles an ideal voltage source is a measure of its strength. When the gate voltage is "high," the NMOS transistors turn on. In contrast, PMOS is said to as being in an OFF state when its gate voltage is "low" in relation to the source, which is "0." However, when these two transistors are combined, the circuit becomes more stable, uses less space, and is highly efficient. The width and length variations add up to an effective output. The enhancement mode is used, while working them in the practical manner in cadence tool, circuits are rigged up using 4 terminal transistors which is directed to increase in power and delay propagated but using 3 terminal transistor makes the different in major types. The pass transistor logic circuit works on minimum power, delay and reduce chip area. The good pass-transistor circuit switches faster rather than the conventional circuits with very low output as power and give increased efficiency with it.

II. IMPROVED WIDTH

The amount of data that is transferred from a connection or interface is measured in bits per second (bps) or bytes per second (B/s). This shows transfer of electric charges which makes the complexity in architectural level also in wider path of single transistor. In this paper, the width and length of the transistors are initiated as default values with respect to cadence tool with the condition Wp = Wn in both the circuits.

2.1 Settling Time

Basic RC circuit denotes best that the time required for a circuit's input to reach the output of it by difference in tolerance band typically with positive and negative of 0.1% to 10% and obtain a steady-state value to the improved conditions with accordance to time constant of the t_settle equations.

$$t\_settle = n \times \tau = n \times R \times C \qquad (2.1)$$

where n depends on accuracy required
- n ~ 2.3 for 90% settling (10% error)
- n ~ 4.6 for 99% settling (1% error)
- n ~ 6.9 for 99.9% settling (0.1% error)

The changes in temperature values also matters with respect to the input and settling time frequency. Improvement in bandwidth makes the variation of output at faster rate in range, with increased delay towards the values. In both CMOS and CPTL circuit, the given input voltage will be obtained in output voltage. This paper doesn't fetch the same values of the voltage given in input which concludes in 99% settling in delay of the circuit but also improve the power required from conventional to CPTL. The moderate chosen value to the technology node of 200n produced by PDK documentation of generic for

200nm in library specifications. CMOS as the full swing, strong drive, no threshold drop produce a clean logic level where as PTL comparison as the same with degraded level of 99%. While performing the settling operation the pass transistor logic gives out the passing of '1'. Initially Vgs = Vdd strong inversion and weak inversion plays a delayed output when the input switching varies, this makes the logic to terminate in falling point with respect to rising. The complementary pass transistor logic (CPTL) has a combination of NMOS and PMOS transistors whereas in traditional pass transistor logic (PTL) only the NMOS transistors are used in configuration of the logic in it. To balance the speed of the processor, traditional PTL is not suitable and this logic degrades logic '1'. This could be resolved by using CPTL logic.

2.2 Response of Magnitude

The primary distinctions between CPTL and CMOS, when CMOS serves as an amplifier, are characterized by gain characteristics and bandwidth behavior. Frequency transmission solely uses a switching mechanism, which causes an output delay, rather than signal amplification. The output is significantly impacted by the variance in the input and its difference. This draws attention to the circuit's switching process and any minor disruptions that could produce disparate output outcomes. Compared to CMOS, CPTL performs and is used very differently. It offers any output response and has a unity gain (0dB) factor over the circuit's passband. For eight stages, the response in CPTL begins flat at 0 dB and then abruptly rolls off at -160 dB, as 8 stages Because CPTL has 10 transistors, the response begins flat at 0dB and then rolls off abruptly at -160dB over 8 stages, hitting the -3dB mark at 2-3 GHz. On the other hand, CMOS boasts real DC gains of 20–40 dB, which are based on the output response product. Importantly, CMOS has a higher response than CPTL, which produces a delayed output because of the input's variable switching. Since there is no regenerative activity in the circuit, restoration is frequently performed in several step gains, particularly for short signal routes, and it has low noise immunity. The response of CPTL, which includes 10 transistors, starts flat at 0 dB and then quickly rolls off at -160 dB across 8 stages, reaching the -3 dB mark at 2-3 GHz. On the other hand, CMOS boasts genuine DC improvements based on the output response product that range from 20 to 40 dB. Crucially, CMOS responds faster than CPTL, which results in a delayed output due to variable switching of the input. Restoration is often carried out in many step gains, especially for short signal pathways, and it has low noise immunity because the circuit lacks regenerative activity.

$$PTL = 1/(2\pi \times R\_TG \times C\_load) \quad (2.2)$$

Where,
R_TG ~ 2-3 k/ohms (parallel NMOS || PMOS),
C_load ~ 10-20f F, CPTL ~ 5-7 GHz per stage

$$CMOS = 1/(2\pi \times R\_out \times C\_load) \quad (2.3)$$

Where,
R_out ~ 5-10 k/ohms (output impedance),
C_load ~ 10-20 fF, CMOS ~ 1.5-3 GHz per gate

2.3 Stability Margins

The circuit should function dependably in any situation, despite differences in noise, temperature, voltage changes, and input conditions. In the CMOS and CPTL circuits covered in this work, the circuit's inherent feedback rejection provides stability and enables it to manage distorted signals. When Wp = Wn and when Wp is twice Wn, the applied voltage has the same threshold values, which are equal to Vdd divided by two. A waveform window is used to record the output response. Additionally, delayed signal transmission results from this configuration, and the delay may be directly or indirectly linked to the way the values change. This can use the margins between high and low logic levels to increase the noise inside the transistors. Every transistor in the CMOS circuit has negative feedback properties via pull-up and pull-down NMOS and PMOS networks. In contrast to the Wp = 2Wn scenario, the circuit operates best when power is the primary focus, even under rail-to-rail conditions with Wp equal to Wn. Increasing the circuit's

complexity does not decrease the input's path or flow when utilizing NMOS to GND or PMOS to Vdd. Eliminating DC current routes, which offers limitless DC loop gain and forces the output to a single state even with two separate inputs, is the only practical solution. The primary cause of instability in CPTL circuits is charge sharing among nodes, which can also result in floating circumstances because the circuit lacks a strong "0" or "1" input. This may lead to a less dependable output with a switching delay. The output waveform is significantly altered by the phase margin decrease of 30 to 45 degrees in PTL circuits and the phase margin reduction of 60 to 90 degrees in CMOS circuits.

III. PROPOSED CONDITION

3.1 Trade-Off Analysis

Transistors are used to design a basic conventional or traditional CMOS circuit which contains combination of PMOS and NMOS and five inverter set-up. The number of transistor may increase even with increase in complexity.

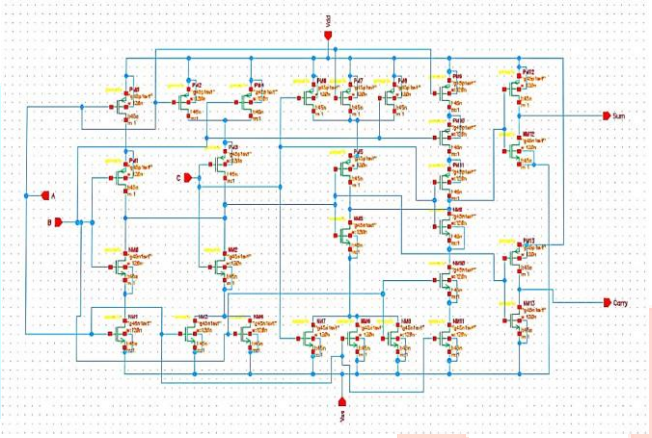

Fig.2 A Conventional Full Adder Circuit using 28 T

Figure 2 shows the use of transistor count and the area which makes the circuit to have power dissipation and also slower switching operation due to more number of nodes used for ratio of calculation in it. Because incomplete logic levels can be obtained, switching is made simple and instantaneous by using an inverter towards the output. Propagation delay is increased by higher resistance and parasitic capacitance; nevertheless, power efficiency can be improved by employing stack transistors.

Strong and full swing carry output is guaranteed by the full adder, which is essential in its critical path. Low power degradation is the primary aim of this design. The output serves as a buffer to stabilize it, and it may be enlarged and added to increase speed without requiring a large amount of space or power. Design propagation must be traded off by taking robustness and area consumption into account. Maintaining a steady value across the circuit is crucial, and the circuit has a faster switching speed. When trading the circuit, transistor size counts because for Wp = Wn, the value of (W/L) equals 120n to both. In contrast, the values of 120n and 240n are utilized to obtain the necessary quantity of lower power utilizing typical conditions for Wp = 2Wn (W/L). Design propagation must be traded off by taking robustness and area consumption into account. Maintaining a steady value across the circuit is crucial, and the circuit has a faster switching speed. When trading the circuit, transistor size counts because for Wp = Wn, the value of (W/L) equals 120n to both. In contrast, the values of 120n and 240n are utilized to obtain the necessary quantity of lower power utilizing typical conditions for Wp = 2Wn (W/L).

3.2 Optimal Power-Delay Product

The energy efficiency is measured by quantified average power consumption using the term called propagation delay. In CMOS with Wp = 2Wn condition the power is more compared to Wp = Wn condition. So, by optimizing this two matter, the CPTL condition is also implemented in this matter to get the power delayed product with more stable output with any number of input.

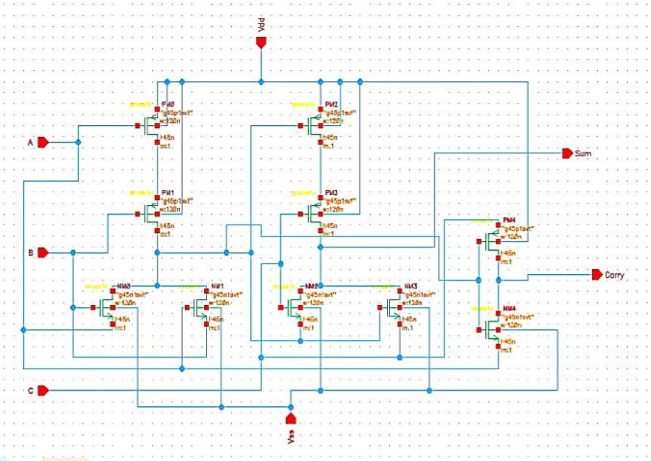

Fig.3 A Complementary Pass Transistor Logic using 10T

Figure 3 shows CPTL circuit when compared to CMOS which contribute in the case of dynamic power by translating the fewer gate capacitance in charging and discharging of the switching. CPTL carryout the single output and gives the delayed featured but consume less power alter to CMOS makes it more reliable, using of capacitance moves the power in increased order. With Wp = Wn the output is stabilized but with Wp = 2Wn usage of capacitance makes it in a order while getting the response of output. Sum and Carry is obtained by using the inverter while complementing the given input to value the output.

3.3 Efficiency of Power

It is demonstrated that CPTL produces superior efficiency when CMOS and CPTL are effectively compared. The performance domains, each of which is founded on its basic architecture, are to blame for this. When comparing the two circuits, the difference in circuit design results in higher efficiency, suggesting that this is a significant design aspect. A single transistor can consume 50–70% less energy when architecture is used strategically, which maximizes benefits and increases effectiveness. Both pull-up and pull-down transistors have a higher density and a more stable circuit when Wp equals Wn in CMOS. Its delayed output doesn't pose any problems because the CPTL circuit has an inverter connected. Instead of using the Wp = 2Wn condition, the condition Wp = Wn is justified in this paper and produces valid results. This results in a power delay product in the femto range, making the selected condition preferable in terms of both power and delay. Even when the circuit complexity develops, the sizing frequently climbs in comparison to the conditions produced. The input difference modifies the circuit's current flow and influences the priority of switching with equal voltage. Higher efficiency, which is ideal in every way, is demonstrated by the condition employed, which makes it special for use in circuit manufacturing. Even in circuits with degradation, power is cut according to the input parameter bit in the CMOS state, which is determined by the Wp = Wn rule.

IV. COMPARISION WITH TWO DIFFERENT CONDITION

Table 4.1 shows the power, delay of propagation (tP/tPD) with these values, we use rise time and fall time formulas with a Vdd/2 threshold for each voltage value to get the Power Delay Product (PDP). Due to the circuit's steady change with increased power and delay, the PDP after 1.2 V is raised by more than 63%. Even with the identical circuit and voltages, the input given to obtain power or any other parameter will instantly alter the output. When tuning it in other parameters, the PDP values are optimal due to the steady increase in power and decrease in latency.

Wp=2Wn						
Vdd (V)	CMOS full-adder			Proposed CPTL based full-adder		
	PD (mW)	*tP (ps)*	*PDP (fJ)*	*PD (uW)*	*tP (ps)*	*PDP (fJ)*
1.2	15.93	42.96	856.67	493.85	87.32	43.12
1.4	18.12	33.83	613.30	701.41	389.01	272.85
1.5	19.15	32.94	631.38	797.85	351.55	280.48
1.8	22.43	31.23	700.76	1126.8	319.45	359.95
2.0	24.65	30.80	759.55	1381.5	302.55	417.97
2.2	26.79	31.07	832.71	1661.2	281.35	467.37

TABLE 4.1: POWER CALCULATION FOR Wp = 2Wn CONDITION

Formula for Propagation Delay (t_{PD}):

$$t_{PD} = \frac{(t_{PLH} + t_{PHL})}{2} \qquad (4.1)$$

Where t_{PLH} is Low-High Propagation Delay, t_{PHL} is High-Low Propagation Delay

Formula for PDP is :

$$PDP = Power * t_{PD} \qquad (4.2)$$

Above formulas are used for calculation in both the table and obtained the power value with respect to it.

TABLE 4.2: POWER CALCULATION FOR Wp=Wn CONDITION

Table 4.2 gives a clear picture about which condition is better or not. Here the table denotes the difference between CMOS and PTL readings with Wp = Wn conditions.

Wp=Wn						
Vdd (V)	CMOS full-adder			Proposed CPTL based full-adder		
	PD (uW)	*tP (ps)*	*PDP (fJ)*	*PD (uW)*	*tP (ps)*	*PDP (fJ)*
1.2	407.75	27.7	11.294	252.13	7.071	1.752
1.4	517.76	24.3	12.581	338.06	6.178	2.088
1.5	557.97	22.7	12.665	375.39	6.006	2.254
1.8	697.87	22.9	15.981	483.87	6.075	2.939
2.0	727.67	22.6	16.445	554.82	6.041	3.352
2.2	780.18	22.6	17.640	625.20	5.953	3.755

By implementing the values in both Table 4.1 and Table 4.2, it can be majorly observed that Wp = Wn condition holds good with all the practical approach in it. The input parameters provided with absolute definition and definite differences by using both the condition. The variation of both the table shows, how impactful even if the condition with Wp = Wn will be optimal to use even with the pull-up and pull-down network transistors rule about it. Clearly, showing CMOS has 10-11% more power rather than CPTL, this concludes the effective use of both conditions with proper usage. Figure 4 shows that the schematic used to conclude and implementing the readings for the circuit is given by Vdd which is constant with variation in the stimuli column of the input. The difference in voltage makes the transmission of signal or the movements of electrons even wiser in less voltage but it is best in 1.8V. The circuit used in this paper are basic to compare the use and power calculation with comparison between PTL and CPTL circuit. This makes implementation of the correct circuit and get benefit from it.

V. RESULTS

Figure 4 is the test schematic circuit for full adder which is also same for CPTL by having the constant voltage of 1.8 V through the various inputs, by changing the voltage in stimuli makes a slight difference in power.

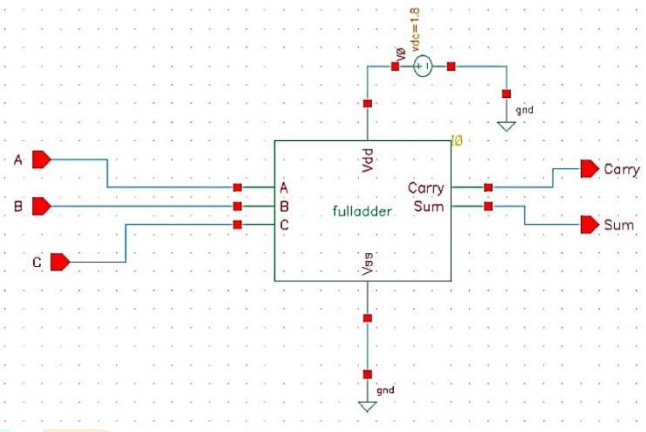

Fig.4 Test Schematic of Full Adder

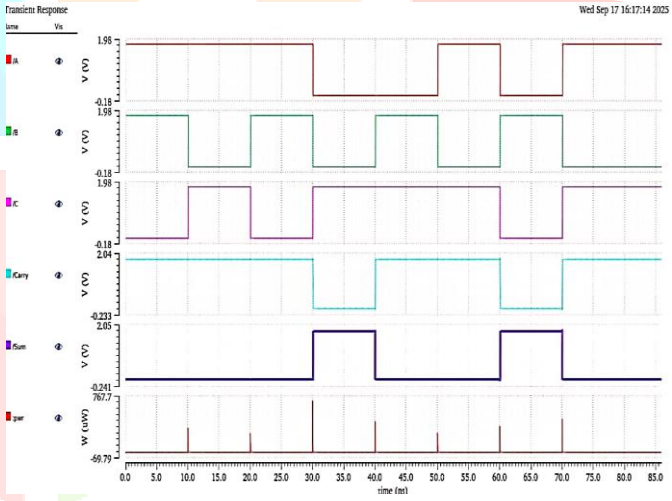

Fig.5 Output Waveform of Full Adder

Figure 5 shows a clear waveform of CMOS in particular to CPTL circuit used. The Table 4.2 values having the data in it provides the major power reduction done by implementing Wp = Wn rather than in Wp = 2Wn. Rise time and fall time is given in pico (p) values because of the smooth square wave output from it with precised 10n of delay value from one time interval to another makes the uniform output provided by input. The power in both input and output stays as neutral using uniform formation of current inside the circuit. In the Wp =2Wn power is higher because of the more power towards NMOS transistors while Wp = Wn manages having same width-to-length values. Transcient response will be varying according to the chosen value in circuit. Power obtained here is in (mW).

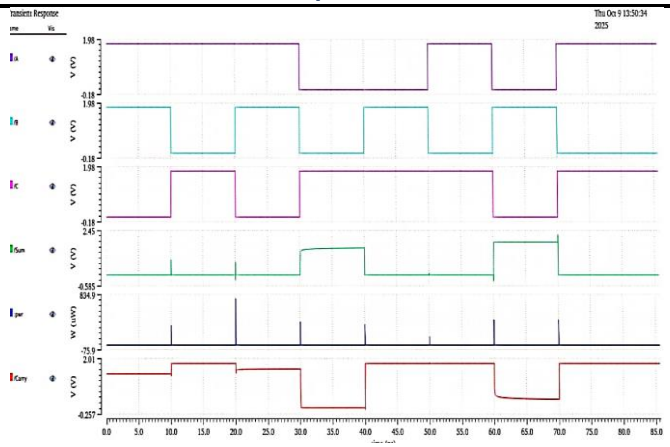

Fig.6 Output Waveform of CTPL Circuit

Figure 6 gives a clear picture of CPTL output waveform with all the preferences given for CMOS along with both the conditions of Wp = 2Wn and Wp = Wn.

Difference between CMOS and CPTL brings out the valuable outcomes, by getting the required less power with proper PDP value. 1.8V can be chosen to denote any number of transistors as it is considered as standard value while assuming and configuring the output to any type of input. Whereas, power obtained is in (uW) with a femto value of PDP makes a better condition with optimal elements provided by the circuit. Variation in the Sum and Carry is because of the switching input given with accordance to delay measurement.

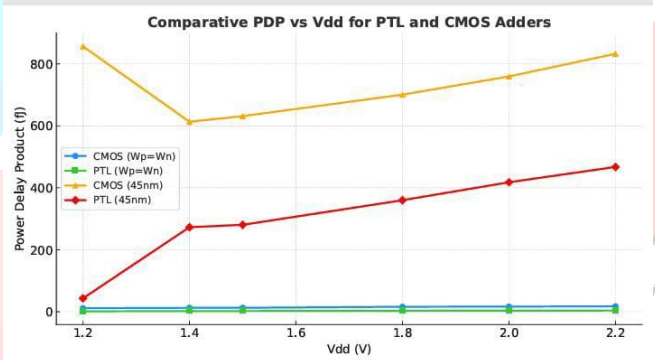

Fig.7 Comparative Line Graph for both the conditions

Figure 7 is a Line Graph which shows the major difference that is done by using two different conditions. It enhances the image of slight fluctuation with respect to the given voltage but with Wp = 2Wn it shows the major variation and significant disturbance with increase in voltage but it doesn't happen with Wp = Wn. From this graph it is observed that the Power delay product is minimum for Wp = Wn condition signifying this is the best design.

VI. CONCLUSION

Processors for example that has to be ported to other location must utilize less power to enhance the efficiency. Full adder circuits are designed using different techniques in early research. Here, CPTL circuit with 10 transistor count is designed to reduce the size. A comparison is shown between the PDP of CMOS and a CPTL based full adders. Also this paper presents difference between CMOS and CPTL in their power delay product. Design voltage is simulated from 1.2V to 2.2V. The strategical use of topology makes the circuit sustainable to its core features. With maximum benefit lower energy in CPTL transistor makes it more effective because the input is connected to source. Condition of Wp = Wn have nearly 190% less power when compared to other condition considered in this research paper. To stabilize the contact, 2 NOR gates are used in CPTL, with consideration towards the conditions of pull-up and pull-

down transistors gives the best outcome. Major advantage of CPTL logic is that it takes less power for switching compared to PTL and CMOS. In this paper it is shown that Wp = Wn condition gives good range of power rather than Wp=2Wn using cadence tool. Less power consumption by the components increases the lifespan of the device and helps in maintaining cost efficiency. Thus, low power operated devices are at less risk from getting damaged. By the above observations it can be concluded that the CPTL full adder needs less area, less delay and also less power dissipation. Whereas the CMOS full adder requires many transistors hence occupies more area. More delay is encountered and also more power dissipation. Hence CPTL full adder is far more advantageous than CMOS full adder.

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