IJCRT.ORG ISSN : 2320-2882

INTERNATIONAL JOURNAL OF CREATIVE RESEARCH THOUGHTS (IJCRT)

An International Open Access, Peer-reviewed, Refereed Journal

Design And Implementation Of ADPLL Using PYNQ Z2 FPGA

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Abstract: This work presents the design and implementation of an All-Digital Phase-Locked Loop (ADPLL) on the PYNQ-Z2 FPGA platform. The proposed system addresses limitations of traditional analog PLLs by utilizing fully digital components, enabling higher precision, scalability, and seamless integration with modern digital systems. The ADPLL architecture integrates a Time-to-Digital Converter (TDC), a Proportional–Integral Digital Loop Filter, a Digitally Controlled Oscillator (DCO), and a Frequency Divider. A normal filter is employed to improve noise immunity and enhance loop stability. The design is implemented in Verilog, synthesized, and deployed on the PYNQ-Z2 FPGA. Simulation and hardware tests validate the system's ability to achieve minimal jitter, zero steady-state phase error, and high synchronization accuracy, making it suitable for communication, signal processing, and clock synchronization applications.

Keywords **-** All-Digital Phase-Locked Loop (ADPLL), PYNQ- Z2 FPGA, Time-to-Digital Converter (TDC), Digital Loop Filter, Digitally Controlled Oscillator (DCO), Frequency Divider, Phase Synchronization.

I. INTRODUCTION

The All-Digital Phase-Locked Loop (ADPLL) plays a crucial role in modern digital systems, especially in communications, signal processing, and clock synchronization applications. Unlike traditional analog PLLs, the ADPLL is implemented entirely with digital components, offering improved scalability, adaptability, and compatibility with digital systems.

This work focuses on the design and implementation of an ADPLL on the PYNQ-Z2 FPGA platform. The PYNQ-Z2 provides efficient digital signal processing capabilities and a flexible hardware interface, making it an ideal platform for implementing complex designs. The primary motivation behind this project is to overcome the limitations of analog PLLs in precision and flexibility, ensuring robust signal synchronization in high-speed digital environments.

The project also demonstrates how digital filters—specifically a normal filter—can be used to reduce noise and maintain system stability in ADPLL applications.

II. LITERATURE SURVEY

L. Shi *et al.* [1] proposed a frequency error prediction method for accelerating the locking process in bang-bang ADPLLs, thereby improving synchronization speed in high-speed communication systems.

S. Safwat *et al.* [2] introduced a low-power bang-bang ADPLL design that employs programmable loop filter coefficients, reducing power consumption while maintaining performance in energy- sensitive environments.

J. Xiang *et al.* [3] presented a wideband DCO architecture offering precise frequency control with a large tuning range and fine resolution, addressing challenges in modern communication systems.

S. Jang *et al.* [4] developed a loop gain tracking technique using autocorrelation in bang-bang phase-frequency detection, improving synchronization accuracy and speed.

W. Namgoong [5] proposed a modified proportional–integral loop filter to suppress DCO noise, enhancing noise performance in precision timing applications.

M. J. Gao *et al.* [6] compared LC-VCO and LC-DCO designs in 65 nm CMOS technology, evaluating trade-offs in tuning range, phase noise, and power consumption.

A. K. Sharma *et al.* [7] suggested a pulse-shrinking TDC-based integer-N digital PLL architecture, improving resolution in frequency synthesis.

A. Hajimiri and T. H. Lee [8] demonstrated digitally enhanced phase- locking circuits for improved noise immunity and scalability in high- speed communications.

Y. Kim *et al.* [9] proposed a fully synthesizable ADPLL with a TDC, offering low power consumption and high scalability for digital applications.

H. Hsu *et al.* [10] investigated advanced digital frequency synthesis techniques, focusing on TDC-based PLLs for high-performance communication systems

III. .PROBLEM STATEMENT

High-speed digital systems require precise synchronization of signals even in noisy environments. Traditional analog PLLs face limitations in integration, scalability, and precision when applied to modern systems.

IV. OBJECTIVES

The objectives of this work are to design an all-digital, FPGA-based PLL that can:

- Enhance precision in signal synchronization.
- Support scalability across various frequency ranges.
- Reduce design complexity compared to analog implementations.

V. METHODOLOGY

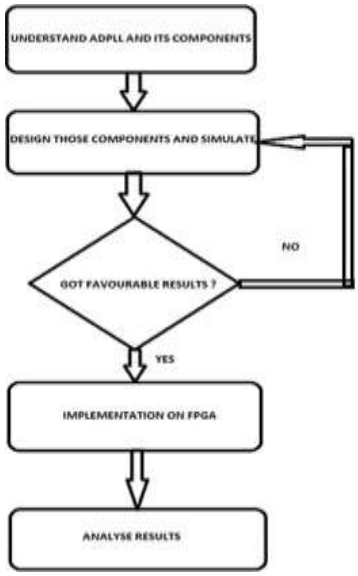

Fig 1. Design Flow

1. Design and Simulation:

- Design the ADPLL architecture, including phase detector, loop filter, and digitally controlled oscillator (DCO).
- Simulate the system using tools like MATLAB/Simulink or Vivado to validate the design.

2. Implementation on PYNQ Z2 FPGA:

- Program the PYNQ Z2 FPGA using Verilog or VHDL to implement the ADPLL components.
- Use a normal filter to manage noise and stabilize the feedback loop.

3. Testing and Validation:

- Input test signals with varying frequencies and analyze the ADPLL's performance in locking to the desired phase and frequency.
- Measure metrics like jitter, lock time, and phase error using onboard FPGA debugging tools.

4. Optimization:

- Adjust filter parameters and loop dynamics to achieve optimal performance.
- Iterate the design based on testing results to enhance stability and accuracy.

VI. WORK DONE

The ADPLL consists of the following main components:

- **TDC** – Measures phase difference between reference and feedback clocks.

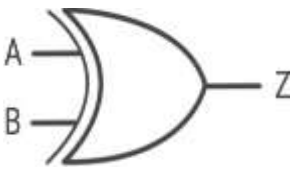

Fig 2. TDC

- **Digital Loop Filter** – Processes phase error using proportional and integral gain to eliminate steady-state error.

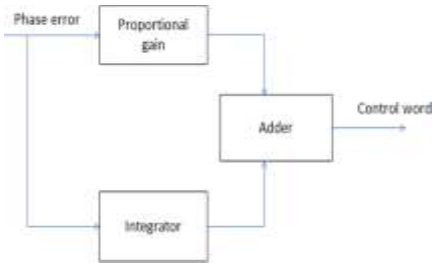

Fig 3. DLF

- **DCO** – Adjusts output frequency based on the loop filter's control signal.

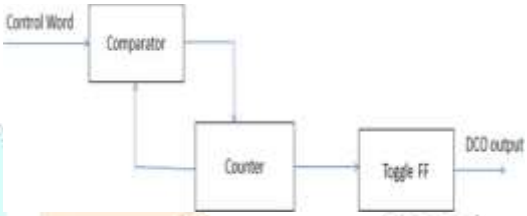

Fig 4. DCO

- **Frequency Divider** – Divides the feedback signal frequency for comparison.

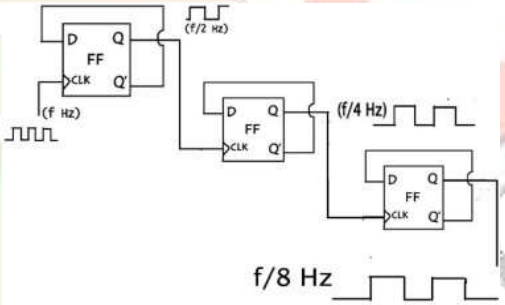

Fig 5. Frequency Divider

Each component was first implemented and verified individually before being integrated into the complete ADPLL design.

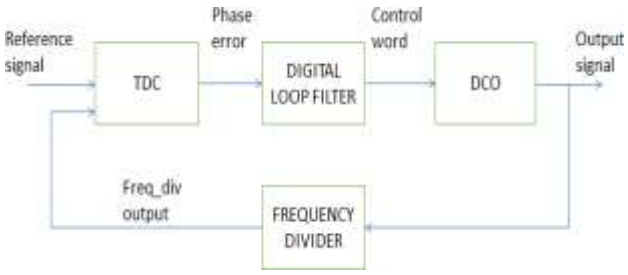

Fig 6. ADPLL

Then, the circuit is verified through simulation of its Verilog code. The screenshot of wave form is given below.

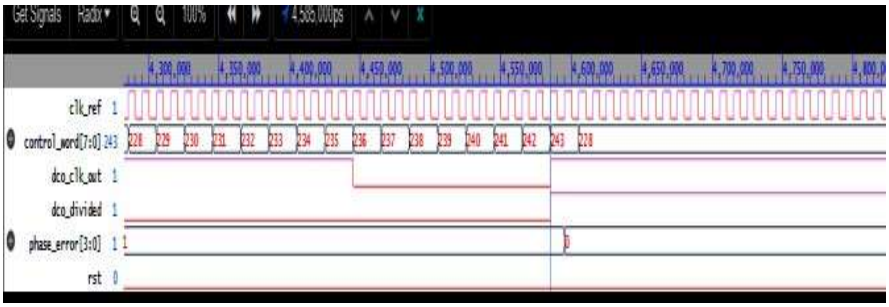

Fig 7. ADPLL simulation waveform

VII. IMPLEMENTATION ON FPGA

The implementation process included synthesis, placement, routing, and bit stream generation:

- **Synthesis** – HDL code was analyzed and mapped to FPGA logic resources.
- **Implementation** – Logic elements were placed and routed to meet timing constraints.

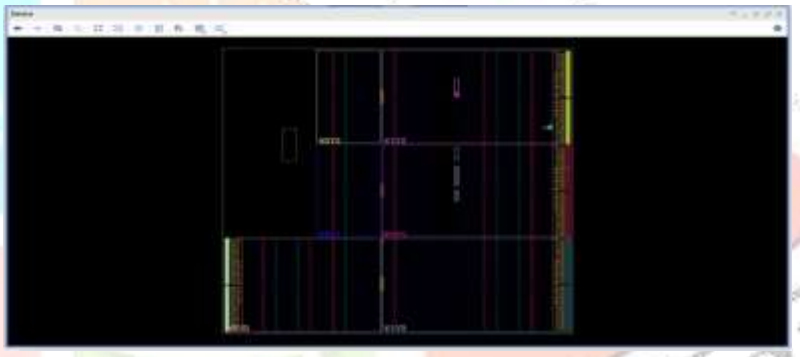

Fig 8. Implemented ADPLL design

- **Bitstream Generation** – The final bitstream file was created and programmed onto the PYNQ-Z2 FPGA.

Experimental setup:

Fig 9. Experimental Setup

The above picture shows the experimental setup for the project, in which the ADPLL is implemented on the PYNQ-Z2 FPGA.

VIII. RESULTS

When the reset signal is active, the ADPLL is held in its initial state on the PYNQ-Z2 FPGA. Internal signals like the control word and DCO output remain at default values with no meaningful oscillation. This ensures the system starts from a known, stable condition before operation begins.

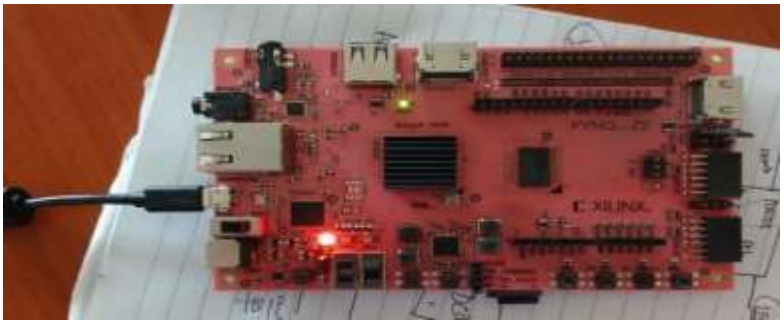

Fig 10. Reset on condition

Once the reset is deactivated, the ADPLL begins normal operation and quickly adjusts the DCO frequency. As seen in the output, the DCO clock aligns with the reference clock, indicating successful phase locking. The phase error stabilizes near zero, confirming the loop is locked and tracking accurately.

Fig 11. After Reset – Phase Lock Condition

IX. CONCLUSION

- In this project, an ADPLL was successfully implemented on the PYNQ-Z2 FPGA.
- Phase lock achieved with zero steady-state error using counter-based DCO.
- Frequency divider stabilized feedback for accurate phase comparison.
- Verified design functionality via simulation and on-board analysis.

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