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TEST COMPRESSION AND REORDERING IN BENCHMARK CIRCUIT TESTING

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Abstract - In Design for Testability (DFT) scan design is an efficient method to overcome problems in testing. VLSI suffers from excessive power consumption during testing due to higher switching activity. This paper proposes a methodology called state skip LFSR to reduce number of patterns and algorithm to minimize switching activity by reordering patterns [1] generated from test pattern generator (TPG). Reduction of switching activity is achieved by decreasing hamming distance among successive test patterns through modified prim's algorithm. Our proposed methodology is implemented in ISCAS'89 benchmark circuits a standard reference circuit called s27 . Experimental result shows an improvement of 54.5% in terms of switching activity with 100% fault coverage in conventional LFSR and 67.5% in state skip method.

Keywords- *Test pattern generator , Linear feedback shift register , Modified Prim's algorithm, State skip LFSR, fault coverage*

I.INTRODUCTION

In modern VLSI , digital circuits operated in either two modes of operation functionality mode and test mode. In functionality mode all the inputs should be applied to get corresponding output. In the same way all the patterns must be tested in test mode for proper functioning of circuit. By applying all possible input combinations results higher switching activity. During testing Test pattern generator is connected at input side to generate input patterns for corresponding bits and output response analyzer is connected to achieve desired output. By adding this additional structure power consumption of the entire circuit becomes high. In sequential circuit external inputs which could not be controlled by the circuit hence scan chain concept is introduced to monitor the testing section. A scan chain is created by number of flipflops connected asynchronous with output of one flipflop to input of another flipflop. The input of first flipflop called scan in where input file is fed and output of last flip flop called scan out where we can take shifted data out. Scan chain are inserted into design to shift test data in and out of circuit. To create patterns TPG is that the simplest method.

TPG here is linear feedback register. Linear feedback register could be a register whose input bit may be a linear function of its previous state. LFSR comprises series of D flipflops depends on size of LFSR. For N bit LFSR, N–Number of flipflops used. 2^N-1– maximum possible output. In LFSR maximum number of states depends on seed and tap connections. In LFSR some states are feeded back to the system through logical ex-or. Hence, to check this circuit 3 bit LFSR is employed as test pattern generator. The polynomial which supplies maximal length or all possible output combination called primitive polynomial. For 3 bit LFSR maximal length is 2^3-1. Primitive polynomial for 3 bit LFSR is x3+x+1. Primitive polynomial of 4 bit LFSR may vary , according to that we can design the logic. Once the pattern generated , these patterns are compressed by a method called state skip LFSR and implemented in XILINX VIVADO. The result of this circuit is then reordered using modified prim's algorithm hence implemented in MATLAB software. The

Reordered result of compressed patterns applied as an input to scan chain of testing circuit called S27. Here S27 sequential benchmark circuit is employed as testing circuit. The experimental result shows an improvement of 33.3% reduction in terms of switching activity hence the dynamic power consumption of whole circuit depends on number of switching, capacitance and supply voltage.

$$\mathbf{P(dynamic)} = \mathbf{SA} \times \mathbf{0.5} \times \mathbf{C} \times \boldsymbol{V^2} \times \boldsymbol{f}$$

II. PROPOSED METHOD

There are three main concepts involved in this proposed methodology

A. Test Pattern Generation
B. State skip LFSR (SS LFSR)
C. Modified Prim's algorithm

A. TEST PATTERN GENERATION

Generation of test patterns [2] is done by linear feedback shift register . The patterns are generated based on Primitive polynomial of length 2^3-1 i.e 7 patterns. For 3 bit LFSR maximum vectors generated could be 7 based on polynomial. LFSR with bit size 3 is portrayed in Figure 1.

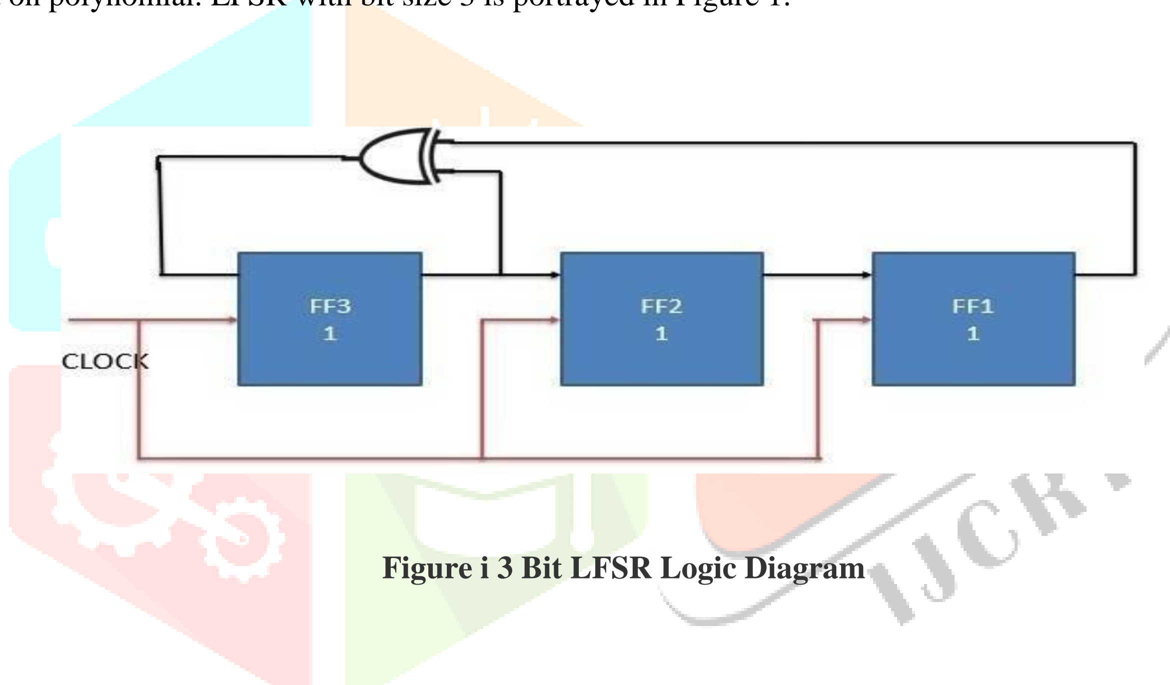

Figure i 3 Bit LFSR Logic Diagram

Test vectors	FF3	FF2	FF1	FF3 XOR FF1
T1	1	1	1(Initial)	0
T2	0	1	1	1
T3	1	0	1	0
T4	0	1	0	0
T5	0	0	1	1
T6	1	0	0	1
T7	1	1	0	1
T1	1	1	1(Repeat)	0

Table 1 3 Bit LFSR Generated Pattern

B STATE SKIP LFSR (SS LFSR)

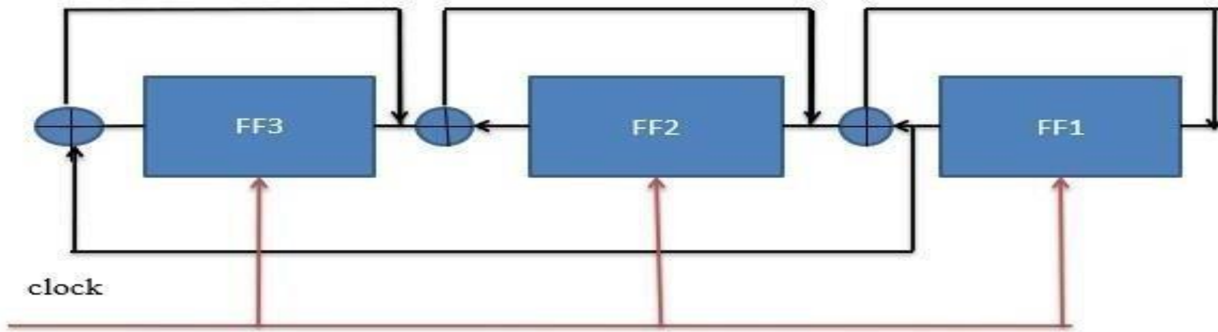

Figure ii State skip LFSR Logic Diagram

Proposed method in this paper is state skipping LFSR method. Normally LFSR generates output based on logic whereas state skipping LFSR skip the states of output of LFSR. N bit LFSR consist of D flip flops and Ex-or gates based on characteristic polynomial. In state skip LFSR we use feedback circuits instead of polynomial. State skip circuit omits predetermined number of states by calculating directly the state after them. M bit state skip LFSR skips M-1 states in conventional LFSR.A State skipping LFSR performs successive jumps with a constant length but state skip circuit skips a predetermined number of states. It has more efficiency when compared to LFSR and length of the patterns get shortened.

VECTORS	FF3	F22	FF1	FF3 XOR FF2XOR FF1
T1	1	1	1	0
T4	0	1	0	0
T7	1	1	0	1

Table 2 State skip LFSR patterns

Reduction of 4 test vectors (7-4=3) is obtained using state skip LFSR.In proposed method Conventional N bit LFSR(N=3) = 7 Patterns;M bit State skip LFSR(M=3)= 3 Patterns

III. TEST VECTOR REORDERING

Reordering of test vectors is done by finding the minimum hamming distance among successive test patterns generated from state skip LFSR. Minimum hamming distance can be calculated using **Modified prim'salgorithm** where the repetition of test vectors is not allowed.

Issues with PRIM'S ALGORITHM

The problem with Prim's algorithm one among a greedy algorithm is to find minimum cost of a spanning treeA group of vertices connected to form spanning tree and these vertices are connected based on weight. The connection among all vertices are established by adding one edge at a time. The addition of neighbor vertices depends on weight of an edge. A vertex is chosen arbitrarily as a root vertex to create minimum spanning tree. Vertex with minimum weight compared to remaining vertices is selected as a proceeding vertex and it is connected to root vertex. This procedure is repeated until all vertices are connected. The spanning tree is completed when n vertices are connected and n-1 edges are formed. To create an efficient spanning tree vertices has to be connected with minimal weight. This criteria can be met by Prim's algorithm .

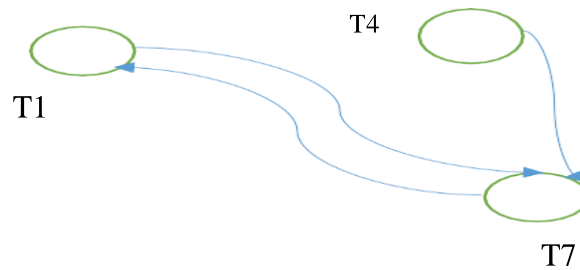

Figure iii Prim's algorithm

In Prim's algorithm minimum cost for a complete tree is computed by considering the entire tree. If this concept is applied to reorder patterns, then repeated test vectors would be available in the final order. This will not meet our goal of decreasing transition among test vectors. For example let as assume a tree is formed with three vertices namely *T1*, *T4* and *T7*. Consider vertex *T7* which is closer to *T1*, but vertex *T4* is the last vertex which is connectedto tree. Then, to establish connection between vertex *T4* and tree, the algorithm will travel through *T7* and reaches *T1*, thereby establishing connection between vertex *T1* and *T7*. Hence, the final order of vertices would be *T1, T7, T1, T4*. From the above example it is clear that many repeated test patterns would be available in final reordered test patterns, which would increase transition among test patterns, thereby test power gets increased. Hence, to overcome this issue Prim's algorithm has to be modified to acheive the goal of minimum power consumption.

IV. MODIFIED PRIM'S ALGORITHM

To overcome the drawback in Prim's algorithm, the algorithm is modified in such a way to eliminate the repeated test vectors in final order. Figure 4 show the implementation of modified Prim's algorithm. In modified Prim's algorithm problem of repetition is eliminated by allowing the vertex to be visited once. Hence the final order would be t1,t7,t4. Modified Prim's algorithm make sure that no test vector is repeated in the final approximated tree. This is how modifications are done to Prim's algorithm to deploy it for the test patter reorderingproblem.

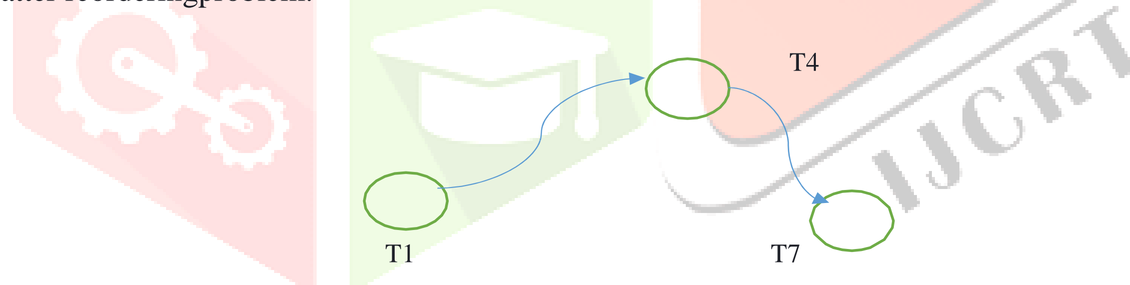

Figure iv Modified Prim's algorithm

Hamming distance calculation in terms of switching activity

Hamming distance (HD) is measured as number of bit positions during which the 2 bits are different. The Hamming distance between two strings, *a* and *b* is denoted as d (t1, t2). By reducing hamming distance between successive test pattern switching activities of circuit get decreased. In 3 bit conventional LFSR ,switching activity reduced from 11 to 6 but when compression technique is applied switching activity becomes 3 and SA of 2 achieved once reordering is performed. Linear feedback shift register used to generate test pattern to test s27 benchmark sequential circuit is of 3 bit size. Initial seed to LFSR is set as *'111'* and test patterns are generated for every clock cycle. Table IV shows switching activity calculation for unordered and reordered pattern of 3 bit LFSR. Table V portrays the unordered and reordered test patterns of state skip LFSR after applying modified Prim's algorithm. Test patterns are reordered in such a way that the hamming distance between consecutive test patterns are 1.

Measurement of switching activity

Power consumption $= SA \times 0.5 \times C \times V^2 \times f$---(1) Power consumption greatly depends on amount of switching activity and it is calculated by equation (1).Load capacitance is referred as c, v refers to supply voltage and f for frequency. From the equation it is understood that switching activity (SA) is directly proportional to power and hence reducing switching activity would lowerpower consumption of circuit. Reduction of switching activity can be achieved by minimizing transition among test pattern through reordering. Switching activity for test patterns *T1* and *T2* is calculated by following formulaein equation (2)

Switching avtivity $(T1, T2) = H(T1, T2)$--**(2)**

Unordered set of vectors		Reordered set of vectors	
Test vector	**Switching activity**	**Test vector**	**Switching activity**
t1-t2	1	t1-t2	1
t2-t3	2	t2-t5	1
t3-t4	3	t5-t3	1
t4-t5	2	t3-t6	1
t5-t6	2	t6-t7	1
t6-t7	1	t7-t4	1
Total	11	Total	6

Table 3 Calculation of switching activity

Switching activity measurement for unordered and ordered test patterns of conventional LFSR is shown in Table V. Column 1 and 2 shows the switching activity for unordered test patterns and switching activity of ordered test patterns are shown in column 3 and 4. It is observed that switching activity of LFSR generated test pattern is 11 before reordering and 6 after reordering test patterns.

Switching activity calculation for unordered and ordered test patterns of state skip LFSR is shown in Table vi. Column 1 and 2 shows the switching activity for unordered test patterns and switching activity of ordered test patterns are shown in column 3 and 4. It is observed that switching activity of LFSR generated test pattern is 3 before reordering and 2 after reordering test patterns.

V. S27 SEQUENTIAL BENCHMARK CIRCUIT

S27 is an ISCAS'89 sequential benchmark circuit used for testing purposes. S27 bench mark circuit is the standard sequential circuit. Here we use s27 benchmark circuit as testing circuit. Test vectors are applied as input to the S27 bench mark sequential circuit.G0, G1, G2, G3 are the input of this circuit. Circuit can be operated in 2 modes: *i) Functionality mode* (SELECT =0) *ii) Scan mode* (SELECT =1). If flip flops in s27 sequential circuit isoperated in normal mode G17(output) depends only on primary inputs G1, G2, G3, G4. In scan mode flip flops are replaced with scan flip flops by adding a multiplexer as an input to D flip flop.

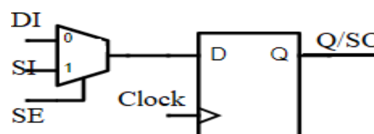

Figure v Mux D scan cell

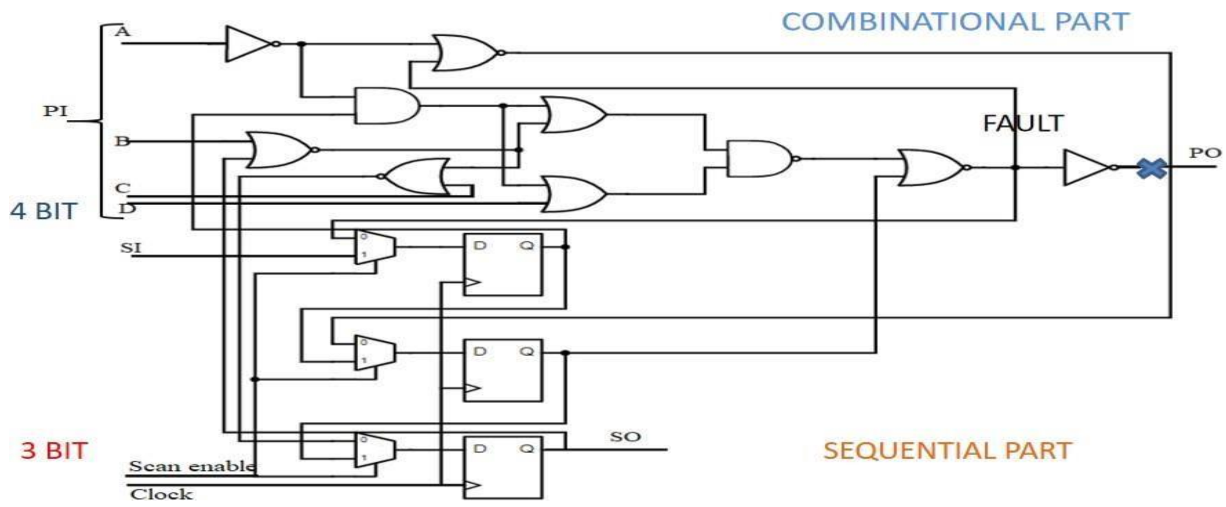

Figure vi S27 sequential benchmark circuit

VI. RESULTS AND DISCUSSION

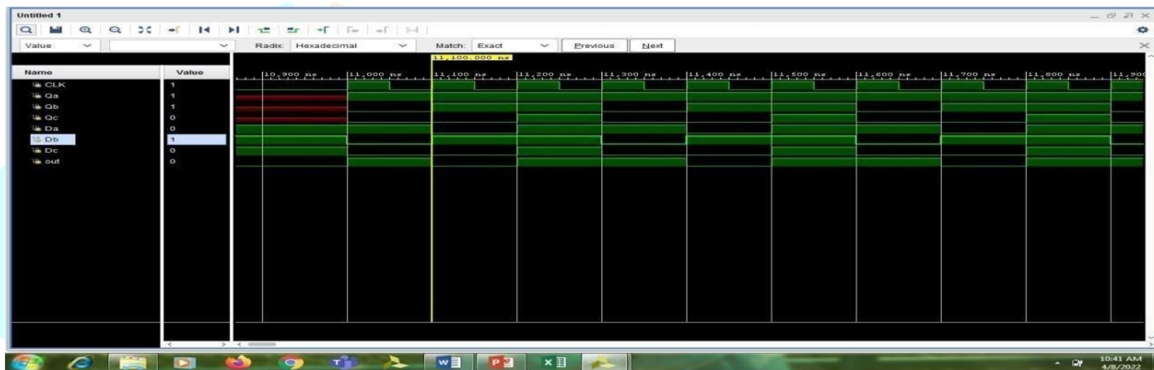

Figure vii . Simulation result of state skip LFSR Pattern

Editor - C:\Users\BIS\Desktop\lfsr code\output.txt
Untitled.m main.m output.txt

```
1 111
2 011
3 010
4 110
5 100
6 101
7 001
8
```

Command Window
New to MATLAB? See resources for Getting Started.

u =

5040

Figure vii a. MATLAB result of Reordered conventional LFSR Pattern

Figure vii b. MATLAB result of Reordered state skip LFSR Pattern

Power calculation of s27 benchmark sequential circuit is shown in Table viii. Column 1 and 2 shows the method used to compute power for conventional LFSR and state skip LFSR. Column 3 and 6 portrays the power value of circuit with unordered and reordered test pattern of both which is calculated using xilinx vivado tool.

CONVENTIONAL LFSR			STATE SKIP LFSR		
Method	Switching	Power	Method	Switching	Power
Before reordering	11	306.57mw	Before reordering	11	210.57mw
After reordering	6	167.22mw	After reordering	6	121.13mw

Table 4 Power calculation

Figure viii a. Simulation result of Reordered LFSR Pattern

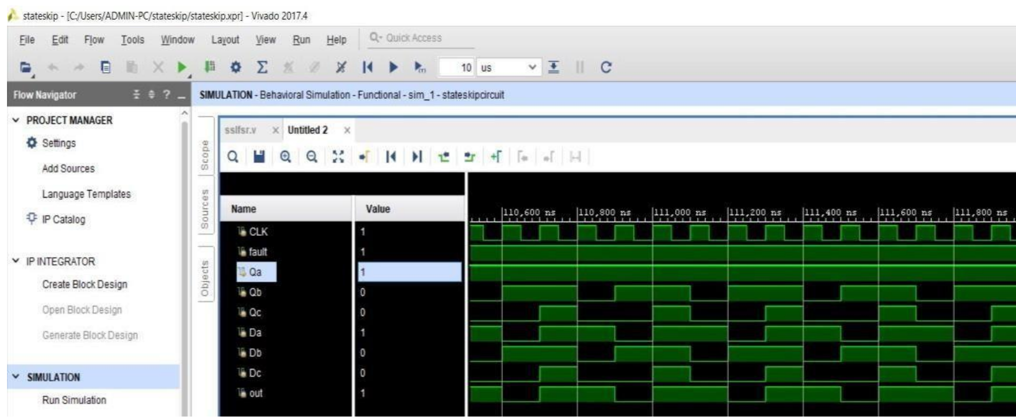

Figure viii b. Simulation result of reordered state skip LFSR pattern

VII. CONCLUSION

In this paper a compression method of state skip LFSR is implemented to decrease the number of test vectors. Reordering is efficiently done by modified prim's algorithm whereas repeated test vectors are neglected. Repetition of test vectors uses more delay and power hence this is the drawback of prim's algorithm used in literature work. Hence, compression technique is applied to reduce the number of test vectors applied and Prim'salgorithm is modified to generate test vectors with minimum switching activity results least power consumption.

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