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HIERARCHICAL DFT APPROACH FOR TESTABILITY

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Abstract: Modern chip designs, driven by rapid VLSI advancements, have become complex and compact, making post-fabrication testability essential for ensuring operational compliance. Design-for-Testability (DFT) techniques are crucial for fault identification after manufacturing, significantly reducing the need for exhaustive functional tests on numerous devices. DFT enhances controllability and observability across design nodes, facilitating effective error detection without extensive individual device testing. Among various DFT methodologies, the hierarchical approach is recognized for its efficiency in verifying manufacturing correctness. This method uses Automatic Test Pattern Generation (ATPG) to create test vectors from a block's netlist, aiming for comprehensive fault coverage with minimal time investment. By integrating compression logic, the number of generated test vectors is significantly reduced. Validation occurs at the block level to ensure compatibility with top-level pins through logical simulation, confirming timing and layout integrity. For blocks with inadequate coverage, a coverage analysis is conducted, followed by test point insertion to enhance coverage targets. The paper concludes with insights into future trends in DFT that can be utilized to improve coverage factor and have a greater yield along with Test point Insertion integration in DFT designs.

Index Terms – Design for Testability, ATPG, Coverage analysis, Test point Insertion, .

I. INTRODUCTION

The IC design cycle encompasses four key stages: specifications, design, implementation, and testing. During testing, Design-for-Testability (DFT) assumes a critical role in verifying chips post-fabrication. This is crucial because the manufacturing process isn't completely error-free, necessitating rigorous testing to ensure that each chip meets specified requirements. Leading industry practices employ a "divide and conquer" strategy, dividing the chip into distinct functional blocks. Each block undergoes independent ATPG targeting, generating test patterns tailored to validate every node. Validation of these blocks considers stringent timing constraints. Specifically, for a 6nm device, CADENCE tools are utilized to generate test patterns at the block level, ensuring thorough verification of functionality and performance.

Test coverage analysis is essential to attain adequate detection of stuck-at (DC) faults and transition (AC) faults as per specifications. Following this, the generated test patterns undergo validation using simulation techniques. Specifically, simulations are conducted using Modus, a tool by Cadence. The Waveform Generation Language (WGL) is employed for these simulations, which are subsequently translated into tester-specific formats for silicon testing. This ensures that the chips are thoroughly tested to meet quality and performance standards before deployment.

In each block of the design, scan flip-flops and combinational logic are integrated using scan stitching, which involves connecting Scan Input (SI) and Scan Output (SO) pins. These pins at the block level are aligned with corresponding top-level scan input and output pins through a process known as top-mapping. The decision on the length of the longest scan chain is based on the available input pins allocated for DFT purposes. This

determines how flops are stitched together within the design. Additionally, compression techniques are employed to minimize the storage requirements for test patterns.

DFT scan is a technique used in digital circuit design to facilitate the testing and debugging of integrated circuits (ICs). The DFT scan methodology involves modifying the circuit design by adding extra logic to enable the capture and output of internal states for testing purposes. The DFT scan technique involves dividing the circuit into a series of smaller units called scan chains. Each scan chain is made up of a set of flip-flops connected in a serial configuration, with additional control logic to enable the scan operation. The scan chains are used to capture the internal state of the circuit, which can then be output for analysis and testing.

Design for Test (DFT) methodologies aim to enhance the ability to control and observe internal nodes within a chip, thereby improving fault coverage. Controllability refers to how easily input pins can be manipulated by assigning binary values (0 or 1). It quantifies the ease of assigning values to primary inputs (PIs) in a circuit. Observability, on the other hand, measures how readily the circuit can detect and propagate node values to primary outputs (POs). Various DFT techniques have been developed to enhance both controllability and observability.

II. LITERATURE SURVEY

In the realm of semiconductor design and testing, achieving high testability is crucial to ensure the reliability and functionality of integrated circuits (ICs). Hierarchical Design for Testability (DFT) has emerged as a significant approach to address the complexities and challenges associated with testing modern ICs. This literature review explores the principles, methodologies, benefits, and challenges of hierarchical DFT in enhancing testability.

In paper [21], the author has described the challenges faced by using of core level scan chains without wrap ports. This may result in the reduction of run time and the test patterns power. The paper aims at test run time and test application power reduction. In this process the functionality of the block remains unaffected. The introduction of the various test modes in the hierarchical DFT approach is discussed. The conventional hierarchical DFT approach is used which reported high coverage detail and high performance of the chip at block level.

In paper [3], insertion of scan chains is explained. Scan chain technique is used to target both the combinational and sequential logic for controllability and observability. Various Automatic Test Pattern Generation tools are available for test pattern generation, post scan stitch process. The test patterns undergo validation by performing simulation methods and the patterns are reported as pass or fail, during simulation. Scan insertion at the lesser process technology results in increased yield of the chip.

Compression logic is the widely used architecture incorporated in DFT technique. In paper [10], compression technique is used. In this technique, the scan chains are connected in a pipeline and the output of the last scan flop in a scan chain is passed through XOR logic. This technique reports on the reduction of the test size and the test run-time, but the area of the chip increases by the inclusion of this design in the DFT region. There comes a need to optimize the area and power. Research on tradeoffs between the power consumed and area occupied is being carried out.

In recent times, low power scan pattern test is being practiced. Power consumption can be optimized by monitoring the switching activity of the scan flops. Paper [7] uses a power-aware approach which controls the power of scan flops during shift operation and capture operation. In this paper, the authors have introduced a new method which overcomes the drawback of low coverage caused by enabling only a set of scan Flip-flops to capture the test responses in a single pulse. This is done by simulated annealing method, which groups the similar combination of dependent flip-flop, also considering the impact of the clock trees. By implementing this method, power consumption during both shift and capture was optimized, with very less loss in fault coverage and no extra hardware overhead for at-speed test for transition faults.

In paper [6], Hierarchical DFT is the appropriate is widely used technique in DFT strategies. SoCs have various blocks at which ATPG will be carried to check for error free nodes. Top-mapping process – mapping of block level pins to device top pins is tedious work and automation needs to be incorporated. Thus, there might arise a need for regenerating the test patterns at block level to verify the generated patterns. This paper throws light on the recursive methodologies used to reduce the redundant fault count. Hence the silicon chip

fabricated reports increase in run time speed in terms of 10X. The coverage details at the block level show high performance.

In paper [22], the author presents the case study on the Hierarchical DFT technique, and describes the problems faced during insertion of the DFT logic in large System On Chip designs (SoC's). According to the author, Hierarchical DFT implementation gives alignment between the front-end and physical design process. The main purpose of this work is to reduce the at-speed run time of the chip. This was achieved on a design which had a gate count of around 4 million gates. This technique in DFT could decrease the scan pattern size and run time. The memory size of the tester is increased to incorporate the new hierarchical DFT approach. With this technique high quality coverage performance of the chip was noted.

In paper [17], the circuits are targeted for high-speed tests for the better performance of the circuits for at-speed. This paper comes with an effective technique which reports in reduction of test patterns during commit test technique, scan shift and capture operation, to control the switching activity of the scan input bits to reduce the power. The area overhead is also taken care of which reflects on the reduced cost of the chip. Three new techniques: launch-on-shift, launch-on-capture and mixed at-speed testing are proposed in this paper to support the low power and low-cost chip testing.

The author in paper [11], focuses on the challenges faced in meeting the area, cost, power and reliability in VLSI chips. Communication chips are upgrading at a very faster rate and are most important criterion to be met is low power consumption. There is rapid power dissipation during scan operation compared to the normal functional modes. To keep the power dissipation in check, a cost effective, BIST circuitry is designed which is reliable and supports low power. The BIST applies Multiple Single Input Change (MSIC) circuit at the testing phase. This technique targets the test patterns generated at BIST and the patterns are validated using logical simulation using Xilinx ISE simulator.

In paper [14], clock gating and non-clock gating structures are used for testing the device. Some modes used clock gating concept whereas the other modes ran with non-clock gating mechanism. The main aim was to reduce power consumption. By running various test cases and analyzing them, the author concluded that the modes with clock gating structure reported more test coverage compared to the non-clock gating modes. Run time was also found to be reduced when compared to the novel approach.

The chips that are used for medical purposes should be accurate and must be tested with great care. Paper [12], testing of chip which goes into medical industry is done. For the clinical diagnosis the chip is manufactured using lithographic techniques. But this method is not able to make the chip error free, hence it is not recommended to be implemented in the real scenarios. The author implemented hierarchical DFT approach to check the microfluidic chip. A chip with 1500 valves was taken as a test case and 100% test coverage was achieved using this DFT technique.

As the complexity of VLSI circuit is increasing, the engineers are facing many difficulties in automating the ATPG tools to perform DFT techniques. Therefore, the leading industries follow divide and conquer approach based hierarchical DFT technique for automation. Partitioning of circuits is the major problem in the VLSI design. A testing perspective for partitioning problem is discussed in this paper [15]. An automated tool which creates parallel testable VLSI circuits along with partitioning the combinational CMOS circuits is designed. The CAD tool is designed such that it gives a tradeoff between the test time and hardware overhead. As a result, it was seen that the vectors generated after optimization and partitioning had considerable reduction in length.

In paper [16], Built In Self-Test (BIST) is the ATPG technique used for testing. BIST is an internal circuit that undergoes several loops to make accurate scan tests and reduces the run time when compared to conventional methods. This type of testing can be used for the circuits that contain combinational blocks. This technique resulted in coverage improvement and reduced pattern size.

In paper [2], A Hierarchical DFT strategy is implemented to enhance SOC testability, partitioning the design into layout and DFT regions based on functionality. Using the D-algorithm for ATPG, it generates test vectors with Modus tools for 16nm technology, targeting high fault coverage (>99% stuck-at, >85% transition faults). Validation through IES simulations ensures accuracy before real silicon deployment, encompassing both block

and device levels with and without timing constraints. Pin-level mapping and logical simulations further validate effective test pattern application and integration across design hierarchy.

Advancements in SAT-based ATPG [4] for VLSI designs, focusing on D-chain enhancements to accelerate solving is discussed. Initially introduced to refine problem representations and limit search space, D-chains have evolved with incremental solving techniques. This study rigorously compares various D-chain strategies and introduces an innovative indirect D-chain approach with promising extensions. Experimental findings highlight significant runtime reductions based on the chosen D-chain method, offering insights into optimizing test pattern generation for complex VLSI designs.

Paper [8] introduces a novel approach to diagnostic test generation specifically for transition faults in full-scan sequential circuits. It leverages existing ATPG tools to distinguish between pairs of transition faults using launch-off-capture and launch-off-shift modes. The method ensures that generated diagnostic test patterns align directly with scan test patterns of the circuit, eliminating the need for pattern conversion. Experimental validations demonstrate the effectiveness of the proposed method across benchmark circuits, showcasing its capability to either differentiate indistinguishable faults or confirm their equivalence using standard commercial ATPG tools.

This study [19] addresses the critical issue of power reduction in at-speed testing of LSIs, particularly focusing on the Launch-To-Capture (LTC) cycle. Previous methods like X-filling have targeted IR-drop and power supply noise during the launch-off capture (LOC) scheme effectively. However, this paper introduces a novel X-filling technique, AP-fill, tailored for the launch-off shift (LOS) scheme. AP-fill surpasses traditional adjacent-fill methods by achieving superior LTC power reduction without compromising fault coverage or increasing test vector count, as demonstrated across significant ITC'99 benchmarks.

The challenge of balancing test quality and cost with power constraints in at-speed and faster-than-at-speed testing of VLSI circuits are addressed [13]. It proposes novel DFT mechanisms for launch-off shift, launch-off capture, and mixed at-speed testing to mitigate excessive switching activity and adhere to peak-power limits. By enabling design partitioning and power-aware utilization of optimized test patterns, the approach aims to maintain test effectiveness and minimize power consumption during launch and capture operations, crucial for preserving yield and reliability in semiconductor testing.

The demand for reliable automotive microcontrollers (MCUs) with complex SoC architectures is addressed by proposing a novel [9] approach to develop functional test patterns using Test Information Model (TIM). The method focuses on enhancing test coverage efficiently while minimizing development time and potential errors through automation. Results indicate significant time savings (60%-70%) compared to traditional simulation-based methods, demonstrating the approach's efficacy in improving pattern reusability and reducing overall test engineer workload. This advancement is crucial for accelerating time-to-market while ensuring high reliability in automotive MCU testing.

To enhance security against side-channel attacks in cryptographic integrated circuits (ICs), scan test methods [5] are commonly used despite their vulnerability. This study proposes bolstering traditional key and lock mechanisms with static obfuscation of scan data, altering certain scan cells' behavior during incorrect test key scenarios to confuse attackers. However, a newly identified test-mode-only signature attack (TMOSA) highlights the inadequacy of static obfuscation when plaintext is directly inputted, prompting the proposal of a dynamic obfuscation method. This approach cyclically shifts the incorrect test key during testing to dynamically obscure scan data, effectively thwarting TMOSA and other scan-based attacks. This countermeasure maintains high testability and low area overhead, offering robust resilience against modern cryptographic IC vulnerabilities.

Reducing average and peak power dissipation in scan chains during shift and capture cycles is crucial. The minimum transition count or adjacent fill algorithm effectively minimizes transitions, thus lowering average power consumption during shifting. Contrary to conventional views, statistical analysis of industrial circuits reveals high correlation between scan-in and scan-out vectors in adjacent fill scenarios. Leveraging this correlation, they introduced a new filling method termed bounded adjacent fill. This algorithm [20] generates test vectors that maintain low switching activity during both shift and capture cycles without affecting pattern count, offering a promising approach to optimize power efficiency in integrated circuit testing.

Paper [1] discusses an approach to enhance fault diagnosis and testability through the strategic insertion of test points, specifically as observation points. To identify optimal observation points, scores are calculated for signal lines associated with each fault pair that the existing test set fails to distinguish. Once the observation points are selected, the method organizes the primary outputs and the inserted observation points into groups, using XOR operations to compact the output responses within the same group. This partitioning strategy reduces the number of observed values while maintaining diagnostic effectiveness. The proposed approach is validated through experiments conducted on benchmark circuits.

III. CONCLUSION AND FUTURE SCOPE

The rapid evolution of VLSI technology has led to increasingly complex and compact chip designs, making post-fabrication testability essential for ensuring that devices meet specifications. Design-for-Testability (DFT) techniques are instrumental in identifying faults, significantly reducing the need for exhaustive testing across numerous devices. By enhancing controllability and observability, DFT optimizes error detection while minimizing testing inefficiencies.

The hierarchical DFT approach stands out for its effectiveness, utilizing Automatic Test Pattern Generation (ATPG) to create compact test vectors that ensure comprehensive fault coverage efficiently. Validation processes further ensure compatibility and integrity at the block level. When certain blocks fail to meet coverage expectations, targeted coverage analysis and test point insertion help address gaps, allowing for the achievement of desired testing targets. Overall, these strategies are crucial for maintaining the reliability and performance of modern chip designs in the competitive semiconductor landscape. Overall, the future of DFT and TPI in VLSI will likely be shaped by advancements in technology, increasing complexity, and the need for efficient testing solutions. Emphasizing automation, machine learning, and integration with broader design methodologies will be key trends.

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