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Design And Implementation Of CMOS Dual Stage Comparator And Oscillator For Path Delay Analysis

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***Abstract*—** In digital systems, the frequency of switching operations involved in internal transistors are high due to complex operations provided by the high demanding applications. The CMOS circuits with increased processing speed perhaps increase the leakage voltage, leakage temperature and leakage current in the transistors. Depends on the number of connectivity (the fan-in and fan-outs) the path delay is generated. The proposed system focused on testing the path delay variations on different circuits involving the reconfigurable comparator and fast frequency generating oscillator. The presented system involved with testing of on-chip performance at different frequency of operations. The reconfigurations are viable with simple tuning operations involved with XILINX XC95144XL device. The device work with 40 MHz operating clock with active low device reset. The configurable oscillator is implemented inside the device; hence the simulation is validated through XILINX ISE and Quartus II. The presented system achieved 3.89 ns latency in which 3.240ns as logical latency and 0.650ns as routing latency. The results are compared with existing state of art approach in terms of path variational delay.

Keywords— Low power design, Path delay, Digital circuits, Oscillator, Cmos design**.**

I. INTRODUCTION

Computing complex circuits involves several challenges, particularly in achieving statistically reliable outcomes within the required analysis window. Digital systems must undergo various levels of testing to evaluate complex competition models effectively. One primary issue in digital circuits is path delay variations, which depend on the circuit routing. The number of fan-in and fan-out controls connected to the core circuit impacts path delivery. In some applications, improper routing of clock signals to various nodes can leave circuits in an open-loop state, causing unwanted latency and errors in logical circuits. Additionally, switching events in digital systems can contribute to path delay variations.

The blockage of existing routes and the creation of new ones due to unknown logical elements further exacerbate these variations. To mitigate these issues, advanced techniques such as Principal Component Analysis (PCA) are employed to reduce system input complexity and computation time. Analyzing input and output parameters is crucial for making decisions on path delivery variation analysis.

To optimize partition space in device-to-device operations, the system matrix needs to be modified to create a correlated process. These modifications are then implemented in integrated circuits to test correlation performance based on computational circuits. In VLSI systems, path delay variations refer to differences in the propagation delay of signals from the source to the destination. Understanding and managing these variations is crucial for developing reliable circuits. Key considerations in the development of digital circuits include strategies to minimize delay variability, ensuring consistent performance and reliability.

Process Variation

Process variation plays a critical role at the manufacturing end, focusing on refining the semiconductor manufacturing process. This helps reduce the delay in transistor-based propagation right from the source node. Additionally, leakage current and leakage voltage generated by the transistors are minimized during production.

Intraday and interday variations are among the on-chip processes where different integrated circuits (ICs) are involved in interconnecting systems. These processes are used to check the performance of the integrated ICs with respect to path delay. Deviations are also associated with leakage voltage and leakage current in transistors interconnected within digital systems. Due to the high-speed switching of transistors, leakage current and leakage voltage are generated. The accumulated leakage current and voltage result in leakage power, which in turn increases path delays and latencies in digital systems.

Simple variations in path delay can lead to timing violations in the circuit's major clocks, affecting setup time and hold time relationships. This can ultimately cause incorrect behavior in digital circuits.

Design variability impacts the adaptable frequency of digital circuits, reducing their overall performance and speed. Power consumption is also affected, especially in major circuits involved in dynamic operations, where reduced switching activity can lead to additional transitions. Increased transitions in digital circuits result in unwanted leakage and glitches in stable clocks, causing operational variations in the circuits within the digital system.

II. BACKGROUND STUDY

Guo et al. (2020) The author presented a predictive framework in which path delay variation is analyzed using a backpropagation algorithm. To address various path delay problems from multiple aspects, a simple test circuit is developed using an on-chip mechanism. This test circuit is evaluated with the backpropagation algorithm by fetching various block signals from multiple corners of the system. By examining different performance measures and the patterns of performance in response to variations in clock pulses, the proposed circuit's response is thoroughly evaluated [6].

Papachatzopoulos et al. (2023) The author presented a simple modelling framework in which the maximum delay of density functions is analyzed. The maximum delay for supply voltages provided to critical circuits is determined for various reasons, allowing for comparative evaluation of nominal and abnormal path delays. This discussion includes a matrix-based path delay variation approach, where the system utilizes a multivariate probability density function [7].

Banerjee et al. (2021) The author presents a significant development in the analysis of statistical delay variations without the use of automatic test pattern generation for multiple benchmark circuits. This development addresses major issues typically managed by commercial tools, which often focus on conventional transitional fault testing using simulation screens with random variations applied to flexible circuits. The proposed methodology employs random variability analysis to test device performance, showcasing the efficacy of this innovative approach [8].

Javvaji et al. (2019) The author presents a system that analyses the probability of path delay by testing various faults provided in the process variations list of an algorithm. The system extends to circuits, analysing them by incorporating gate delay modelling and novel predictions of gate deviations. Correlations within each logical system are examined by providing path delay analysis using monitor simulation. This approach allows for a comprehensive understanding of path delay probabilities and their impact on circuit performance[9].

Sandhu et al. (2019) The presented approach considers compensator circuits for testing the sensitivity and delay variations of various applications. A major issue in digital integrated circuits is the generation of clock skew within the logic. This approach accounts for a maximum operating frequency range of 250 MHz to 1 GHz for testing path delay variations and conducting on-chip evaluations[10].

Considering various existing models developed for delay analysis, the presented system addresses major drawbacks identified in prior systems. These include complexities in architecture, the need for more specialized solutions in testing path delay variations, and challenges in tracking delays in complex circuits. Moreover, normalization of fan-in and fan-out controls is hindered by unwanted logical elements. To address these issues, the presented system adopts standardized circuits for testing and further evaluates path delay variations in the circuit. This standardized approach aims to mitigate the variational problems observed in previous systems.

Drawbacks in existing system includes, Complexity in architecture for testing the path delay variation. Tracking of delay is difficult, Fan-in Fan-out based delay is considered.

III. PROPOSED METHODOLOGY

In the proposed system, multi-voltage CMOS circuit such as dual voltage comparator, configurable oscillator etc. the test circuit is evaluated with multi-voltage fetched design and path delay is evaluated. The performance in terms of DC analysis is formulated through SPICE tool simulation, partial configuration of the Dual voltage comparator and Configurable oscillator are tested with XILINX XPE for power analysis and implemented using XILINX FPGA device.

Advantages of proposed system, multi-voltage multiple frequency is applied to test different CMOS circuits. DC analysis is made and tested with path delay.

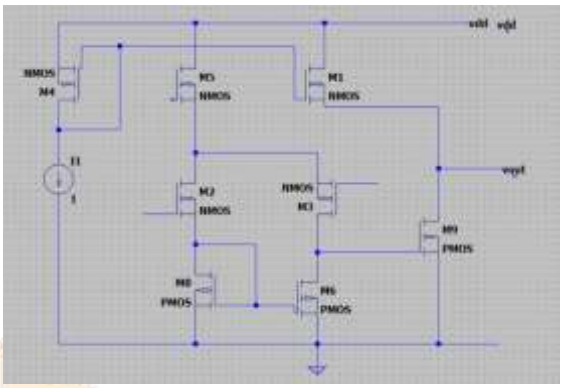

Fig 1. CMOS dual stage comparator

Fig 1. Shows the CMOS dual stage comparator developed using LT-SPICE tool. The design circuit consists of CMOS transistors developed with PMOS and NMOS combinations of configurable nodes utilized for manual and automated testing modes. The input voltage is compared with the reference voltage through reference nodes connected to the NMOS transistors. The dual stage comparator is developed by cascading the comparator circuits together as the output of one circuit is connected with the input of another circuit. The dual stage comparator enhances the precision and potential of the reference clock input. The leakage voltage in the transistor junctions is managed through intermediate resistance circuits. In the first stage, the input voltage is compared with the reference voltage tuned up and fetched into the next stage. The final voltage received at the cascaded comparator block is utilized for final decision making of voltage comparison. The dual stage comparator produces results opted with enhanced speed, accuracy, power efficiency applicable for most of the analog to digital converters. In various sensor interfaces, the need for accurate comparator is increased. The high speed and reliable comparator result precise voltage comparisons.

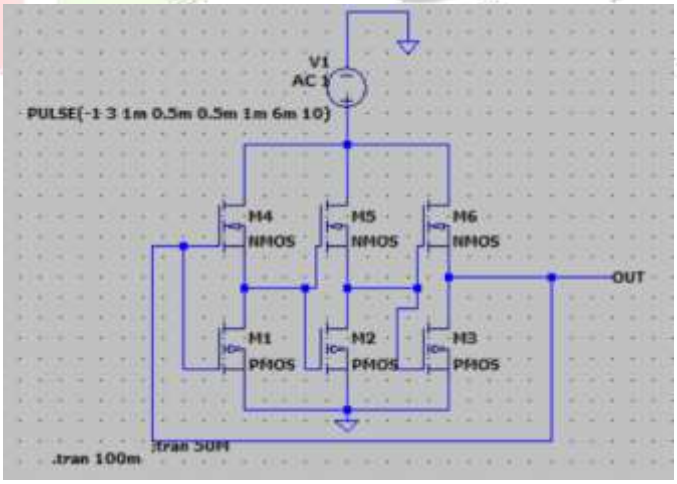

Fig 2. Configurable CMOS oscillator

Software implementation summary

There are two design strategies are implemented as far the simulation part is concerned. The conventional method is implemented using MODELSIM 6.3g Altera Software, the analog performance and characteristics is developed using LT-Spice tool. The Voltage -Current characteristics towards the configurable oscillator as well as the trigger output of the comparator is simulated. The spice tool is automatically formulated to the required design constraints to show up the simulation.

Hardware implementation summary

The proposed system with hardware implementation is developed with XILINX XC95144XL hardware. The kit consists of numerous input output ports connected with jumpers to access the logic flow of the chip.

The global clock is connected with 40MHz crystal oscillator which produces stable clock pulses. The global reset is connected with reset switch set up provided with a jumper wire.When the digital hardware get switched ON, the continuous flow of stable clock pulses are generated and provided to the FPGA IC.

The proposed system consists of low power configurable oscillator circuit implemented inside the chip.the configuration bits are connected to 4 bit I/O ports. These bits are tuned from “0000” to “1111” to provide configurable clock output. Similar way the output of the oscillator is connected to the LED set up to show up the clock signals. The signals are further tested with digital storage oscilloscope for frequency measurement. The frequency generated from the oscillator ranges from 600Hz to 20 MHz based on the configuration bits.

The hardware implementation provides the justification for synthesized architecture developed using the low power configurable CMOS comparator and CMOS dual stage oscillator circuit for path analysis.

IV. RESULTS AND DISCUSSIONS

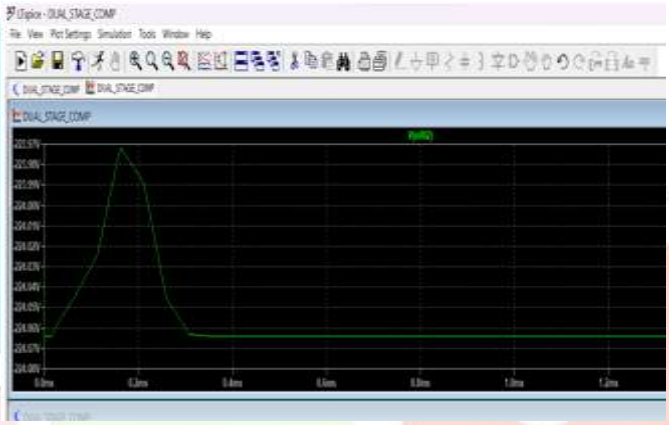

Fig 3. Comparator trigger output

Fig 3. Shows the comparator result showing the voltage get maximum trigger after the dual stage operation. The proposed model simplifies the design process involved in high precision comparators, replacing the dual stage comparator with decision making circuit itself. The reconfigurable comparator have the capability to adjust the voltages accordig to the demand of real time applications, dynamically through simple low power operations.

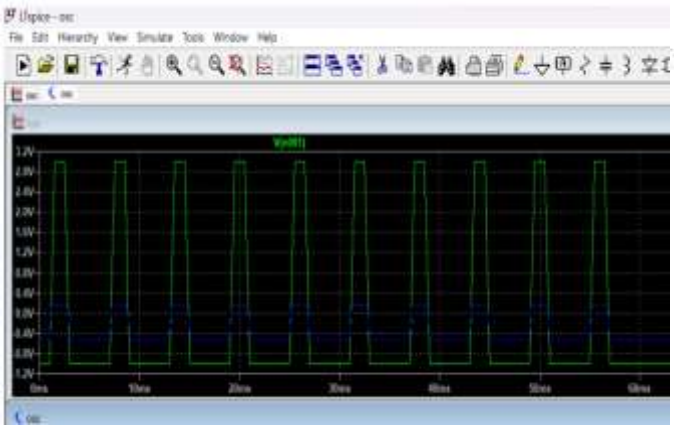

Fig 4. Configurable oscillator output

Fig 4. Shows the oscillator output, in which CMOS three stage inverter circuit based operation is developed. The path delay between the eeach inverter is limited hence the variations are suppressed here.

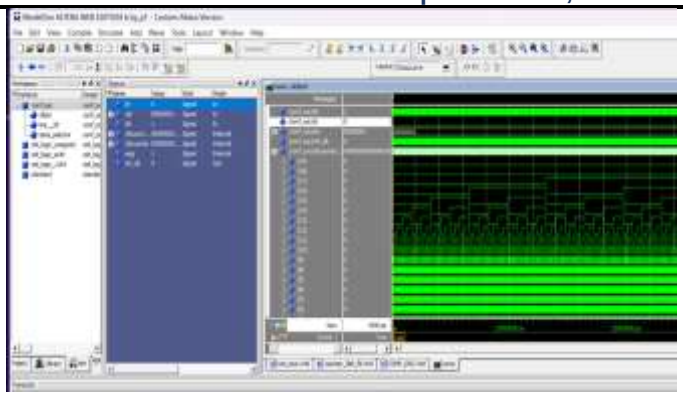

Fig 5. Conventional Dual stage comparator result

Fig 5. Shows the simulation result of conventional comparator design using RTL simulator. Mentor graphics tool is utilized over here for the purpose of test, verification of RTL codes towards the digital test circuit.

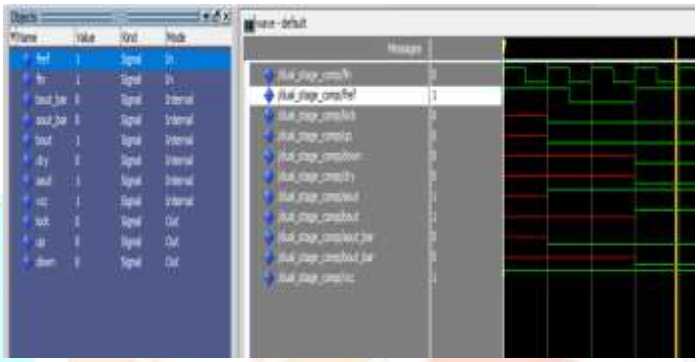

Fig 6. Conventional Comparator trigger part

Fig 6. Shows the conventional comparator result showing the two frequencies fin and fref is compared. As the initial part of the conventional comparator have undetermined state since the comparator is not dynamically modelled as well.

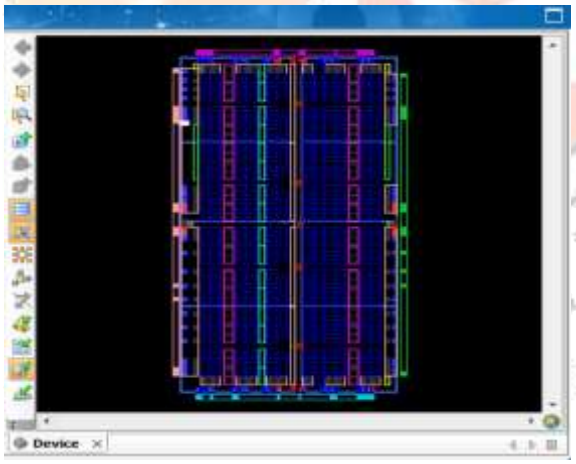

Fig 7. Chip modelling

Fig 7. Shows the pin assignment of proposed method towards the development of configurable comparator and oscillator circuit.

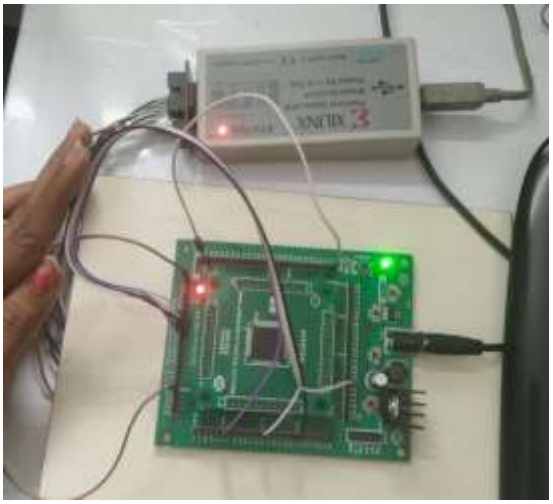

Fig 8. Hardware implementation

Fig 8. Shows the integrated hardware implementation of proposed configurable oscillator circuit using XILINX XC95144XL device. The device work with +3.3V input and output voltage ,with operating frequency of 40MHZ generated from stable crystal oscillator. The configurable oscillator circuit adjust the operating frequency by tuning the clock tree synthesizer. The clock synthesizer is connected with 4 bit hardware switches hence, the logic low is provided by connecting the wire with GND, logic high is provided by connecting the wire with +3.3V DC.

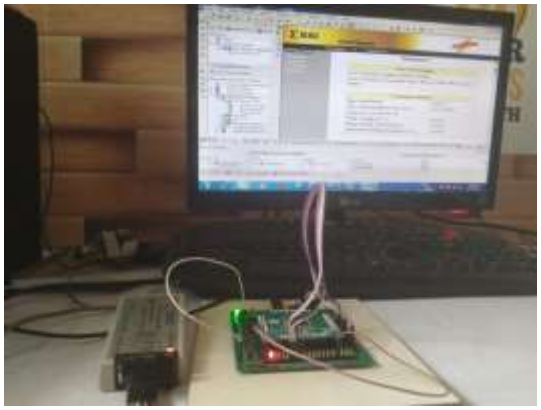

Fig 9

Table 1. Latency Report

Sl. No	Metric	Latency in ns.	Latency in %
1	LOGICAL DELAY	3.240 ns	83.3%
2	ROUTING DELAY	0.650 ns	16.7%

Table 1. shows the latency report of the proposed work in which the logical delay of 3.240ns is achived with routing delay of 0.650ns is achieved.

Table 2. Comparative path variations summary

Sl. No	Reference.	Path Variations	Method
1	PROPOSED APPROACH	3.89 ns	Conf. Oscillator
2	EXISTING SYSTEM	10.00 ns	Monte Carlo

Table 2. shows the comparative path variations summary. The proposed approach achieved 3.89ns comparing with the existing state of art work achieved 10 ns for monte carlo simulation.

V. CONCLUSION

The implementation of the configurable oscillator circuit has been successfully achieved using partial FPGA configuration on the XILINX XC95144XL device. The primary objective was to validate that the proposed system is synthesizable with low power consumption while maintaining efficient performance metrics. The synthesized design demonstrates a commendable logic implementation latency of 3.240ns, complemented by a routing latency of 0.650ns. These metrics indicate a highly efficient design, optimized for minimal delay. Furthermore, the entire system operates at an impressively low power consumption of just 1mW. This low power usage underscores the effectiveness of the design in terms of energy efficiency, making it suitable for applications where power conservation is critical. In conclusion, the proposed configurable oscillator circuit not only meets the functional and performance requirements but also excels in achieving low power consumption, thus validating the feasibility and efficiency of the design.

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