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# IMPLEMENTATION OF ARITHMETIC LOGIC UNIT USING QUANTUM DOT CELLULAR AUTOMATA

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***Abstract:*** In the domain of digital computing, the quest for higher performance, energy efficiency, and miniaturization has driven the exploration of alternative technologies to overcome the limitations of traditional Complementary Metal-Oxide-Semiconductor(CMOS) technology. Quantum Dot Cellular Automata (QCA) has emerges as a promising candidate for revolutionizing the field of digital circuits, offering the potential to push the boundaries of speed and power efficiency.

Arithmetic Logic Unit, also known as ALU, is responsible for carrying out logical and arithmetic operations based on the input operands. The proposed Arithmetic Logic Unit is fed input through layering, which results in reduced occupation area and cell count. It consists of half adder and NAND gate followed by two 2 x1 Multiplexer. The proposed design of a half adder and NAND gate (used for And operation) uses less space, less cells, and low energy dissipation than the existing design.

***Index Terms*** - QCA – Quantum Dot Cellular Automata, QCA Cell, QCA Designer, ALU – Arithmetic Logic Unit.

## I. INTRODUCTION

The emerging technology of Quantum-dot Cellular Automation (QCA) utilizes novel paradigms like synthesizing reversible gates. QCA is a construction nano electronic technology that gives another approach to computation at nano level. Boolean logic functions can now be implemented in QCA designer thanks to the improvements in QCA and enhancements. The use of QCA in digital circuits for quantum mechanical effects results in a significant reduction in size and area and achieves high speed operation at very low power levels. Hence the neighbouring cells interacts with each other the state changes happened in QCA due to electrostatic or magnetic fields. Consequently, in QCA, electron localization is used to represent binary values in quantum

dots, instead of using ranges of voltages and currents in traditional computers. Large number of QCA integrated circuits are designed and implemented in densities up 1014 cells/cm2 and there is a rapid increase in circuit switching frequency which is almost close to a terahertz. QCA is an array of cells, each cell carries the binary information and the transfer of information flow is possible by the Coulombic interaction between cells. Generally CMOS technology based on combinational circuit consist of AND,OR,NAND,NOR and INV logic primitives while QCA circuit consists of main logic primitive Majority Voter(MV).

## II. SOFTWARE IMPLEMENTATION

### QCA BACKGROUND

Quantum-Dot Cellular Automata to introduce classic cellular automations with quantum dots. Quantum dots are nanoscale structures, constructed from semiconductors such as Gallium Arsenide (GaAS). The QCA circuits comprises of quantum cells which further consist of four quantum dots. The fabrication of circuits in QCA is done using quantum cells, and each cell contains two electrons. The transfer of information is accomplished through the change in polarization state rather than electrons flow in CMOS, which further reduces power dissipation, delay and increases equipment density.

A small number of QCA-based arithmetic and logic units have been proposed so far. Our project involves simulating an Arithmetic Logic Unit that includes a Half Adder and Nand gate.

### QCA CELLS

A QCA cell is a nano structure with four quantum dots as illustrated in fig.1. A QCA cell is the basic building block of QCA- based computing system. Two electrons and four quantum dots are present in each QCA cell, and because of Coulomb interaction between these identical charges, they occupy the dots in a diagonal way. As a result, the two stable polarization states for a QCA cell have been achieved, the instantaneous polarization of a cell is denoted as either '-1' or '+1'. Which is encoded to represent a binary '0' value and '1' value, respectively in fig.2(a) and 2(b).

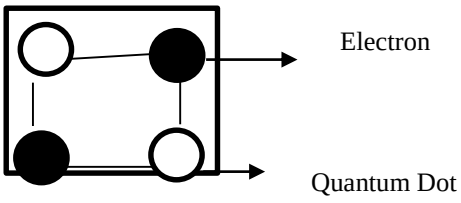
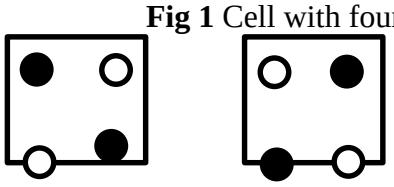



**Fig 1** Cell with four Quantum Dots

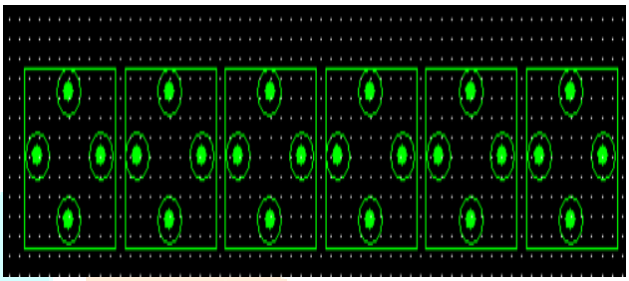


**(a)** **Bina**ry 0 (P= -1) (b) Binary 1 (P = 1)

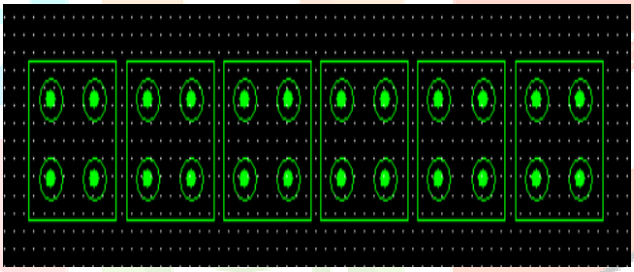
**Figure 2** Quantum Cells with Polarization

**QCA WIRE**

An array of identically polarized cells that transmits a signal from one end to the other is called a QCA wire. Fig.(a) depicts the signal propagation utilizing the 45◦ wire, also referred to as the inverter wire, and the 90◦ wire, referred to as the normal wire,Fig.(b).Since the signal in a 45◦ wire is always reversed, there needs to be an odd number of neighboring cells between the input and the output cell in order to transfer the original input signal to the output end.



(a)



(b)

proposed system overview is that it allows the user to upload the image of the food and it display the calories, Macro Nutrient values of that food and also Recipes of that food image. The food recognition will be done by using CNN Model Architecture which is MobilenetV2.MobileNetV2 uses convolution layers to extract hierarchical features from input images. Different levels of abstraction are covered by these features, with simple edges and textures being the first, followed by more complex patterns like shapes and object parts. The knowledge gained from training on a large dataset can be leveraged by using MobileNetV2 as a pre-trained model. The calorie estimation and other nutrient values will be acquired through USDA Food Data Central API .Natural Language Processing is used for displaying the dishes based on the given input image. NLP techniques such as text preprocessing, feature extraction (using Count Vectorizer), and cosine similarity calculation are employed to analyze the textual information (ingredients) associated with dishes. This analysis enables the system to display dishes that closely match the user's input based on ingredient similarity.

**MAJORITY GATE AND INVERTER GATE**

Two states of QCA cells are available to begin with is 900 normal cells and the other is 450 rotated cells. In QCA, basic logic elements are inverter and a three-input majority gate. An inverter is made by situating cells diagonal to each other to accomplish the reversal functionality and example of inverter gate is shown in Fig (a).

A basic three input cells of majority voter will decide the polarity of the center cell and the output is obtained is the majority voted polarity. Majority gate is the universal gate of the QCA logic. It can be used as AND or

OR gate by fixing the input polarity of one input to +1 or respectively. A basic three-input majority gate as shown in Fig(b).

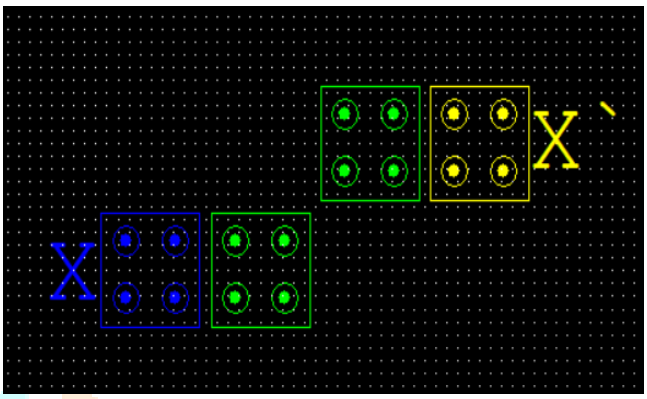



Fig (a). Inverter Gate

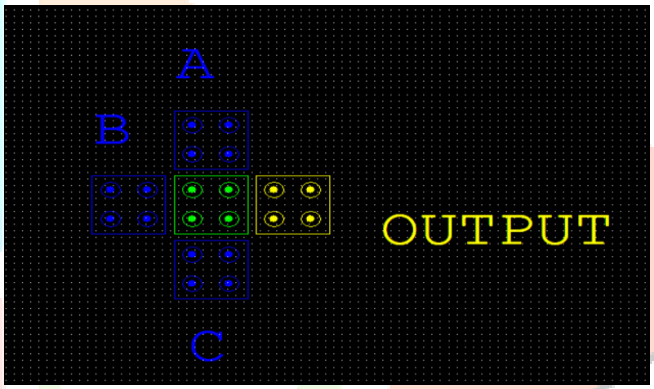



Fig (b). Majority Gate

**QCA CLOCKING**

QCA circuits require clocking to function properly. The transitions between quantum dot states in QCA cells occur due to potential barriers that are controlled by the QCA clock. The clock raises and lowers these tunneling barriers, regulating data flow and providing power. The QCA clock has four stages that correspond to the tunneling barriers above it. First, the barriers start to increase. Once high enough to prevent electron tunneling, the second stage begins, next the high barriers decrease in third stage. Finally, in the fourth stage, the lowered barriers allow electrons to tunnel freely again. In summary, the high clock signal enables electron tunneling while the low clock signal latches the cell, show in the Fig.

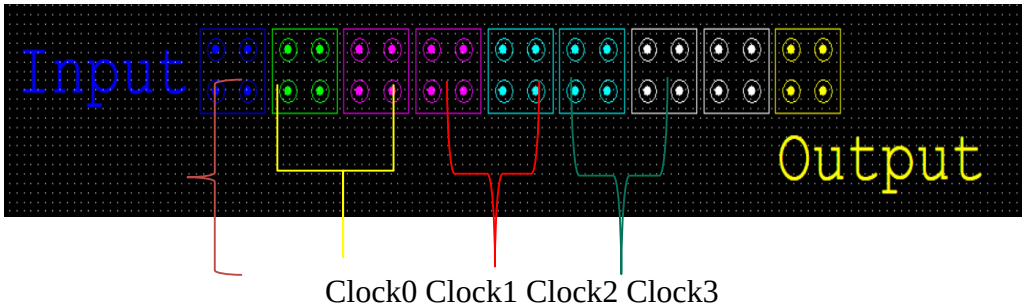



Fig. QCA Cells with different Clocking

### CLOCKING ZONES

The A single QCA cell functions as a wire that can compute and store data. Information is processed and transmitted via a wire that is made up of a cascade connection of QCA cells. An external clock is utilized to govern the signal transmission.[10] Hold, Switch, Relax, and Release are the four clock zones into which QCA circuits are divided. As the clock zones progress, there is a 90-degree phase shift.

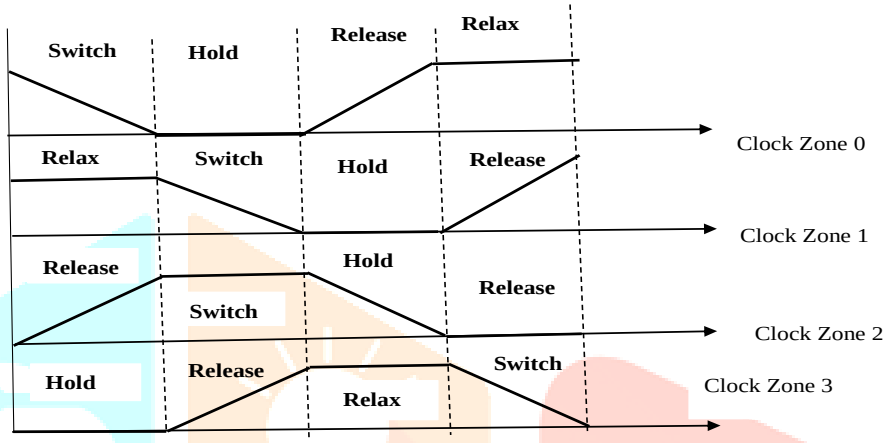



Fig. Clocking Zones in QCA

## III. PROPOSED SYSTEM

### ALU BACKGROUND

An ALU stands for Arithmetic Logic Unit, which carries out logical and arithmetic operations based on the input operands. Arithmetic operations are broken down into addition, subtraction, multiplication, and division. Whereas logical operations consist of AND, OR, and NOT. By implementing ALU in QCA, there are improvements in parameters like area, cell count, and power dissipation compared to CMOS, a transistor based technology.

### UNIVERSAL GATES

There are two types of Universal gates, NAND gate and NOR gate which can be connected to create Inverter, AND gate and OR gate.

NAND Gate

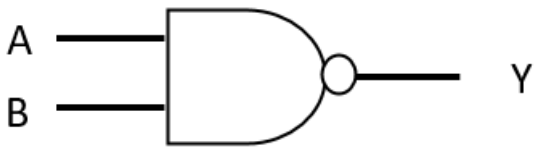



Fig. NAND Gate

Table 1 Truth Table of NAND Gate

| A | B | NAND |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

NOR Gate

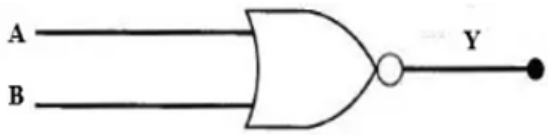


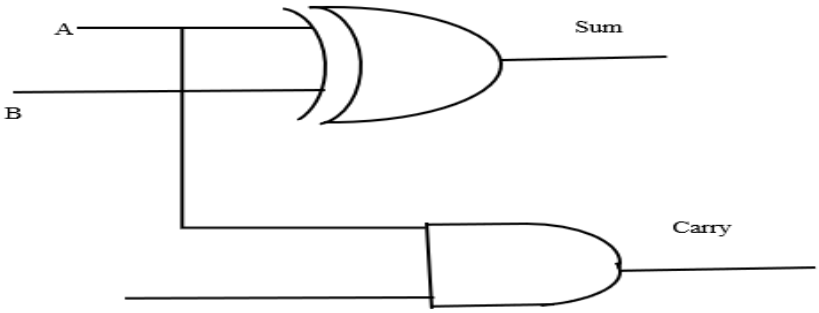

Fig. Logic Diagram of NOR Gate

Table 2 Truth Table of NOR Gate

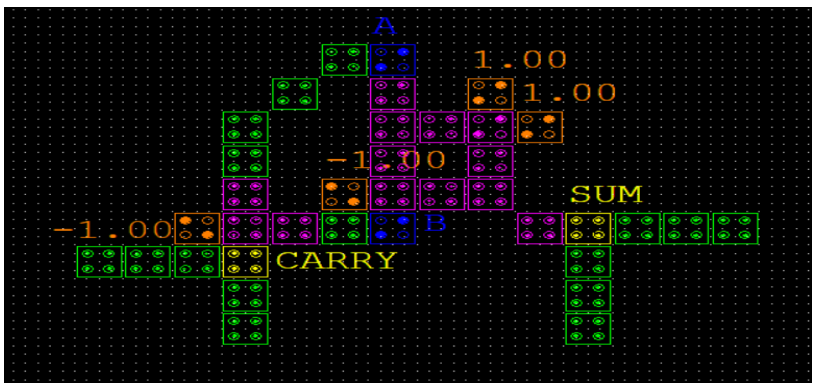
| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

## DESIGN HALF-ADDER AND HALF-SUBTRACTOR

A half adder performs the addition of two Boolean variables and gives two outputs, one is sum and the other is the carry. Let A and B be two input variables. The basic building block proposed consists of two MV gates and NOT gate. One of the MV gates functions as an AND gate, while the other functions as an OR gate. Then the sum and carry is respectively given by




(a)



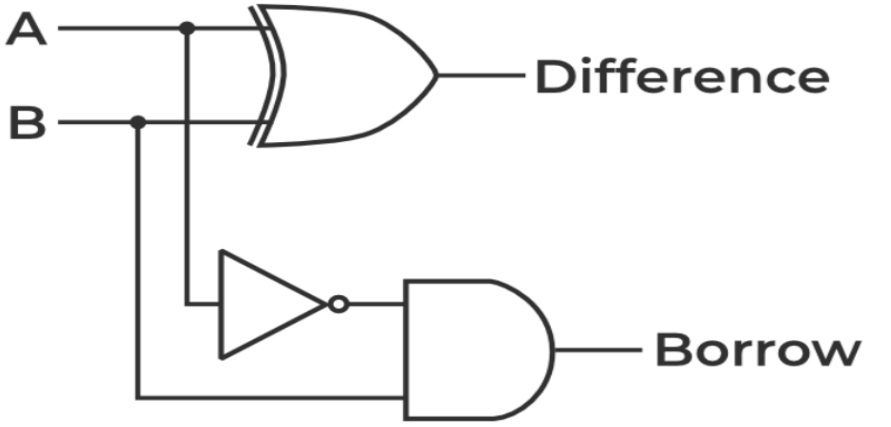

(b)

Table 3 Truth Table of Half-Adder

| Inputs | | Outputs | |
|---|---|---|---|
| A | B | Sum | Carry |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

## HALF SUBTRACTOR

A half subtractor performs the subtraction of two Boolean variables and given to outputs. One is Difference and the other is the borrow. Let A and B be the two input variables. The basic building block consists of two MV gates and one NOT gate.




(a)


(b)

Fig. (a) Logic Design of Half Subtractor (b) Half Subtractor Design in QCA Designer

Table 4 Truth Table of Half Subtractor

| A | B | DIFF | BORROW |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |

## 2X1 MULTIPLEXER

A 2X1 multiplexer is a digital circuit that selects one of the two input signals and forwards it to the output based on a control signal. It hat two data inputs i.e A and B, one select input and the other is Output. The select input determines which data input gets passed to the output.

which data input gets passed to the output.

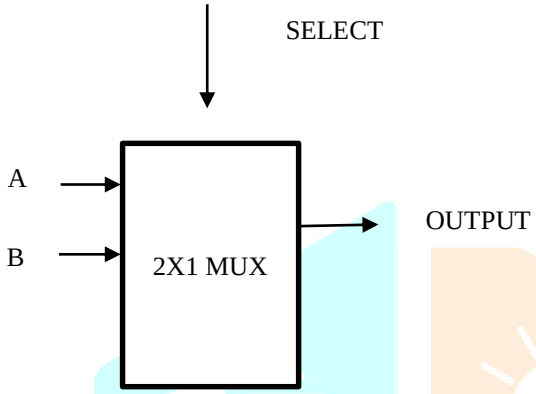



Table 5 Truth Table of 2X1 Multiplexer

| S | A | B | Output |
|---|---|---|---|
| 0 | 0 | X | 0 |
| 0 | 1 | X | 1 |
| 1 | X | 0 | 0 |
| 1 | X | 1 | 1 |

## QCA IMPLEMENTATION OF ARITHMETIC LOGIC UNIT

QCA Designer has been used to create a Arithmetic Logic Unit. QCA Circuits can be designed and simulated using this software tool. The blue and yellow cells are the input and output cells, respectively. The orange cell is of fixed polarization as shown in the figure.

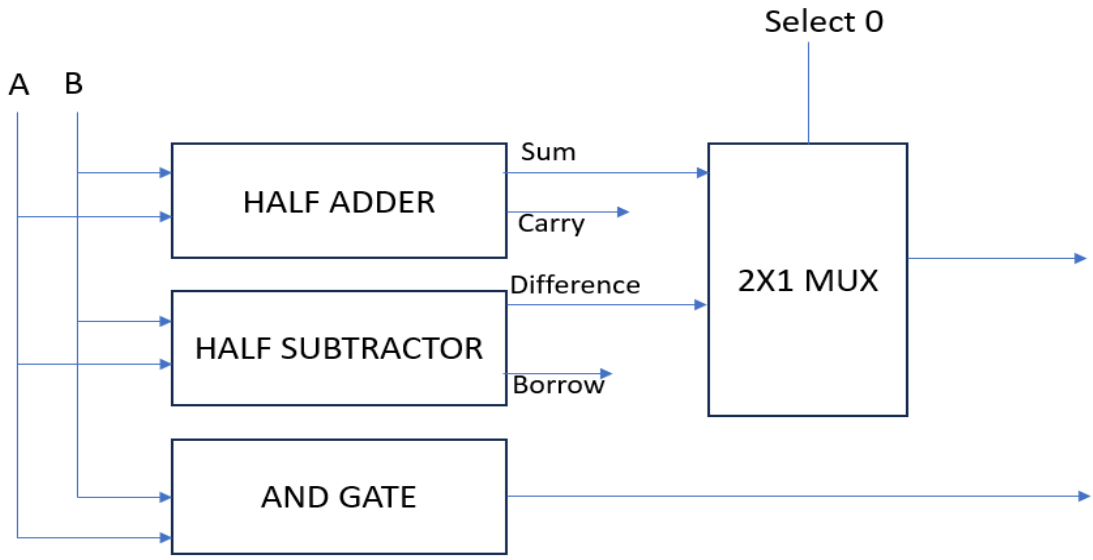



Fig. Block Diagram of ALU

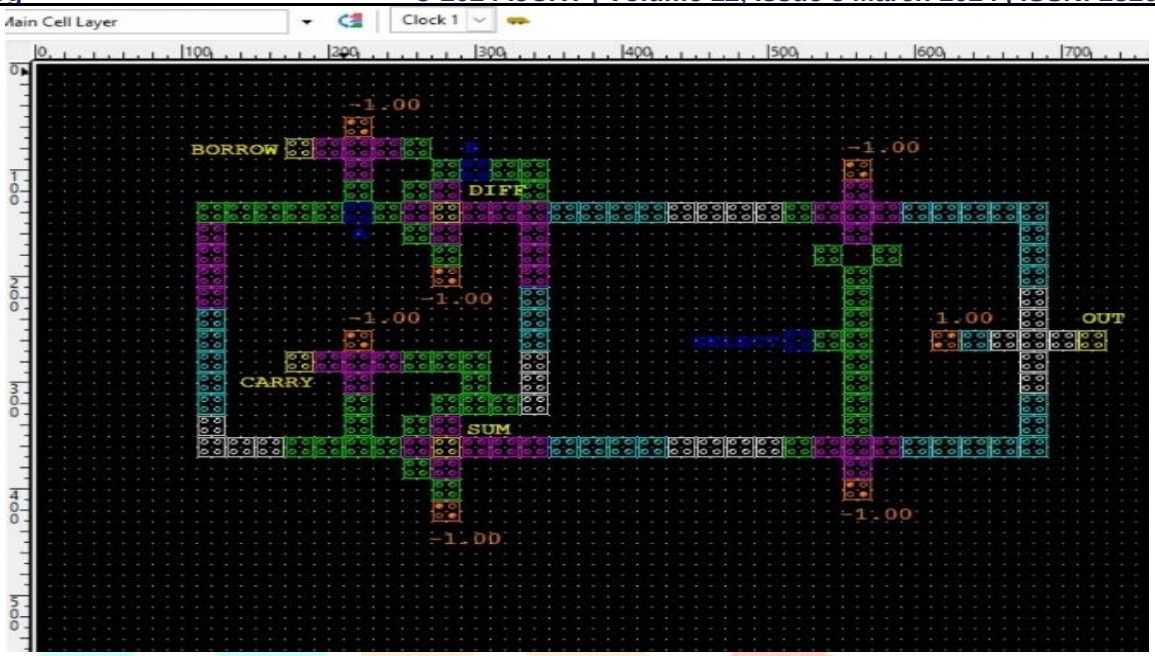



Fig. ALU Design in QCA Designer

## XII.SIMULATION RESULTS

The simulation results of all the circuits tested are represented in the below graphs of , Half Adder, Half Subtractor and Arithmetic Logic Unit.

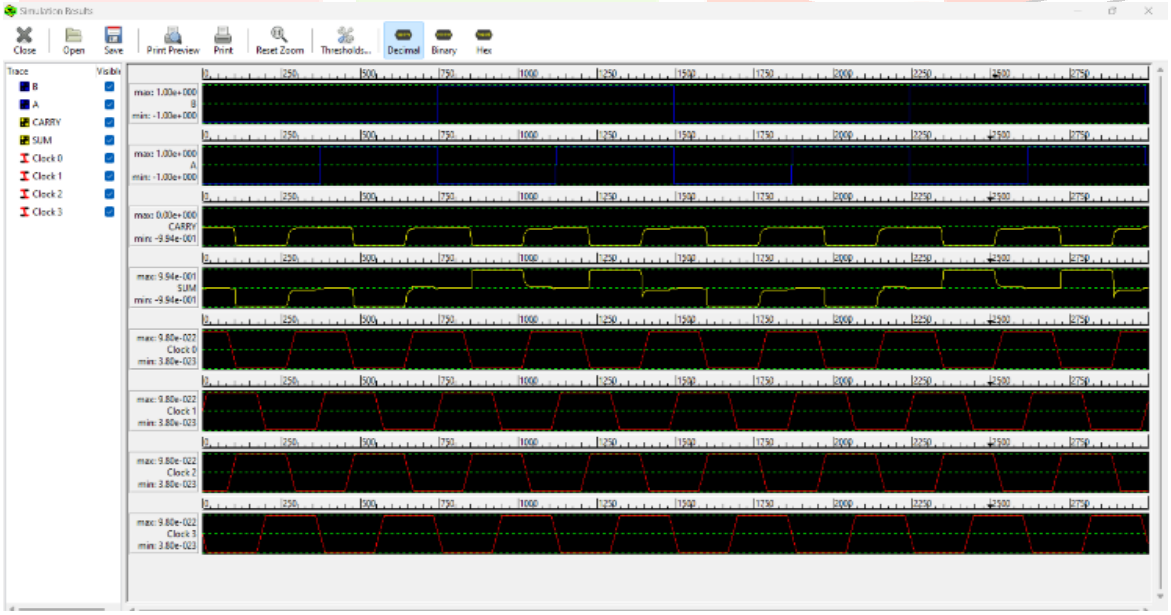



Fig. Half-Adder Simulation Result

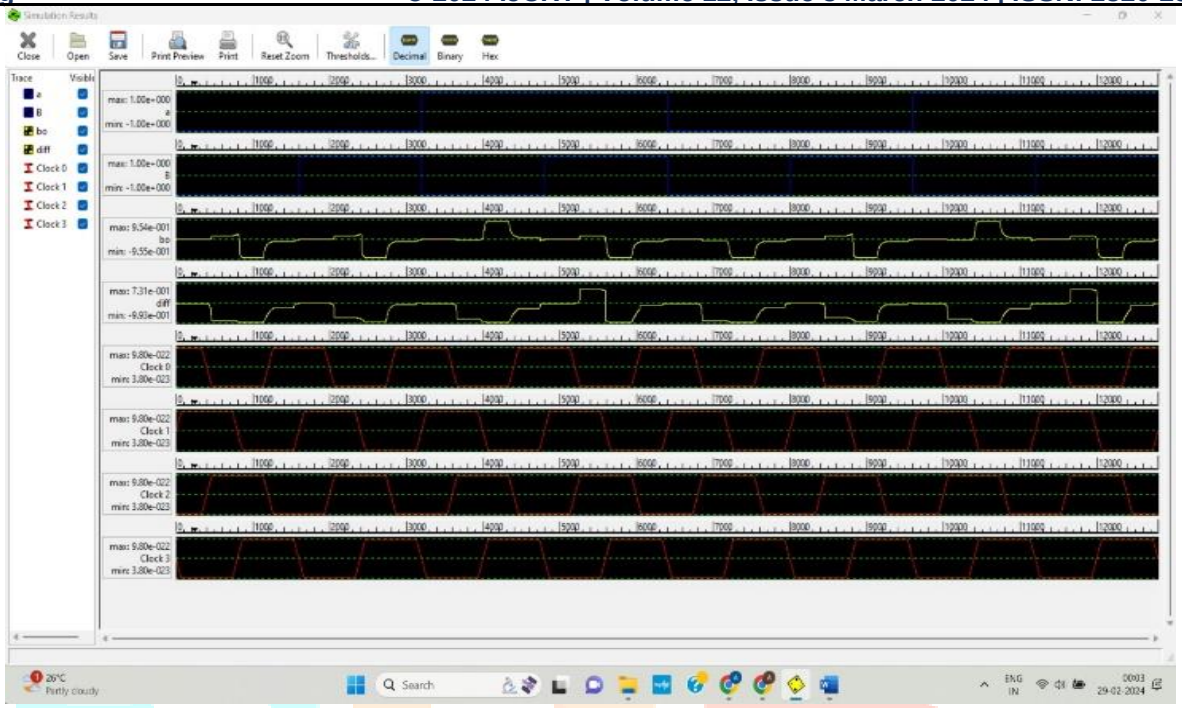


Fig. Half-Subtractor Simulation Result

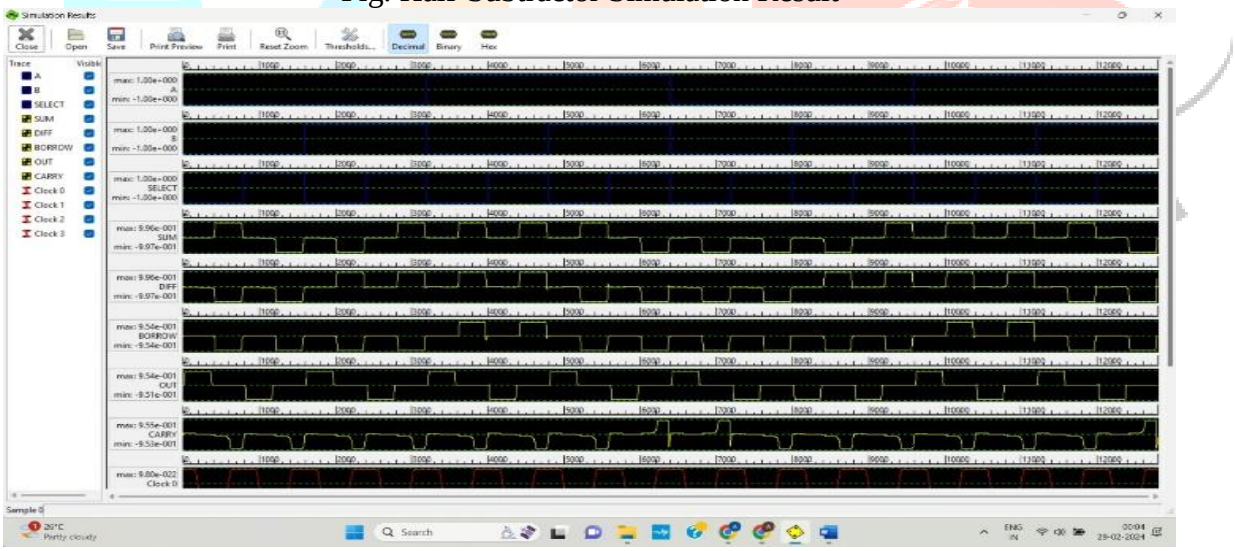


Fig. Arithmetic Logic Unit Simulation Result

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