IJCRT.ORG ISSN : 2320-2882

INTERNATIONAL JOURNAL OF CREATIVE RESEARCH THOUGHTS (IJCRT)

An International Open Access, Peer-reviewed, Refereed Journal

A SERVEY ON APPLICATION OF VEDIC MATHEMATION IN COMPUTER SCIENCE

Ajay Kumar[1st]
Assistant Professor of Mathematics
Dr. C.V. Raman University, Vaishali, Bihar
Dr. Sushil Kumar Jamariar[2nd]
Associate Professor & HOD
Department of Mathematics
Dr. C.V. Raman University, Vaishali, Bihar
Vijayendra Kumar[3rd]
Student of M.Sc.(Mathematics)
Dr. C.V. Raman University, Vaishali, Bihar
Santosh Singh[4th]
Student of M.Sc. (Mathematics)
Dr. C.V. Raman University, Vaishali, Bihar

Abstract

Vedic Mathematics is used by several researchers in the field of digital signal processing , chip designing, Discrete fourier Transform, High speed low power VLSI arithematic and algorithm , RSA encryption system. Veda is the store house of Knowledge. Hence Vedic Mathematics has a much ancient origin throgh attributed to the techniques rediscovered between 1911 & 1918 . Now a days interest in Vedic mathematics is growing in the field of computer science where researchers are looking for a new and better knowledge to the subject .

Even for eign researcher's are said to be using this ancient technique for implementation of fast algorithms.

In this paper we are going to overview of this ancient technique used as well as computer science. Whenever we many Vedic sutras are used in multipliers unit of computer science. It will gone very faster result which is required in cryptographs. Algorithm image processing application for example Ekadhiken purvena and Ekanyainen purvena, sutra use in $i < -i + 1$ & $i < -i - 1$ in software routinse.

Kew words – Vedic Mathematics, Nikhilam Sutra , Urdhwa tiryabhyam, RSA algorithm , image processing , Dhavasankasutra, Parvartya Sutra.

1. Introduction Sri Bharati krishna Tirtha ji (1884-1960) rediscoved, the Indian Sanskrit texts Between 1991 and 1918, [1]

Veda means the store-house of all knowledge.

Vedic Mathematics is based on sixteen sutras or principles. In practice many application of These Sutras may be learned and useful. To solve actual problems. Beauty of Vedic Mathematics lies in the fact that at reduces otherwise cumbersome Looking Calculation in Conventional mathematics to a very simple area [2]

This is a very interesting field and presents Some effective algorithm which can be applied to various branches of engineering Such as Computer, VLSI implementation and digital signal processing. In this paper we overview Nikhilam Navada charanam Dashatah, Urdhwa- tiryakbhyam

2. Vedic Mathematics Sutra

Sri Sathya Sai veda Pratishthan has Complied K. 16 Sutra and 13 Sub Sutra[] In the field of Engineering maximum researchers uses The Sutra Nikhilam Nevada Churanam Dashatah and Urdhwa-Tiryakbhyan

2.1 Nikhilam navada charanam Dashatan This means all from 9 and the last from 10. The algorithm has its best Case in multiplication. Of numbers, which are nearer to bases of 10, 100, 1000 etc. The pod due of multiplication using the Nikhilam involves minimum mental manual calculation which in terms will lead to reduced number of steps in Computation reducing the space, Saving more time for Computation The numbers taken Can be either less or more then the base considered Here is Survey of Different Multiplier Design using Vedic math

S.N	Title of Paper	Publisher& year	Method / sutras From veda	Features	Language or tool
1.	Binary Division Algorithm and High speed Deconvolubun Algorithm	IEEE 2014	Nikhilam Parvarty sutras	Applied for calculating deconvulate reduced time delay and Complexity	VHDL and Xilinx ISE
2.	Multiplier design based on ancient Vedic Mathematics	IEEE 2008	Urdhva Tirgakbhyam Nikhilam	Faster Multiplier and Square krchiteeture delay and design area less	ALTERA cyclone II FPGA
3.	Vedic mathematics Based Multiply Accumulate unit	IEEE 2011	Urdhva Tirgakbhyam	Binary number multiplication Realized easily on silicon due to regular and parallel structure	VHDL and Xilinx ISE
4.	Design a DSP operation using Vedic Mathematics	IEEE 2013	Vedic mathematics based DSP require less processing	Low on chip area and high speed	Mat lab

			time then inbuilt MATLAB pureness gives better result		
5.	Novel Architecture Inverse max Columns for AES using Ancient Vedic Mathematics FPGA	IEEE 2009	Urdhva Tirgakbhyam Advanced encryption standard (AES)	Low on chip area and high speed	Xilinx

2.4 Let us consider two n-bit numbers a and b to be multiplied. Then Their Components Can be represented as a^n = 10-a and $b^n = 10^n - b$ The product of two numbers Can be giren as p = (ab). Now a factor $10^{2n} + 10^n (a+b)$ is added and Subtracted on the right hand side of the product equation which can be exposed Mathematically as

$P = ab + 10^{2n} + 10^n (a+b) - 10^{2n} - 10^n (a+b)$ on Simplifying, we have

$P = \{10^n (a+b) - 10^{2n}\} + \{10^{2n} - 10^n (a+b) + a\}$

$= 10^n \{(a+b) - 10^n\} + \{(10^n - a)(10^n - b)\}$

$= 10^n \{ (a-b) + (ab) \}$

Form this equation. we Con derive the left hand side of the product as $(a-b_1)$ or $(b-a_1)$ and right hand Side as (a_1b_1).

The basic equation in the algorithm for a given set of numbers are as follows

Now consider to solve 97x96 Here nearest base is 100

97 (100-3) 96 (100-4) Column I column II	97 3 96 4 93 | 12 result is 97*96= 9312

2.5 Urdhva – Tiryagbhyam

This is general formula which can be use to are cases of multiplication. Urdhva – Tiryagbham means' vertically and cross wise.

For this we consider

Step I

456 result 24

864 prev carry 0

4 24

Carry 2

step II

456 result 56

864 prev carry 2

84 58

carry 5

step III

456 result 94

864 pre carry 5

984 99

carry 9

Step IV

456 result 64

864 prev carry 9

3984 73

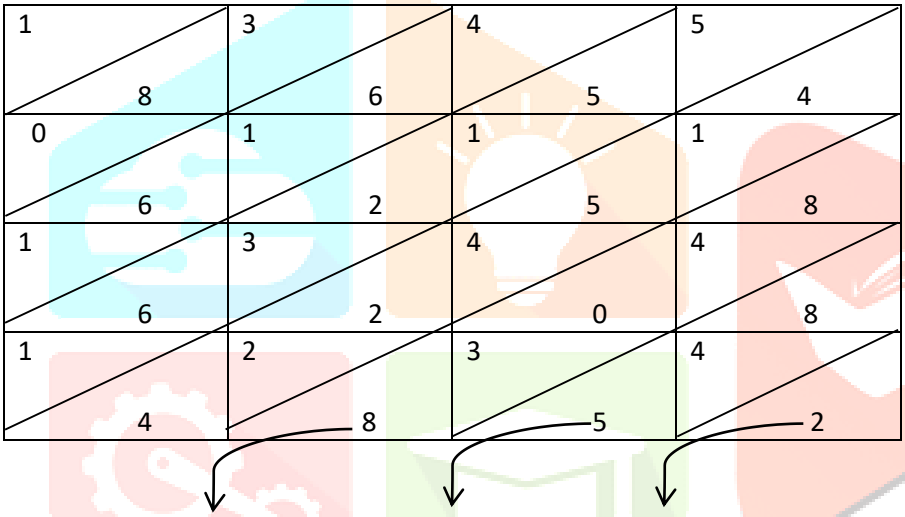
Carry 7

step V

456 result 32

864 prev carry 7

393984 39

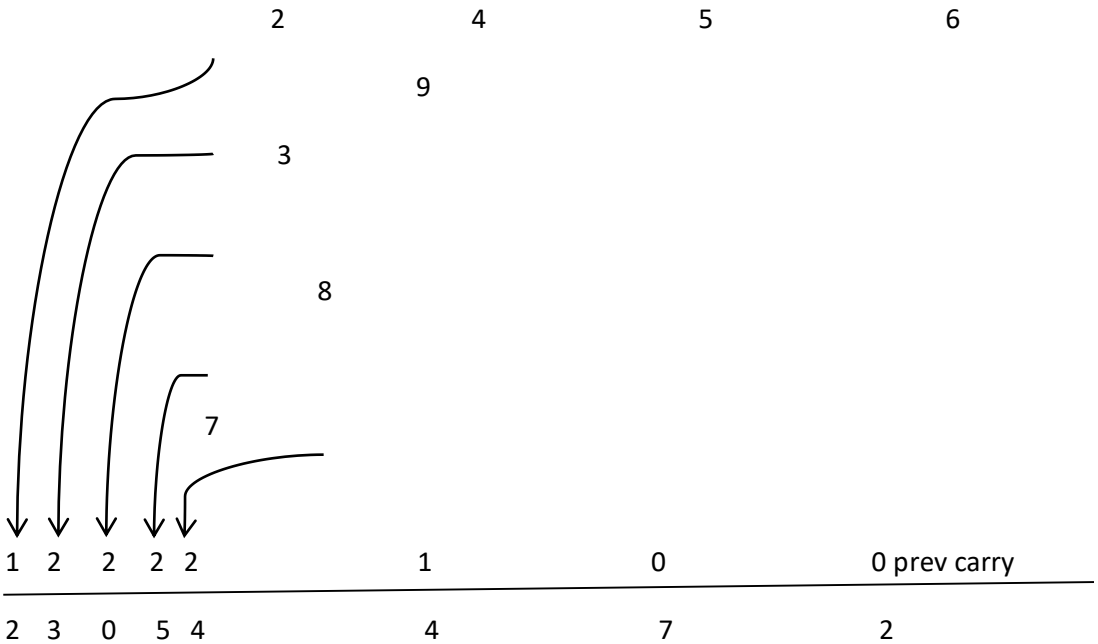


456* 864 = 393984

Figure 1 step's for multiplication by Urdhva tiryakbhyam sutra

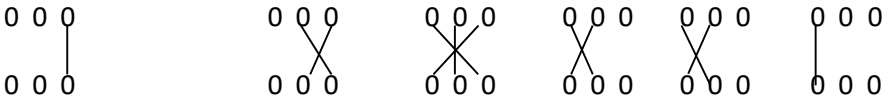
Now we are going to solve multiplication of four digits as 2456 * 9387

The convential method will require 16 multiplication and 15 addition but Urdhva tirykbhyam sutra solve it very easily as follows alternative way of multiplication by Urdhav tiryakbhyam sutra



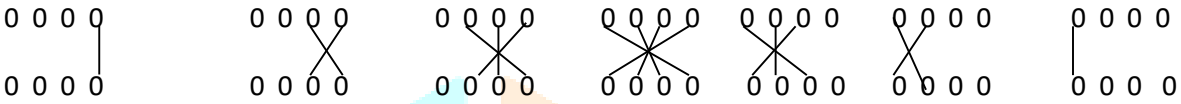
Alternative way of multiplication by urdhva tiryakbhyam sutra

- Algorithm for 3 by 3 multiplication



Step I step II step III step IV step V step VI

Algorithm for 4*4 multiplication



Step I step II step III step IV step V step VI step VII

3.1 Descrete Fourier transform.

For finding DFT now a days only VAN NEU MAN Architectural implementation is classical method is found to be used in digital Computes.

Mr S Kulkarni (5) analysers and Compares the implementation of its algorithm by existing and by Indian Vedic Mathematics techniques, Indian Vedic mathematics method increase The overall efficiency of DFT procedure.

3.2 Digital Signal Processing. which is a technology used almost in engineering discipline for faster addition and multiplication of extreme importance in DSP for Convolution, DFT and Digital filters The Core Computing process is always a multiplication routine, so DSP engineers are Constantly looking for new algorithm and hardware to implement them The Mangesh Karad and Mr chidguker (6) noted the use of multiplication press based on Indian Vedic algorithm and implemented 8085 and 8086 microprocessor. Where use of Vedic algorithm Shows appreciable Saving of processing time.

3.3. Vedic mathematics is used in the field Digital Signal process, chip designing, Discrete Fourier Transform, High speed low power VLSI arithmetic and algorithm, RSA encryption system. Most of necessarily have used mathematics method Such as multiplication division, Sequence and cubes in above fields,

3.4. VLSI Implementation of RSA encryption

H. Jhapligal[3] implemented RSA encryption or decryption algorithm using the algorithm. A Vedic mathematics which is being modified to improve the performances the most significant aspect & the development of divisor, architecture based on Straight division algorithm of in Anceur Indian Vedic mathematics and embody it in RSA encryption or decryption Circuitry for improved efficiency. They proved that RSA circuitry implemented using Vedic division and speed Compared to its implementable using Conventional multiplication and division architecture.

3.5. Multiplier and Squire architecture Time area and power shod in bared an Vedic mathematics developed algorithm by H.Thapliyal (4) the design implemented gate and high level verilog Hardware description larder

3.6 A block Convolution

In DSP application Convolution with very Long Sequence is always required there Compute convolution of long sequence Overlap and method OLA and over lab solve mathod OLS Can be Considered

Hanuman Tharaju M.C., Jayalaxmi H (7)

Proposed a high preference and area efficient architecture for FPGA implementation of black Convolution Development of OLA and OLS Method, using vertically and horizontally Cross wise structure. of Indian Vedic Mathematics architecture developed.

If the bits in the number area Continuously increased to N by N bits then Vedic Mathematics Shows greatest advantage as Compare to other architecture of the multiples over gate delays and regularity of structure

3.7 ALU Design.

The speed of ALU depend on The multiplier algorithm and Structure levels, numerous multiplication technology have developed to enhance the effacing of multiplier which concentrates on reduces the partial product and addition but the care principle behind ite multiplication remains same. By the application for Vedic Mathematics Strikes differ in actual process. M Romalatha(B) and Urdhva tirkbhyam sutra Af Indian Vedic mathematics to built a high speed power efficient multiplier in the Co-processor. Vedic ALU designed by various arithmetic models. This Vedic co-processor is more efficient than the Conventional.

3-8 Elliptic curve encryption

An algorithm developed by H.Thapliyd and M.B Srinivas [9] or point doubling built by Square algorithm of Ancient Indian Vedic mathematics Calculating efficient hand were cereunt Square of number and duplex D property of binary numbers. A considerable input in the point addition and doubling has observed when implementation using proposed techniques for exponentiation.

4. Performance analyses of Ancent Indian Vedic Algorithm.
The following table shows that the Comparison Delay (ns) factor for multiplications implemented in different algorithm between Conventional and Vedic mathematics.

Conclusion : Vedic mathematics can be used in implementation of fast algorithm in various field of engineering and computer the preformation an algorithm is done on the base of delay Efficient of Vedic multiplier in term of high speed and less complexity .

S.N.	Implemented in	Conventional		Vedic	
		8 bit	16 bit	8 bit	16 bit
1	VLSI implementation of high performance RSA algorithm	31.241	57.973	26.081	54973
2	High speed energy efficient ALU Design	31.029	46.811	15.418	22.604
3	An efficient method of elliptic curve encryption (for square)	30.370	60.646	15.193	23.600
4	An efficient method of elliptic curve encryption (for point doubling)	604.861	1327.809	542.325	1207.677

Table I

Sunvay of different multiplication design using Vedic mathematics

6	High speed energy efficient ALU design using Vedic multiplication technique	IEEE 2009	Urdhava Tirkayebhyam	Parallel genention of intermediate product	
7	Implementation of fixed and floating point division using dhvajanaka sutra	IJVES 2013	dhvajanaka sutra	Used in division of RSA on cryption / decryption , efficient in term of area and speed	VHDL and FPGA 8 synthess using Xilinx library
8	A new paradigm in fast BCD division using ancient Indian Vedic mathematics sutras	ICCSEA 2013	Nikhilam and Parvartya sutra	The computing time required by the vedic division algorithm is approximation constant irrespective of the size of divided	

Reference

1. Swami Bharat Krishna Tirthaji, Vedic Mathematics Delhi, Motilal Banarasi Des Publishers, 1965.

2. Vedic mathematics (online available) http://www.hinduism. Co.za/vedic.htm

3. H. Thapiliyal and M.B Srinivas. VLSI implementation of RSA Encryption System using Vedic Mathematics Proceeded As Intsnatimal Conferences an Security Management 2005

4. H. Thabliyal and M. B Srinivas High speed efficient N by N bit parallel. H overlay Multiplier Architecture Based. pb 225-228 Dee 2004

5. Mr Shripad Kulkarni; Descrete Fourier Transform my Vedic Mathematics

6. PD chidigupkar and MT Karao "The Implemental of Vedic algorithm in Digital Signal processing, Global J of Egg Ed vol8 102

PP 153-158.2004

7. Hanumanter Raju M.L, Jay Lakshani H Renuka. R. Ravishankar, M High Speed Block Convulalis using Ancient Vedic Mathematics 2007

M Romalatha, K. Deena Daglan, P Phanome 'High speed Energy Efficient ALU Design using Vedic Multiplication Technique ACTE A, IEEE PP 600-603

9. H Thapliyel and MB Srinivas. An & efficient Method of Elliptic cumeo-2005

10.Vedic Mathematics. The Cesmic software for implementable of fast algorithm. Dr SM kherinar, MS sheetal kapile and Navess Shorpade.