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DESIGN OF AN OPTIMIZED MULTI LEVEL INVERTER WITH MINIMAL SWITCHES EMPLOYING NLC TECHNIQUE

[1]Lakshmi Priya.G , [2]Deepa.K, [3]Isaac.A

[1]Assistant Professor,[2]Assistant Professor,[3]Assistant Professor

[1]Electrical and Electronics Engineering ,

[1]CSI College of Engineering, Ketti, The Nilgiris, India

Abstract: This paper presents a novel multilevel inverter topology for overcoming some of the limitations of the existing topologies. The proposed MLI has a reduced quantity of power electronic switches, thus making is more efficient. The architecture may be expanded to a modular higher voltage level inverter, which uses less DC supplies and uses them correctly without the need of an extra H-bridge circuit. To determine their optimum capabilities, the proposed inverter parameters' simplified formulas are constructed. Furthermore, the extended model of the proposed architecture is used to generate an optimum PMLI design for lowering the total standing voltage (TSV) of the inverter. To demonstrate its advantages over recent MLIs of similar types, comparison studies are given to justify the proposed inverter. Through proper simulation, the MLI obtained a higher efficiency of 95.54%. On the other hand, the optimized 17-level version of PMLI obtained total harmonic distortions (THD) of only 5.15% which successfully attained IEEE 519 standard performance.

Index Terms - Inverter, PMLI design ,Total standing Voltage

I. INTRODUCTION

Multilevel inverters (MLIs) have gained significant attention in recent years and are widely studied in the field of power electronics. MLIs have several advantages over traditional two-level inverters, such as reduced harmonic distortion, improved voltage waveforms, and increased efficiency. Currently, MLIs are being researched and developed for a variety of applications, including renewable energy systems, electric vehicles, and high power industrial drives. In addition, several topologies of MLIs have been proposed and evaluated for their performance, including the Neutral Point Clamped (NPC) inverter, the Flying Capacitor (FC) inverter, and the Cascaded H-Bridge (CHB) inverter. There is ongoing research in the field of multilevel inverters, with an emphasis on overcoming the limitations of current designs, increasing switching frequency, improving efficiency, and reducing cost.

A proposed topology of a minimized component 9-level inverter constructed with just two DC supplies is presented in this project. Many of the suggested low component multilevel inverters (MLIs) use DC supplies that are not being used appropriately along with additional conducting switches. Since this PMLI

(PMLI) has a reduced quantity of power electronic switches, it is more efficient. The architecture may be expanded to a modular higher voltage level inverter, which uses less DC supplies and uses them correctly without the need of an extra H-bridge circuit. To determine their optimum capabilities, the proposed inverter parameters' simplified formulas are constructed. Furthermore, the extended model of the proposed architecture is used to generate an optimum MLI design for lowering the total standing voltage (TSV) of the inverter. To demonstrate its advantages over recent MLIs of similar types, comparison studies are given to justify the proposed inverter. Through proper simulation, the MLI obtained a higher efficiency of 95.54%. In addition, the optimized 17-level version of MLI obtained total harmonic distortions (THD) of only 5.15% which successfully attained IEEE 519 standard performance.

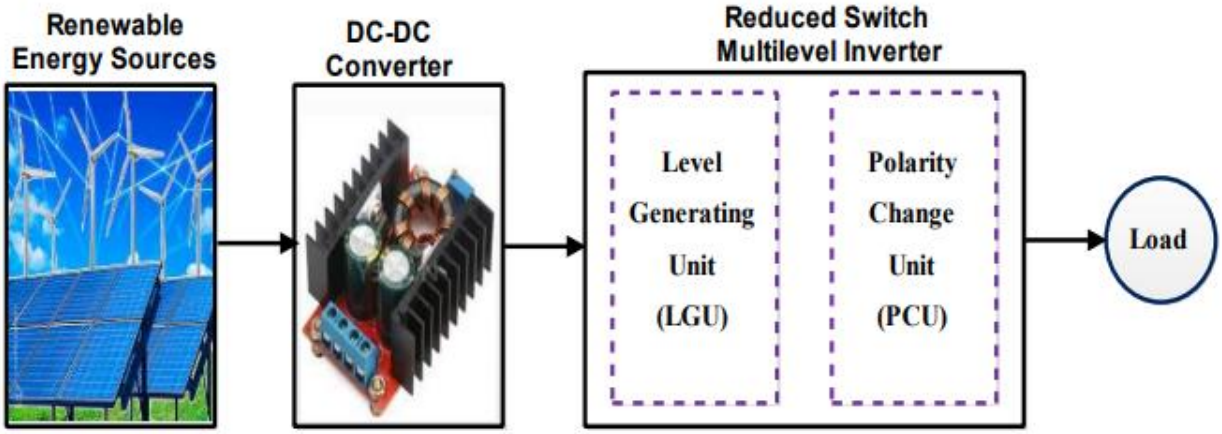
II. LITERATURE REVIEW

Multilevel inverters offer a consistent and precise output voltage. In the realm of power electronics, researchers find MLIs that have different shapes to be very interesting. Recently, a large diversity of configurations has developed in power systems, with variety of applications. In medium and high-power systems, including power grid, electrical vehicles [1], drive systems [2], active power filters [3], [4], wind turbines [5], solar systems [6], and HVDC for transmission lines [7], MLIs are the preferred inverter above standard two-level inverters. Since MLIs generate multilayer voltage, they feature minimal harmonic profile and ripple-free output voltage. The cascade connection capabilities of MLIs confirms that the switches have minimal stress and electromagnetic interference, resulting in high efficacy for the system. Multilevel inverters come in a variety of modules, for instance, Neutral Point Clamped (NPC), Flying Capacitor (FC), and Cascade H-bridge (CHB). Large capacitor voltage dips are observed in FC and NPC, resulting in imbalanced DC links and high voltage stress on the switches. CHB topologies, on the other hand, are suggested by researchers as a way to design configurations with fewer components. The fundamental disadvantage of typical CHB-MLIs is that they need a large number of separate DC sources and conductor switches to generate multilevel voltage. According to [8], MLIs can be divided into three different types depending on the structure and the magnitude of the DC supplies: which are asymmetrical, symmetrical, and hybrid MLIs. In the unipolar MLI topologies proposed in [9]–[12], H-bridge circuits with polarity generating capacity are necessary to acquire negative and positive voltage levels at the output provided by the level generating (LG) section. Although the LG section generated voltage become approximately double by the H-bridge, the power electronic switches of the H-bridge need to endure the highest voltage stress equivalent to the total DC-link voltage [13]. Switched-battery boost (SBB) MLI as reported in [14] reduces the switch count by using two DC supplies with one diode and a switch to generate just two voltage levels. However, to generate higher voltages, this MLI needs a greater number of DC supplies, and the levels can only be attained by combining the multiple sources. As an alternative, criss-cross switch based inverters are proposed to generate greater voltage with fewer components. The MLI using criss-cross switch configuration as shown in [15] included the semi-half-bridge cell that employed a moderate number of DC sources and semiconductor switches to achieve a certain voltage level. Although these MLIs employ minimal DC sources, an extra H-bridge circuit is utilized that has high voltage stress and therefore, raised

their total standing voltage (TSV). To overcome these disadvantages, a novel topology has been proposed in this project.

III. EXISTING SYSTEM

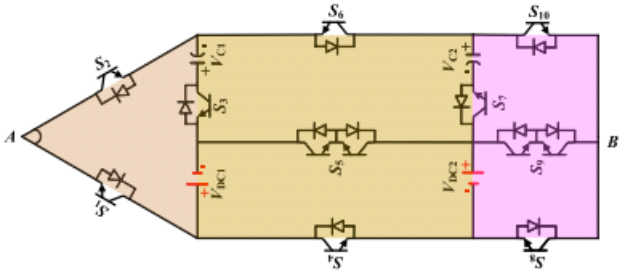
A Multi-level Inverter (MLI) is a type of converter system used in power electronics to produces the preferred output voltage from input of several DC voltage levels.MLI power conversion technology has rapidly progressed with strong potential for future use [1].The conventional Multi-Level Inverters has two or three stages of conversion. The first step is to amplify the input DC voltage to the required voltage level using DC - DC converter and second step is to feed the boosted DC voltage to the inverter to convert input DC from RES to AC of required voltage [2].Due to the varying output voltage of Renewable Energy Sources (RES), a DC-DC boost converter between the inverter and the RES must be integrated to achieve constant DC-link voltage as shown in Figure. This is also called a two-stage power transducer. An extra dc – dc converter, however, makes the whole system complex, voluminous, high-cost and less efficient. Multi-level Inverters has advantage over standard two level and three level inverter because of less cost, complexity, EMI, voltage tension and switching losses [3-6].The most widely used topologies for MLI are flying capacitors, clamped diodes and cascaded H-bridge inverters. Amidst this topology Hbridge topology has less number of components to generate same output [7].



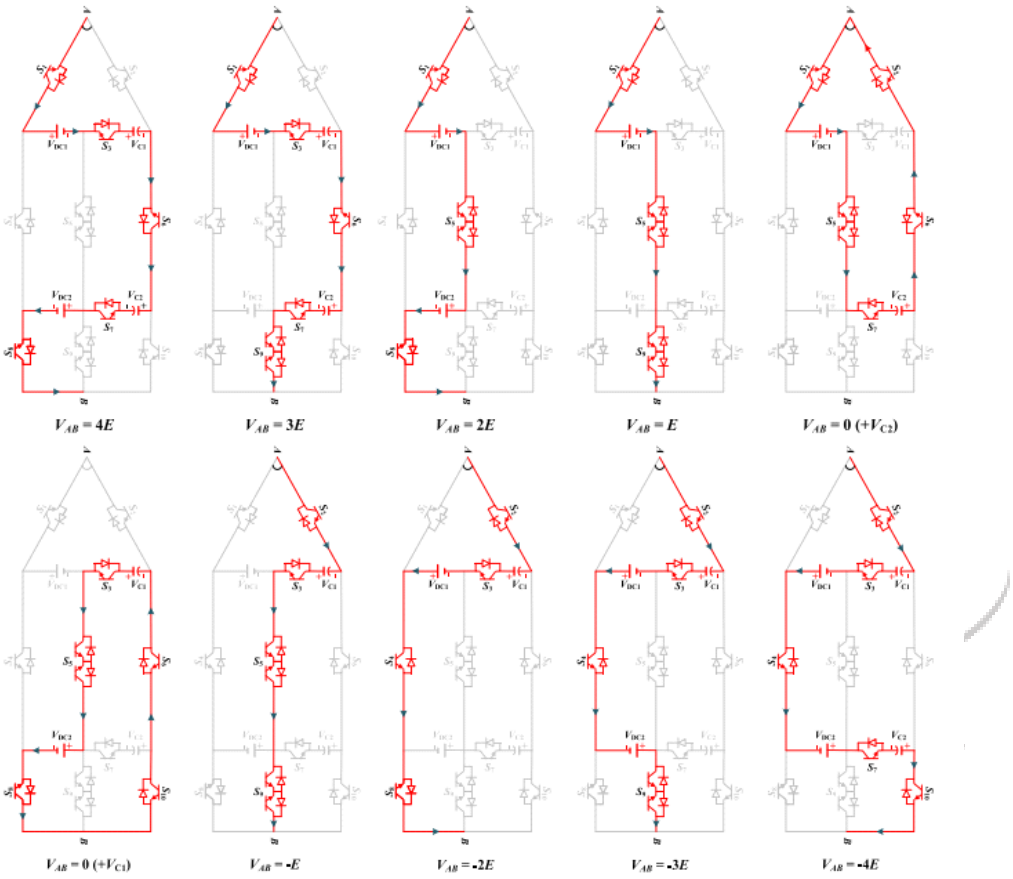
RES integrated with DC-DC converter and MLI (Two stage converter)

IV. PROPOSED MLI AND ITS CONFIGURATION

The PMLI module is built using a proper configuration of power electronic components to achieve maximum number of voltage levels using the DC sources and switched capacitors. This topology uses the basic operation of switched capacitors to further increase and boost the voltage levels. Another challenge in this type of MLI would be to maintain the voltage of the capacitors without needing any additional circuit.



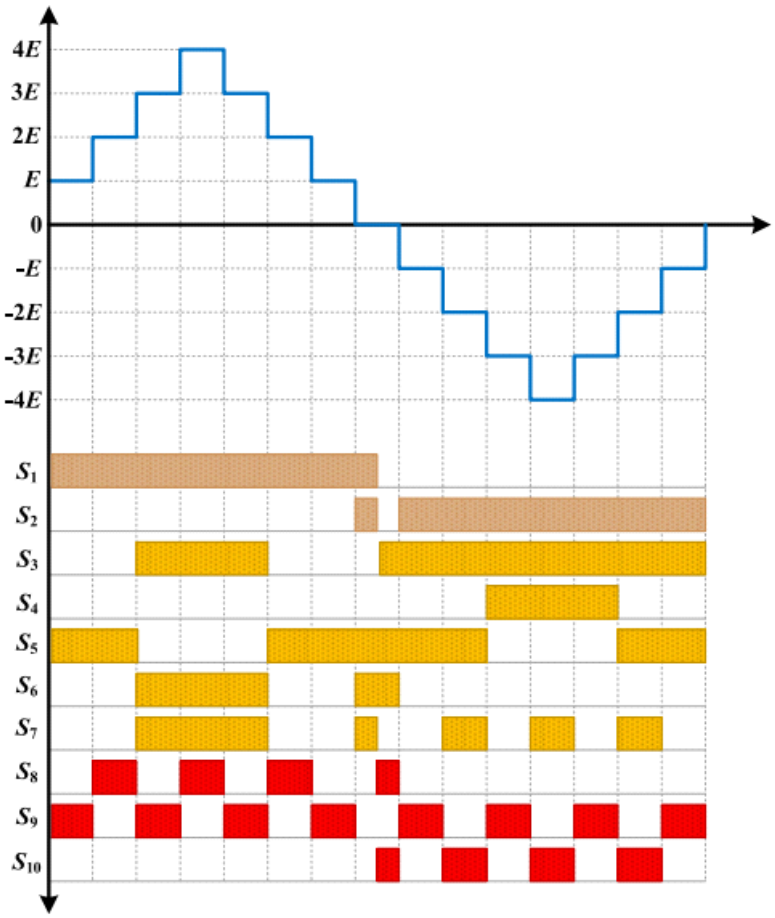
SCHEMATIC CIRCUIT DIAGRAM OF PROPOSED MLI



CONFIGURATION AND WORKING PRINCIPLE OF PMLI

The PMLI is designed following the edifice of a pencil as depicted in figure. It has 3 principal segments which are represented using three color schemes. The first part is called the head (faded-pink color), the 2nd segment is referred as the body (brown color) and eraser is the final part (pink color). The first section includes 2 unidirectional switches (S1, S2,). These serve as directional switches and the module's current path is determined by them. PMLI, for example, will only produce positive voltage levels, if S1 is switched on. However, when S2 is turned on, it can typically generate negative voltage levels. The body part consists of 4 unidirectional switches (S3, S4, S6, S7) and 1 bidirectional switch (S5), 2 DC source (V_{DC1}, V_{DC2}) and 2 switched capacitors (V_{C1}, V_{C2}). The switches S3 and S7 is utilized to avoid the short-circuit of capacitor V_{C1} and V_{C2}. The body part performs as the channel between the head and the eraser. The reverse current is blocked by the bidirectional switch S5. The bottom part of PMLI is an eraser shaped part that consists of 2 unidirectional switches (S8, S10) and 1 bidirectional switch (S9). It structurally looks like a T-type inverter and thus can generate negative levels without needing additional H-bridge unit. The MLI can produce 9

levels voltage (±4 levels, and 0 level) using the DC-links. PMLI's power switches are cleverly implemented so that the capacitors and DC supplies are coupled through different current channels, requiring no additional circuit to balance out the voltage of the capacitors.



V. OPERATION OF PMLI USING NLC TECHNIQUE

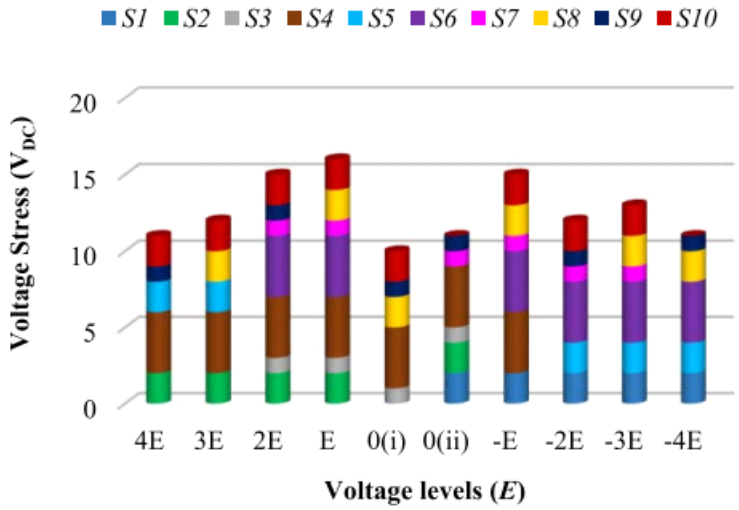
PMLI's switching pattern

Output		Pattern of switching									
	V_{AB}	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}
+Levels	4E	1	0	1	0	0	1	1	1	0	0
	3E	1	0	1	0	0	1	1	0	1	0
	2E	1	0	0	0	1	0	0	1	0	0
	E	1	0	0	0	1	0	0	0	1	0
$+V_{C2}$	0(i)	1	1	0	0	1	1	1	0	0	0
$+V_{C1}$	0(ii)	0	0	1	0	1	1	0	1	0	1
- Levels	-E	0	1	1	0	1	0	0	0	1	0
	-2E	0	1	1	1	0	0	0	1	0	0
	-3E	0	1	1	1	0	0	0	0	1	0
	-4E	0	1	1	1	0	0	1	0	0	1
Number of turn on in each cycle		1	3	2	1	2	3	4	7	8	3

Table shows the switching pattern while figure.4.2 illustrates the current routes of PMLI. In addition, figure.4.3 shows the behave of the power switching components of the proposed PMLI using the nearest level control (NLC) technique. It can be observed that zero voltage level is used to charge the DC capacitors. Table.4.1. also shows the number of times each switch turns on during one complete cycle of operation. The

switching sequences of Table.4.1. confirm that switches (S1, S2, S3, S4, S5, S6, S10) are turning with low frequency which has significantly reduced the TSV of the PMLI. For each voltage level of PMLI, a graphical depiction of the TSV of each switch for every voltage level is presented in figure.4.4. Thus, the TSV of the PMLI is calculated to be 16 V_{DC}.

MODULARITY OF SYMMETRIC MODULE



TSV of PMLI's each switch at various voltages.

The proposed PMLI's flexibility is verified in this section by showcasing its ability to generate higher number of voltage levels. This is done by extending the structure of the 9-level PMLI inverter which is depicted in figure. Here, the ratio between the DC sources and the capacitors is unity. The extended structure is developed by extending the body part of PMLI and which is then connected with another similar structure using cascaded connection as depicted in figure. The polarity is converted using 2 conduit switches which are placed between the main body and extended body of the PMLI. These 2 switches will also function as the polarity converter similar to the directional switches used in the head section of the PMLI. The cascaded connection is established with z th module to double the voltage producing ability. The x th sub-modules incorporate 6 unidirectional switches, 1 bidirectional switch, 2 switched capacitors, and 2 DC sources. For a specific number of x th module and z th module, the number of voltage sources (N_{DC}), number of capacitors (N_C), number of power switches (N_P), and the voltage levels (N_V), TSV (N_{TSV}) can be determined using the following:

$$N_{DC} = N_C = 2(z + x + 1) \quad (1)$$

$$N_P = 4(3z + 2x + 3) \quad (2)$$

$$N_V = 8x + 8z + 9 \quad (3)$$

$$N_{TSV} = 16x + 21(z + 1) \quad (4)$$

Considering the above figure. and at constant z, for a specific number of DC sources, the other parameters of PMLI can be determined as follows:

$$N_{DC} = N_C = k \quad (5)$$

$$N_P = 4(k + 1) \quad (6)$$

$$N_V = 4k + 1 \quad (7)$$

$$N_{TSV} = 8k + 5 \quad (8)$$

Since power switches of the symmetrical cascaded z th module have same TSV as the original module (n = 1), the TSV can be realized by:

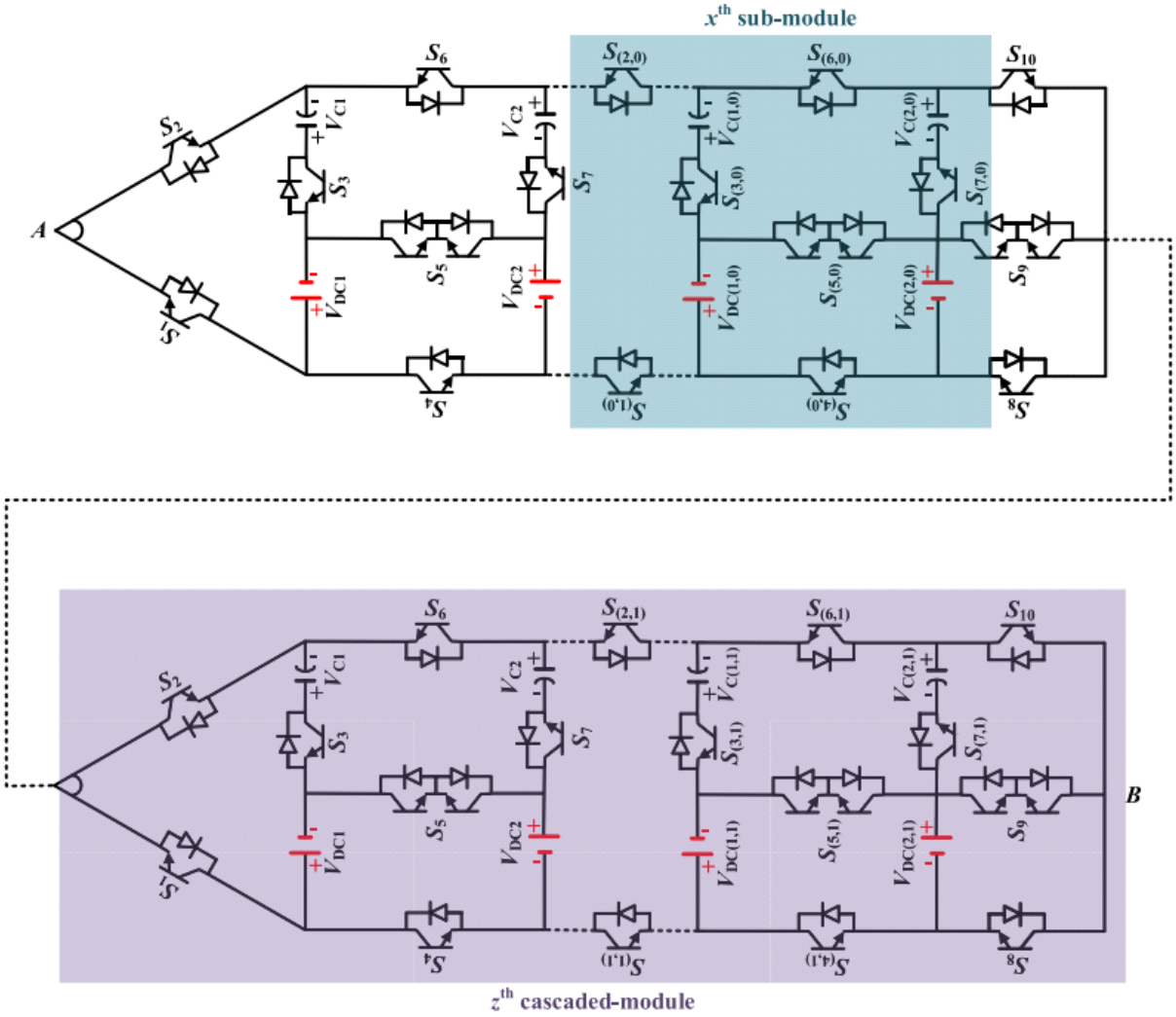
$$TSV_{n=1} = TSV_{z1} = TSV_{z2} \quad (9)$$

Considering a constant number of cascaded modules, the voltage stress of the switches of the symmetrical sub modules can be determined by:

$$Vs_{(7x-6,z)} = Vs_{(7x-6,z)} = Vs_{(7x-6,z)} = 2V_{DC} \quad (10)$$

$$Vs_{(7x-3,z)} = Vs_{(7x-1,z)} = 4V_{DC} \quad (11)$$

$$Vs_{(7x-4,z)} = Vs_{(7x,z)} = V_{DC} \quad (12)$$



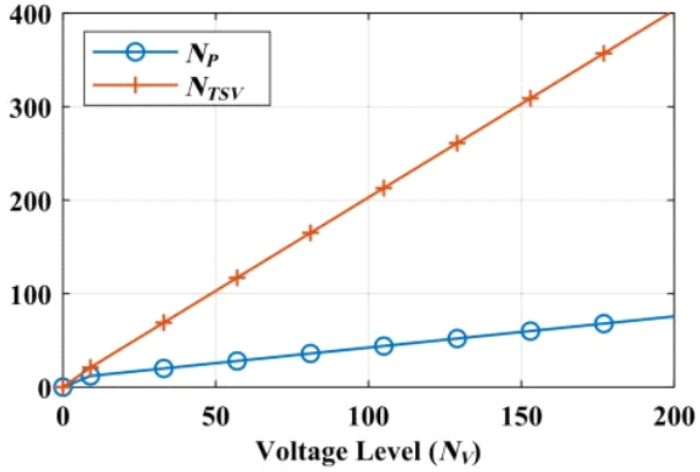
Modularity of Asymmetric Module

VI. PMLI UNIT WITH X^TH AND Z^TH MODULES

Although asymmetrical MLI structures induces superfluous voltage stress and imbalance into the system, it is one of the simplest methods of boosting voltage levels without introducing any structural complexity or usage of higher number of power electric components. The proposed PMLI can also be extended using asymmetrical module. In order to maximize the voltage level, the second submodule or of the PMLI is designed with voltage sources with tertiary voltage capability (i.e., $V_{DC}(1,0) = V_{DC}(2,0) = 3E$) or in other words, a voltage ratio of 1:3 is maintained between the original module and the extended module. Thus, with the addition of only 8 switches the extended PMLI would have the ability to generate 33 voltage levels. For synthesizing similar number of voltage levels, a symmetrical PMLI would require 3 extra submodules (i.e., x = 3) or 36 power switches according to (2) and (6). However, the TSV of the entire PMLI would increase to $69V_{DC}$. The relation between the voltage levels and voltage stress are shown in figure.4.6. for further comprehension. Similar to the symmetrical extension of PMLI, the equations for the asymmetrical extension can be realized by:

$$N_V = 3(8x + 8z + 9) \quad (13)$$

$$N_{TSV} = 48x + 63z + 21 \quad (14)$$



Characteristics of extended asymmetrical PMLI.

Considering a constant number of cascaded modules, the voltage stress of the switches of the asymmetrical submodules can be determined by:

$$Vs_{(7x-6,z)} = Vs_{(7x-5,z)} = Vs_{(7x-2,z)} = 6V_{DC} \quad (15)$$

$$Vs_{(7x-3,z)} = Vs_{(7x-1,z)} = 12V_{DC} \quad (16)$$

$$Vs_{(7x-4,z)} = Vs_{(7x,z)} = 3V_{DC} \quad (17)$$

VII. VOLTAGE RIPPLE CALCULATION OF PMLI

For a high-quality AC output, a constant total DC-link voltage is necessary. In order to avoid a significant amount of voltage ripple, a switchable capacitor must have a voltage ripple of no more than 5%. The following calculation can be used to calculate the voltage ripples of both capacitors:

$$\Delta V_C = (1/\omega C) \quad (21)$$

where $i = i_0$

Using PMLI's basic output current, this may be figured out further as follows:

$$\Delta V_C = (IAB/\ \omega C) \quad (22)$$

Here, ϕ indicates the angular shift between voltage and current, ω indicates the angular frequency of the multilevel AC voltage, ripple voltage end angle is indicated by θoff , ripple voltage starting angle is indicated by θon, capacitance of capacitors is indicated by C. Using the following equations, the ripple angle can be calculated as:

$$\theta_{on} = \sin^{-1}[\ (N_{VR} + 0.5)/Q \times m(N_C + 1)\ ] \quad (23)$$

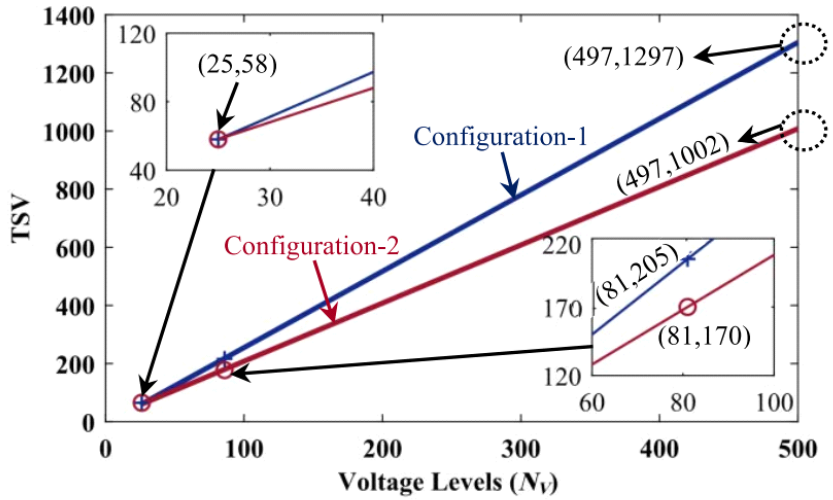
$$\theta_{off} = \Pi - \theta_{on} \quad (24)$$

where, the quality factor is indicated by Q and modulation index is indicated by m. The capacitor voltage ripple level is indicated by N_{VR}. Both capacitors' voltage ripples are computed, and the computed value is 3.23 V. This determines that low ripples exist in the capacitor voltage, and the PMLI can be implemented effectively.

VIII. OPTIMIZED PMLI TOPOLOGY

By choosing an optimum structure for each module, the TSV of the extended symmetrical PMLI can be reduced. Here, the asymmetric PMLI is not considered because of drawbacks associated with those modules such as high TSV and voltage imbalance which can cause serious problems specially in renewable energy applications. A specific combination of x (submodules) and z (cascaded modules) must be chosen to develop the proposed PMLI's extended structure having minimum voltage stress. This optimum configuration also ensures that a reduced number of power electric components are fully utilized. Thus, the voltage levels (N_V) and corresponding TSV for two alternative configurations of PMLI under different values of x and z can be plotted to find the optimal configuration.

A. CONFIGURATION 1: The PMLI can be designed with any number of cascaded or z th modules, each having one cross connected submodule (x = 1). Under this configuration with the number of voltage levels that can be produced by the proposed inverter is found using (3) which is 8z+17. On the other hand, the TSV of the whole inverter can be determined by utilizing (4).



N_V vs. TSV of extended PMLI for configurations 1 and 2.

B. CONFIGURATION 2: The PMLI can be designed with only cascaded module (z) and several submodules (x > 1) in this configuration. Under these circumstances (configuration-1 and configuration-2), the number of voltage levels (N_V) and TSV of the novel MLI can be again determined using (3) and (4) respectively. The graphical representation of N_V vs TSV is illustrated figure.4.7. It is visible from figure.4.7. that in terms of TSV configuration-2 is more feasible than configuration-1. The higher THD of configuration-1 is due to the utilization of 4 extra switches while adding several cascaded modules. Thus, the overall cost of configuration-1 will be much higher than configuration2 since switches with high voltage ratings are highly expensive [28]. However, in terms of simplicity and switching similar cascaded modules and same switching sequences. In terms of power switches, configuration-2 is more costeffective since it requires a smaller number of power switches for generating higher voltage levels. Configuration2 can generate 81-level voltage utilizing 84 power switches while configuration-1 requires 112 power switches for generating same voltage level. Considering all these advantageous aspects, this project gives more emphasis on configuration 2.

IX. COMPARISON STUDIES

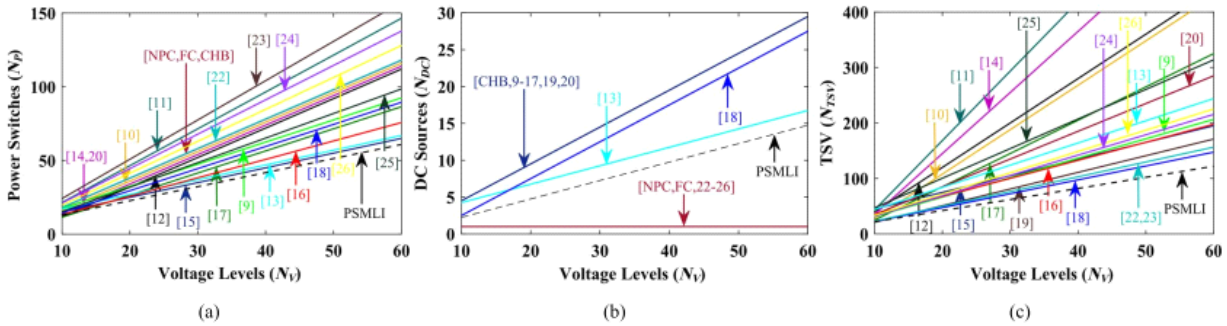
In order to justify PMLI's superiority in terms of usage of lesser number power electronic components, a comprehensive comparative analysis is presented in this section with classical and other recently PMLIs. For comparison, the symmetrical version is selected for each MLI. Configuration-2 of PMLI is selected for this analysis since it is more optimized than configuration-1. The parameters that are chosen to conduct this comparison: number of DC sources (N_{DC}), number of power switches (N_P), number of voltage levels (N_V), maximum voltage (N_{Vmax}), TSV, boosting factor and requirement of H-bridge circuit.

Comparison analysis between different MLI's

MLIs	N_{DC}	N_P	N_{Vmax}	N_V	TSV	Boosting Factor	H-bridge
NPC	1	$4(n+3)$	$n+3$	$2n+7$	$4(n+3)$	0	No
FC	1	$4(n+3)$	$n+3$	$2n+7$	$4(n+3)$	0	No
CHB	$n+3$	$4(n+3)$	$n+3$	$2n+7$	$4(n+3)$	0	Yes
[9]	$2(n+1)$	$2(3n+5)$	$2(n+1)$	$4n+5$	$14(n+1)$	0	Yes
[10]	$n+3$	$2(2n+5)$	$n+3$	$2n+7$	$4(4n+1)$	0	Yes
[11]	$n+3$	$5n+14$	$n+3$	$2n+7$	$25n+6$	0	Yes
[12]	$n+3$	$2(2n+3)$	$n+3$	$2n+7$	$16(n+1)$	0	Yes
[13]	$n+3$	$4(n+3)$	$2(n+1)$	$4n+5$	$8(2n+3)$	0	Yes
[14]	$n+3$	$4(n+2)$	$n+3$	$2n+7$	$2(11n+1)$	0	Yes
[15]	$n+3$	$2(n+6)$	$n+3$	$2n+7$	$6(n+6)$	0	Yes
[16]	$2(n+1)$	$5n+7$	$2(n+1)$	$4n+5$	$13n+19$	0	No
[17]	$n+3$	$3n+7$	$n+3$	$2n+7$	$12n+7$	0	No
[18]	$2n$	$5n+9$	$2(n+1)$	$4n+5$	$10(n+1)$	2	No
[19]	$n+4$	$2n+10$	$n+4$	$2n+9$	$2(4n+9)$	0	No
[20]	$n+3$	$4(n+2)$	$n+3$	$2n+7$	$10(n+2)$	0	No
[22]	1	$12n$	$3n$	$6n+1$	$16n$	3	No
[23]	1	$16n$	$3n$	$6n+1$	$16n$	3	No
[24]	1	$14n$	$3n$	$6n+1$	$22n$	4	No
[25]	1	$10n$	$3n$	$6n+1$	$32n$	3	Yes
[26]	1	$13n$	$3n$	$6n+1$	$23n$	4	Yes
[27]	1	$12n$	$3n$	$6n+1$	$22n$	3	No
PSMLI	$2n$	$4(2n+1)$	$4n$	$8n+1$	$8(n+1)$	2	No

The generalized equations of the MLIs are shown in Table.4.2.In comparison with the classical MLIs it can be observed that the PMLI has used low number of power switches. The classical NPC inverters require a smaller number of DC sources compared to PMLI. However, it requires huge number of switches, clamping diodes and capacitors to generate greater voltage levels. Thus, it has serious voltage imbalance issues which requires the application of complex modulation techniques to be resolved. FC MLIs also requires small number of DC sources but has the characteristics of using large number of capacitors and power switches as shown in above figure.. which can greatly hamper the efficiency of the MLI by inducing capacitor losses in the system. CHB MLI requires large number of switches and DC sources compare to the PMLI as illustrated in figure.4.8(a). and 8(b) respectively. Symmetric CCMLI [15] requires 14 switches and 5 DC sources to

generate 9-level output which is more than the PMLI. In addition, the TSV of the CCMLI is $42V_{DC}$ as shown in the figure. which is substantially greater than PMLI. A similar attribute can be observed in the MLIs proposed in [16]–[20] where, large number of switches and DC sources are required compared to PMLI. The PMLI in [17], [19] require same number of switches as PMLI for the basic configuration (n = 1). However, as the voltage level increases, they require a greater number of DC sources and switches evidential from figure.4.7(c). On the other hand, the MLIs proposed in [16]–[20], [22]–[24], [27] avoided the use of H-bridge. However, they require high number of power switches. The PMLI is also compared with similar class of switched capacitors MLIs (SCMLI) proposed in [22]–[27]. It can be observed from figure.8(b). that although these MLIs utilized a single DC source, they tend to have higher TSV and uses increased number of switching devices compared to the PMLI. It is further noticeable that the boosting factor is only present for the MLIs that are comprised of switched capacitors units. This provides an added advantage to these MLIs since they do not require high number of isolated DC sources and transformers. The highest boosting factor is provided by the MLIs proposed in [24] and [26] as shown in Table. Both of these modules used single DC source to produce 9-level output at n = 1. On the contrary, the SCMLIs proposed in [22], [23], [25], and [27] have a triple boosting ability. Although, these MLIs have higher boosting ability than the PMLI, they have utilized high number of power switches and also induced high TSV which is evident from figure (a). and figure (c), respectively. Thus, it can be stated that the proposed PMLI has created a balance among the utilization of power electronic components such as switch and DC sources, voltage boosting ability, and TSV. PMLI's superiority is further validated by comparing it with other MLIs in terms of power losses and efficiencies. The power losses and efficiencies are obtained using PLECS software.



Comparative analysis among different MLI's in terms of: (a) switches [N_P], (b) DC sources [N_{DC}], (c) TSV [N_{TSV}].

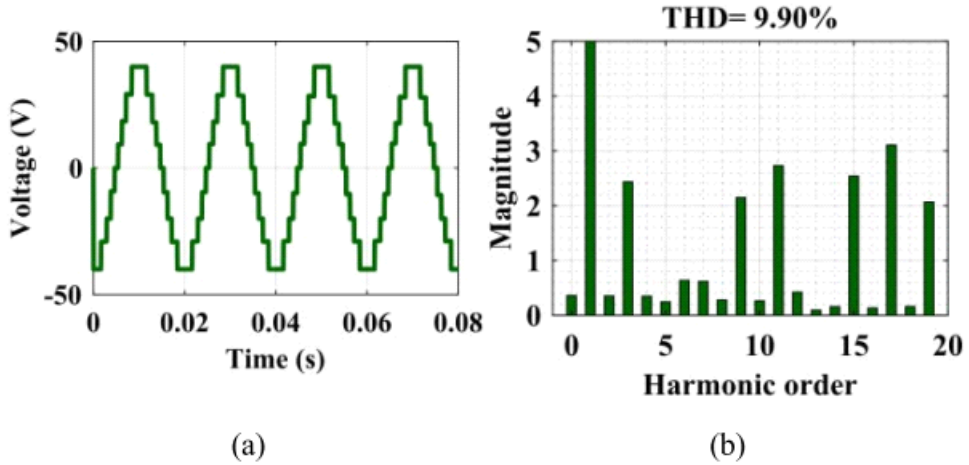
Power loss and efficiency comparison for different MLI's.

MLIs	P_{con} (W)	P_{sw} (W)	P_{cap} (W)	P_{total} (W)	η (%)
NPC	9.49	0.12	23.66	33.27	91.68
FC	8.43	0.14	73.12	81.69	79.58
CHB	8.67	0.14	0	8.81	97.83
[9]	18.45	0.22	0	18.67	95.33
[10]	22.40	0.15	0	22.55	94.36
[11]	38.80	0.28	0	39.08	90.23
[12]	21.08	0.07	0	21.15	94.71
[13]	42.16	0.30	0	42.46	89.39
[14]	18.97	0.09	0	19.06	95.24
[15]	19.37	0.28	0	19.65	95.09
[16]	12.65	0.18	0	12.83	96.79
[17]	6.26	0.15	0	6.41	98.40
[18]	9.22	0.13	11.83	21.18	94.70
[19]	5.93	0.08	0	6.01	98.49
[20]	11.86	0.17	0	12.03	96.98
[22]	6.32	0.09	11.80	18.21	95.45
[23]	8.43	0.12	11.79	20.34	94.92
[24]	10.14	0.14	11.81	22.09	94.48
[25]	10.54	0.30	11.80	22.64	94.34
[26]	9.85	0.14	29.48	39.47	90.13
PSMLI	9.20	0.21	11.80	22.06	95.54

The MLIs are built with similar model of power electronic switches, DC sources, diodes and capacitors to justify the comparison. Furthermore, a maximum DC-link voltage of 200 V is considered for the MLIs with an operating power of 900 W. The efficiencies (η) of each MLI are determined by considering three types of losses which are conduction losses (Pcon), switching losses (Psw) and capacitor losses (Pcap). The power loss data obtained from PLECS software is then added to determine the total power losses (Ptotal) of each MLI as demonstrated in Table. It can be observed from the above table . that PMLI's efficiency is less than the MLIs proposed in [16]–[20]. It is due to the fact that these MLIs does not incorporates any capacitors and hence, there is no capacitor loss. Nevertheless, all these MLIs use several DC sources which can massively increase their building costs. It should be addressed that the SCMLIs' efficiency is calculated for generating 7-level voltage. Yet, the PMLI has higher efficiency than all SCMLIs**.**

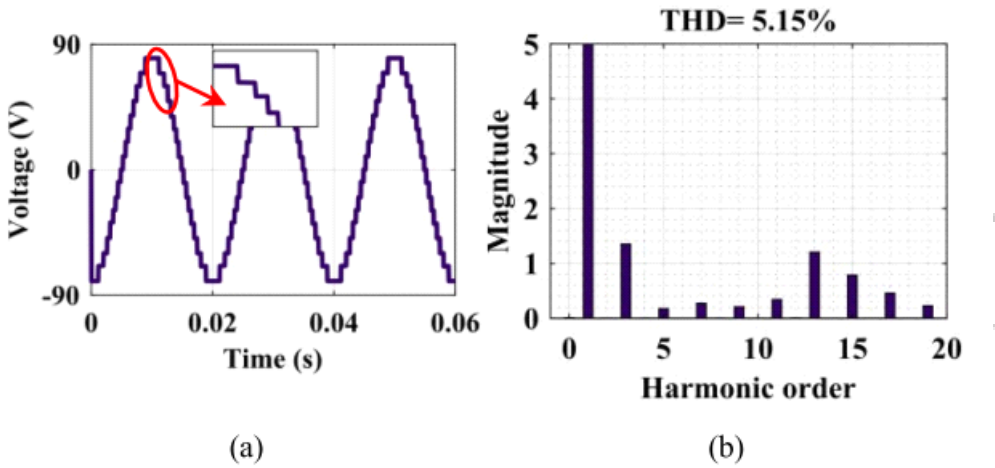
X. RESULTS AND DISCUSSION

MATLAB Simulink is used to simulate the proposed PMLI. The illustration for 9-level (n = 1) output voltage of PMLI is given in figure.4.9(a). using the NLC modulation technique. Here, each voltage level is 10 V to create a 50 Hz multilevel staircase output voltage of 40 V.



Simulation results of 9-level PMLI: (a) output voltage and (b) harmonic spectrum

The harmonic spectrum of the 9-levels output voltage is depicted in figure (b). Furthermore, the 17-levels (n = 2) output voltage and harmonic spectrum of the cascaded PMLI are shown in figure (a) and figure (b) respectively. Having the same individual voltage level of 10 V, this cascaded module is able to generate 80 V output. It can be noticed that in terms of THD, the extended configuration performed much better than the basic configuration since it produced almost double amount of voltage level.



Simulation results of 17-level extended PMLI: (a) output voltage and (b) harmonic spectrum.

Therefore, the THD of this module has effectively fulfilled the IEEE 519 standard. The THD of 9-level PMLI can be improved by implementing selective harmonic elimination (SHE) control where the switching angle of each power switch is individually optimized [28].

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