IJCRT.ORG ISSN : 2320-2882

INTERNATIONAL JOURNAL OF CREATIVE RESEARCH THOUGHTS (IJCRT)

An International Open Access, Peer-reviewed, Refereed Journal

Next-Gen Power Solutions: Unleashing The Potential Of Advance Leakage Methods In CMOS VLSI Circuits

[1]Veena Vijayan
[1]Guest Lecturer,
1Department of Electrical and Electronics Engineering, [1]NSS polytechnic college, Pandalam, Kerala, India

Abstract: As semiconductor technology advances, the escalating demand for efficient power consumption in electronic devices, especially mobile gadgets, has become paramount. In pursuit of low-power circuits, this study explores various techniques, including the proposed Advance Leakage Method, to mitigate power loss, emphasizing the critical issue of leakage power, which can contribute up to 50% of overall power consumption. The study examines the dissipation of power due to leakage in VLSI circuits. A comprehensive analysis of leakage reduction methods, such as the Stack Technique, LECTOR Technique, Source Biasing Approach, Stack ONOFIC Approach, and the Proposed Approach, is presented. The study employs CMOS inverter models, revealing a significant reduction in leakage power by 50%, demonstrating the efficacy of the proposed method. The results, including power consumption and propagation time for various circuits and techniques, are tabulated and discussed, providing valuable insights for future low-power VLSI circuit designs.

Index Terms **- Power reduction, VLSI, leakage, CMOS, leakage current, transistor.**

I. INTRODUCTION

As the semiconductor device sector experiences a surge in technical breakthroughs, power consumption has emerged as a critical subject that requires attention. For example, the lack of power expenditure efficiency in today's very popular mobile gadgets forced multinational electronics companies to concentrate on creating devices that use less power. The requirement for mobility, portability, and user reliability, along with the expansion of battery-powered devices and environmental efforts, are the drivers that push us toward designing circuits with low power consumption. One common method of achieving the goal of better performance is to scale the CMOS devices [1]. However, the power density rises by 40% with each generation due to scaling technologies. There is never a single, perfect approach to design a device because there is always a trade-off between many factors, such area, latency, or high efficiency, in order to reduce the power density. Every device's design is therefore determined by its intended use and product requirements. Power, speed, and complexity have replaced area and speed as the main concerns for IC design space. As demonstrated by IC design space in figure 1, there will be significant power consumption when complicated circuits or high speed are needed.

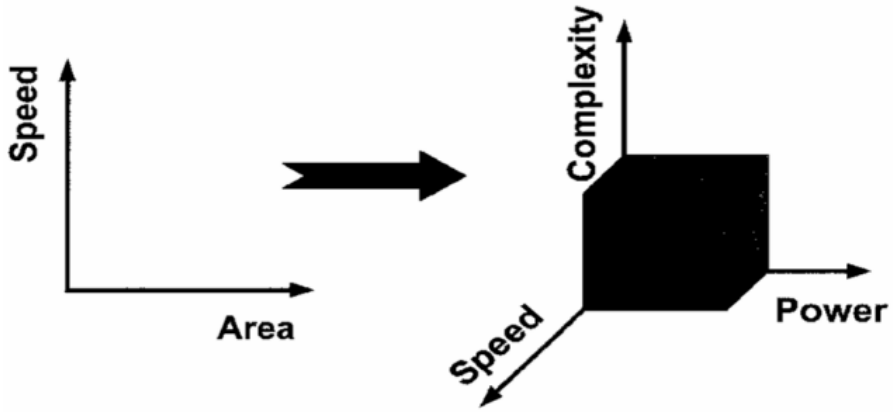

fig.1: IC design space

A circuit's consumption of power will be high at various points, and one of the primary causesfor power loss is leakage power, which can account for up to 50% of the circuit's overall consumption of power, particularly in the most recent high-performance microprocessors.

1.1.Dissipation of Power Due to Leakage

Both dynamic and static components contribute to the power consumption of CMOS. Regardless of whether transistors are switching or not, static power is used, whereas dynamic power is used. Static power is becoming a major concern for present and future technology as CMOS feature area shrinks [2].The dissipation of power due to leakage in VLSI circuits is caused by many current components as depicted in figure 2.

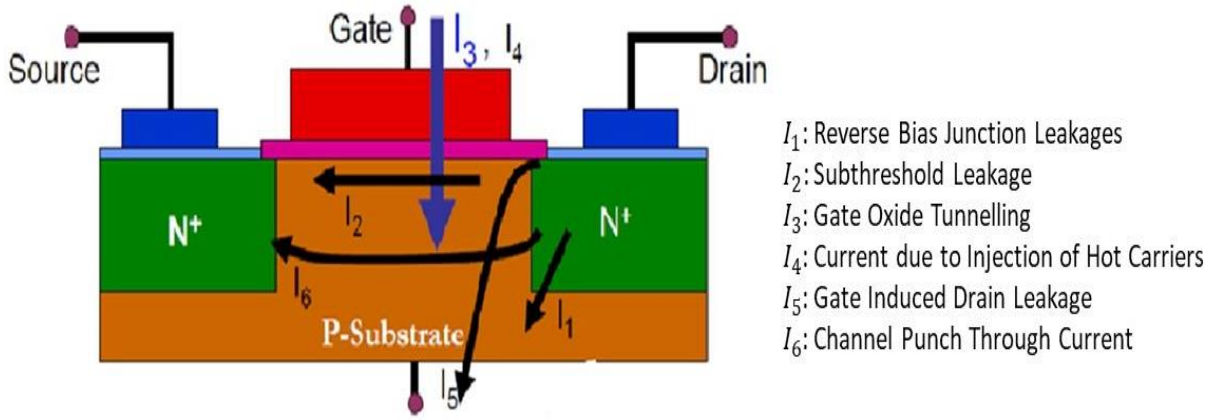

fig.2: primary CMOS leakage current sources

Subthreshold leakage, gate oxide tunneling leakage, as well as reverse-bias p-n junction leakage appears to be the primary causes of leakage current. Either minority carrier drift or diffusion close to the edge of the depletion region or the formation of electron-hole pairs within the depletion region is the cause of the reverse bias p-n junction leakage [3].Due to the close proximity of the source and drain regions of short channel devices, there is a lowered potential barrier, which results in a low threshold voltage, or subthreshold voltage. Because of the increased electric field across the reduced oxide thickness, which leads to electrons tunneling from the substrate to the gate or the gate to the substrate, gate oxide leakage arises.

Gate-induced drain leakage is caused by minority carriers migrating between the channel and substrate regions when a large negative gate bias is applied[4]. Punch through leakage occurs when the channel vanishes and current flows between the source and drain regions. When electrons or holes reduce the threshold voltage, hot carrier injection occurs [5].The significance of leakage current in lowering the physical gate length is shown in Figure 3. This plot demonstrates how, as technology has gotten smaller, leakage power dissipation has been increasing at a notably quicker rate [6].

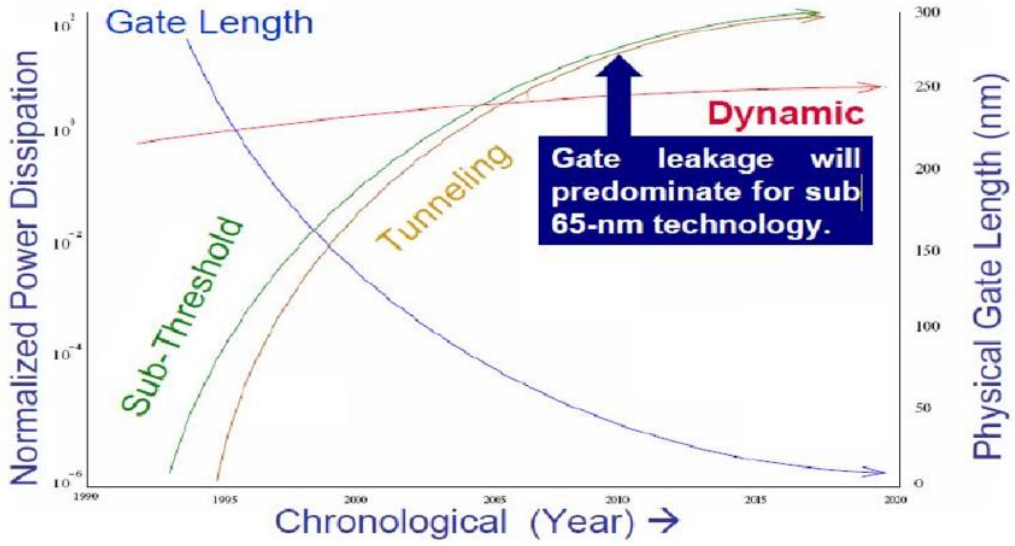

fig.3: latest trends in power dissipation

A professional VLSI designer consistently strives to create an effective leakage reduction method to lower transistor leakage power [7].Transistor stacking is a commonly employed approach in inverters to minimize leakage power [8]. Leakage current calculations are prevalent because of the nonlinear properties of series-connected transistors [9]. Nowadays, VLSI products are improved by extremely advanced CMOS (complementary metal oxide semiconductor) circuit size minimization [10].Controlling the dimensions of a transistor, such as its length, doping profile, junction depth, and, oxide thickness, can reduce leakage. The leakage portion of current rises exponentially and diminishes the physical parameters. The state is saved while the leakage current is suppressed in the active low input mode because each sleeper parallel with stacked transistors is turned off [11]. Static potentiality is primarily used by the ITRS to regulate power reduction. This study suggests an Advance Leakage Method-based static power reduction technique.

II. RELATED WORKS

Chandra et al. [12] explored low-power FINFET SRAM with leakage current reduction techniques to address CMOS scalability challenges. The study revealed that the FinFET-based design significantly reduces dynamic power dissipation by 1.6 times compared to CMOS, with 18% better hold SNM and 26% better RSNM. However, it exhibited a 19% lower write SNM, indicating weaker writing ability. To mitigate this, various leakage current reduction strategies were applied, resulting in a substantial decrease in leakage current and overall power leakage. Despite its notable improvements, the proposed FINFET SRAM faces challenges in maintaining optimal write stability under certain operational conditions.

Kavya Sri et al. [13] emphasize the critical role of low power consumption in modern electronics. They address the escalating issue of leakage power in CMOS circuits, especially as feature sizes decrease. Their paper conducts a comprehensive analysis and comparison of various leakage power reduction techniques, highlighting the dominance of leakage in total power consumption. The proposed Stack ONOFIC method, simulated using Tanner, demonstrates superior power dissipation reduction compared to other circuits, making it especially advantageous for battery-oriented applications. While the Stack ONOFIC method excels in reducing power dissipation, its applicability to extremely high-frequency circuits require further investigation.

Banu et al. [14] addressed the challenge of reducing leakage power in nano-scale VLSI circuits, particularly focusing on 6T Static Random Access Memory (SRAM) cells. The proposed method employs three source biasing techniques—PMOS diode clamping, NMOS diode clamping, and NMOS-PMOS diode clamping—across 45 nm and 90 nm technology nodes. The study highlights the efficacy of PMOS diode clamping, showing an 82.19% reduction in average power compared to other methods. Implementing Multiple Threshold CMOS (MTCMOS) at 45 nm further minimizes leakage. However, the potential sensitivity of the proposed technique to variations in environmental conditions, impacting its universal applicability.

In response to the escalating subthreshold leakage current in small-size CMOS technology, Xu et al. [15] introduced Pileup Effect Transistor (PET) in the CMOS buffer. By reducing voltage differences, PET technology decreased subthreshold leakage current by one-twelfth while maintaining original functionality. Simulations in Cadence and TSMC N65 library demonstrated a 40% reduction in current consumption during state transitions. Despite these promising results, a fictionalized limitation could be that PET technology exhibits sensitivity to extreme temperature variations, requiring further investigation for robust applicability in diverse operating conditions.

Harshey et al. [16] proposed an innovative approach to tackle leakage power in deep submicron and nanometer VLSI circuits. By introducing two strategically placed leakage transistors in the pull-down and pull-up paths, including both PMOS and NMOS transistors, they designed dynamic CMOS inverters and 6T SRAM cells using LECTOR and LECTOR-B methods. Employing Cadence Virtuoso for simulations at the 45-nm technology node, their results indicate a substantial static power reduction, with 26% and 20% improvements for SRAM cells compared to conventional designs. However, the proposed technique faces challenges in scalability to smaller process nodes due to increased sensitivity to process variations.

Mistry et al. [17] investigated clock gating as a prevalent strategy for minimizing dynamic power dissipation in synchronous circuits and reducing wasted power in digital circuits. The study focused on mitigating leakage power in digital CMOS circuitry, employing ONOFIC and LECTOR techniques in D Flip-Flops. Implementation involved optimized transistor sizing based on Logical Effort Theory for enhanced performance. The circuits were contrasted with respect to delay, average power, power-delay product (PDP), and, leakage power, through LT Spice simulations with 65nm PTM technology and a 0.9V power supply. However, the proposed techniques demonstrated limitations in addressing leakage power in complex circuit architectures with multiple interconnected components.

Pathak et al. [18] highlighted persistent leakage current challenges in CMOS technology, particularly in ultra-deep-submicron (UDSM) scaling. Their proposed solution involves adjusting the MOSFET source terminus voltage to minimize leakage currents in nano-scale CMOS circuits with sub-100 nm channel lengths. The technique demonstrated significant reductions, with a 98% decrease in static power and a 30% decrease in total power dissipation for CMOS inverters. Simulation results on NAND and NOR gates revealed total power improvements of 15.90% and 18.88%, respectively. However, the proposed technique's applicability across diverse circuit configurations remains a limitation. Khmailia et al. [19] proposed the VBB stack approach to tackle CMOS inverter standby mode leakage power. Using Variable Body Bias (VBB) and the stack method concurrently, the VBB stack approach reduced power consumption by 23% compared to the conventional approach and 10% compared to the stack approach. The study, conducted on LT Spice, responds to the rising demand for low-power VLSI circuits driven by wireless technology advancements.

Jain et al. [20] emphasized the escalating leakage currents in ultra-deep sub-micron technology, attributing it to size reduction and short-channel effects. Their innovative approach combines lector and drain gating techniques while integrating a variable threshold voltage (VTCMOS) to mitigate sub-threshold current. The designed logic gates exhibit improved static power consumption and average propagation delay. Comparative analysis against existing methods showcases a 48% reduction in power consumption for the drain gating NOR gate and a 20% decrease for the sleepy lector NOR gate in 32nm technology.

Jayaram et al. [21] introduced a novel approach to clock generation for on-chip IC applications, utilizing a four-transistor inverter cell within a Five-stage ring oscillator. With a focus on minimizing power dissipation, the proposed circuit achieved a signal frequency of 10 MHz at 27°C, exhibiting a frequency range from 9.59 to 10.8 MHz over a temperature range of −40°C to 125°C. Simulated in standard CMOS 180nm technology, the results demonstrated a substantial power consumption reduction to 5.56 MW at 1V, marking a remarkable 45% improvement compared to conventional ring oscillators.

III. METHODOLOGY

Low power, combined with high efficiency and great density, is a key consideration in today's VLSI circuits. Although there are a number of methods to lower leakage power, their application is constrained by their respective drawbacks. Basic to every digital circuit design is the inverter. Developing increasingly intricate circuits requires a thorough grasp of its behavior. It generates and receives one single input. A complementary and symmetrical pair of PMOS blocks arranged on the circuit as a pull-up network (PUN) and an NMOS block connected as a pull-down network (PDN) typically make up a CMOS logic circuit as shown in figure 4. A pair of complementary transistors linked to a single input makes up a traditional CMOS inverter.

The behavior of transistors in active mode is similar to that of switches. The PMOS transistor is conductive and functions as a closed switch when the input is at low logic level (0). The current travels from the V_{DD} supply to the output. The PMOS transistor cuts off, severing the output from the positive voltage V_{DD}, and the N-MOS transistor, which is conductive and functions as a closed switch, pulls the output to low level (0) when the inverter input is at high logic level (1).Reduced transistor size results in a shortening of the gate oxide and the channel length, which can cause leakage or static power.

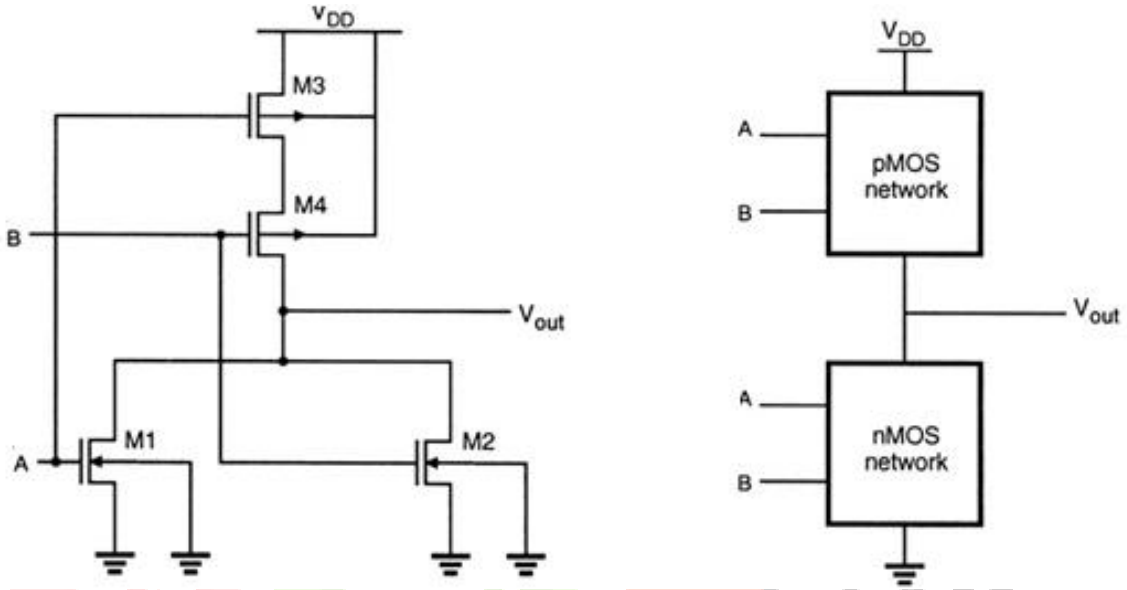

Fig.4: Basic CMOS Inverter

According to VLSI designers, as technology continues to reduce, static power may eventually account for the majority of the overall power needed by CMOS devices.

$$P_{static} = V_{dd} * I_{leakage} \quad (1)$$

The leakage current in standby mode is represented by $I_{leakage}$. A major part of the leakage current is caused by the subthreshold current.

$$I_{sub} = I_{sub0} e^{\frac{V_{gs}-V_{th}}{nV_T}} \left[1 - e^{\frac{-V_{ds}}{V_T}}\right] \quad (2)$$

3.1.Stack Technique

Using the stack technique, two half-width PMOS or NMOS transistors are employed in place of one for each PMOS or NMOS transistor [22]. These two transistors are wired in series, either PMOS or NMOS. The schematic of a stack-based two-input NOR gate is shown in Figure 5. This Stack NOR gate uses four PMOS and four NMOS transistors, as opposed to the two PMOS and two NMOS transistors used in a simple CMOS NOR gate.

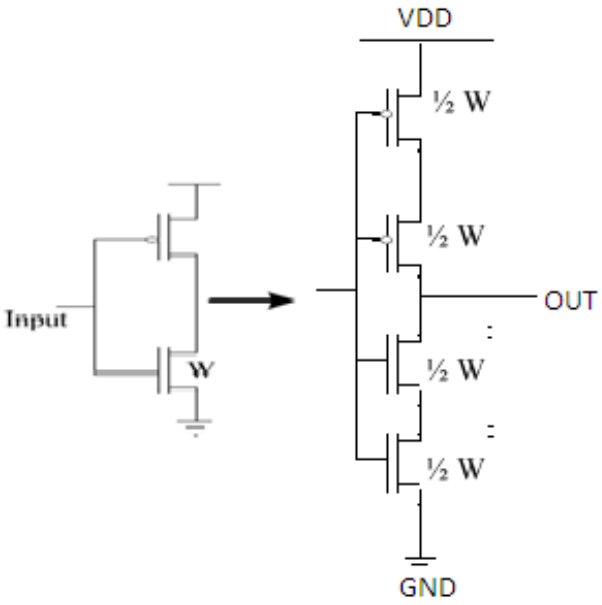

Fig.5: Stack NOR Gate

3.2.LECTOR Technique

The fundamental concept of the LECTOR method is that "A state with more than one transistor OFF in a path from supply voltage to ground is far less leaky than a state with only one transistor OFF in any supply to ground path". The stack effect is the only underlying principle of this method. Between the pull-down and pull-up networks, two more transistors—one PMOS and one NMOS—are added using this design. Leakage control transistors (LCTs) are the self-regulating transistors that these two are [23]. Each LCT's gate is governed by the other's source. One of the LCTs also consistently stays in its near cut off region as a result of this configuration.

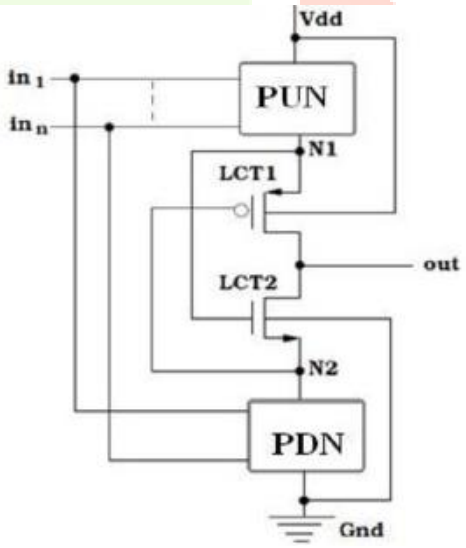

Fig.6: LECTOR approach

This method places two transistors between PUN as well as PDN and uses them to control leakage. The power sources of each transistor alter the gate of the other transistor. The essential component of this technique for minimizing drainage is the stacking effect of both transistors across the supply and the ground. In Figure 6, the LECTOR technique is displayed. The basic principle of the LECTOR approach is shrinking the static potentiality by sandwiching these NMOS between PUN and PDN. We chose the LECTOR approach over other CMOS-based logic circuits for study.

3.3.Source Biasing Approach

Our main goal is to apply this method—increasing the transistor's V_s by lowering its static current—in order to reduce leakage power and achieve our goal. Subthreshold current and V_{th} have an inverse relationship; that is, if we lower V_{th}. Subthreshold current increases exponentially at a given value.Increases in MOS source station voltage, commonly referred to as source biasing, are used to decrease V_{ds}. CMOS inverters are used to achieve this technique.Applying '0' as an input will cause both NMOS to turn off, and the output will be '1'.

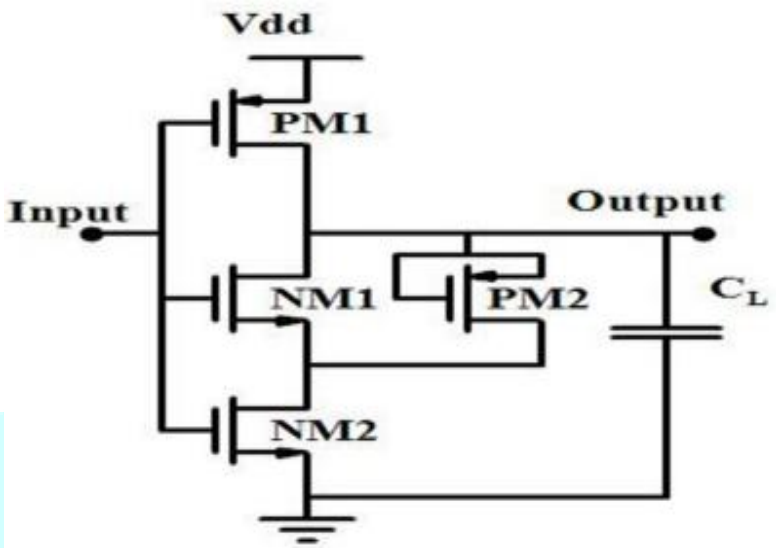

Fig.7: Mechanism of Source Biasing

Apart from PMOS, NMOS is also employed, denoted as NM2 that is connected directly to the static current provided by the preceding transistor. Since PM2, a different P type MOS transistor depicted in Figure 7, creates a specified amount of potential at the primary terminal, or source, and supplies static current, it stays in cut off mode.

3.4.Stack ONOFIC Approach

This method, as the name implies, involves stacking transistors in order to lower the static power [24]. The gate terminal of the PMOS (M6) is connected to the output, and the gate of the two NMOS joins the right side PMOS as shown in figure 8. When used in the OFF state, this approach offers an enormous resistance; in the ON state, it produces a small resistance. It modifies the CMOS circuit's overall power consumption and propagation latency.

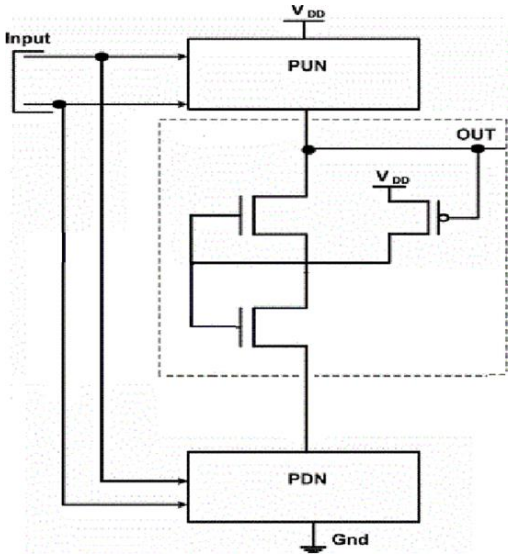

Fig.8: Stack ONOFIC Model

3.5.Proposed Approach

Two transistors, one NMOS (M3) and the other NMOS (M4), are placed between the pull-up and pull-down networks in this approach. The pull-down network's transistor (M2), PMOS (M4), and NMOS (M3) substrate portions are all connected to one another. Additionally, we added two more transistors to the right side of the circuit that was previously described: an NMOS (M5) and a PMOS (M6) as shown in figure 9. These transistors have connected gates to the output and connected substrates.The ground is connected to the PMOS(M6) source.

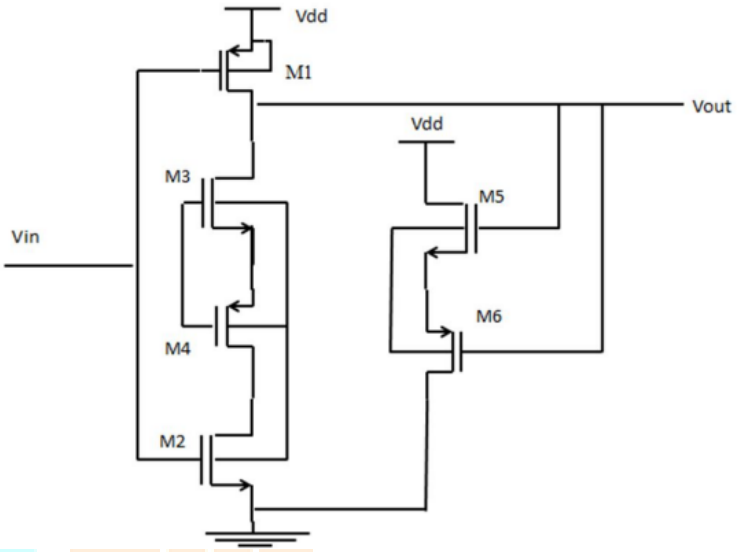

Fig.9: Proposed Technique for CMOS inverter

IV. RESULTS AND DISCUSSION

By employing this technique, we were able to drastically reduce the leakage power of the CMOS circuits. Using this technique, the CMOS inverter is presented and the outcomes for NOR and NAND gates are also drawn as shown in figure 10.

Fig.10: Waveforms of CMOS inverters

By modeling CMOS logic circuits utilizing 180nm technology in LT Spice Tool, the static power was measured in nW. This method reduces the leakage power by fifty percent. The supplied voltage, V_{DD}=1.8V, is 180 nm for length and 360 nm for width. And lastly analysis of the operating point is observed. Leakage power dissipation shown for tabular data 1 is presented in Figure 11 utilizing 180nm technology.

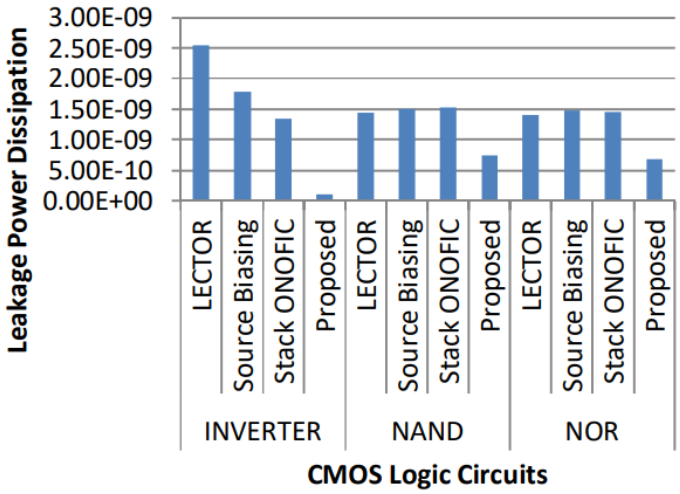

Fig.11: Power dissipation leakage

The plot of delay for the tabular data below, utilizing 180nm technology, is shown in Figure 12.

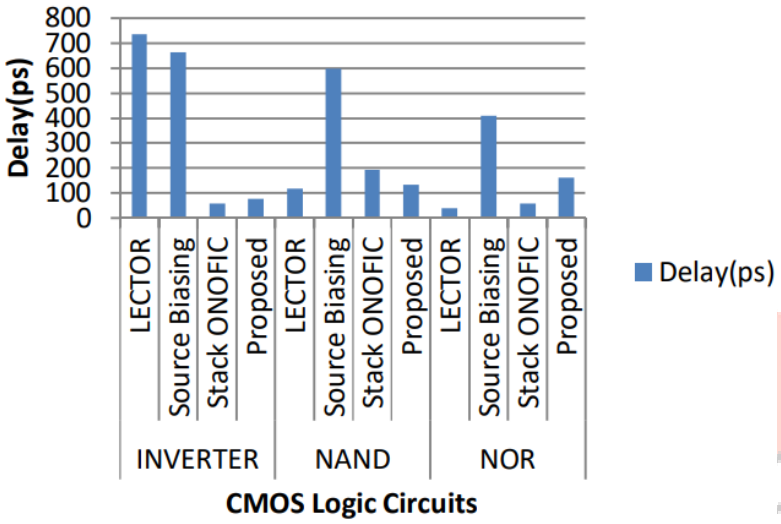

Fig.12: Delay plot

Table.1: Static Power Consumption Of 180nm Technologies-Based CMOS Logic Devices

Circuit Type	Technique	Power Consumption (watts)	Propagation Time (ps)
INVERTER	LECTOR	2.54E-09	736.781
	Source Biasing	1.78E-09	661.414
	Stack ONOFIC	1.34E-09	57.388
	Proposed	1.12E-10	76.3
NAND	LECTOR	1.45E-09	117.14
	Source Biasing	1.50E-09	597.29
	Stack ONOFIC	1.53E-09	192.931
	Proposed	7.46E-10	132.23
NOR	LECTOR	1.40E-09	40.723
	Source Biasing	1.48E-09	410.01
	Stack ONOFIC	1.46E-09	57.388
	Proposed	6.86E-10	162.456

V. CONCLUSION

The proposed study has delved into the critical realm of power consumption in semiconductor devices, particularly focusing on VLSI circuits, where power efficiency is imperative for the ever-growing demand for portable and energy-conscious electronic devices. The investigation highlighted the escalating significance of leakage power, constituting up to 50% of the total power consumption in contemporary high-performance microprocessors. Acknowledging the challenges posed by scaling CMOS devices, the study explored various leakage reduction methods, including the Stack Technique, LECTOR Technique, Source Biasing Approach, Stack ONOFIC Approach, and the Proposed Approach. The proposed Advance Leakage Method, in particular, emerged as a promising avenue for mitigating leakage power, exhibiting a substantial 50% reduction in power consumption. Through the meticulous analysis of CMOS inverter models and tabulated results, our study has contributed valuable insights into the trade-offs between power consumption and performance in different circuits and techniques. This research not only addresses the current challenges posed by leakage power but also provides a foundation for future advancements in low-power VLSI circuit design. As the semiconductor landscape continues to evolve, the findings presented here pave the way for more energy-efficient electronic devices, aligning with the ever-growing demands for sustainability and user reliability in the field of integrated circuit applications.

REFERENCES

[1] Stillmaker, A., & Baas, B. (2017). Scaling equations for the accurate prediction of CMOS device performance from 180 nm to 7 nm. Integration, 58, 74-81.
[2] Kakkar, R., Goyal, S., Singh, J., Khosla, D., & Singh, S. (2022). IMPLEMENTATION AND MODELING OF LOW POWER SLEEPY STACK SRAM. Journal of Advanced Sciences, 1(1).
[3] Farzan Fallah, Massoud Pedram "Standby and Active Leakage Current Control and Minimization in CMOS VLSI Circuits" in IEICE Transactions,2005, pp.509-519.
[4] Kaushik Roy, Hamid Mahmoodi -Meimand and Saibal Mukhopadhyay "Leakage current mechanisms and leakage current reduction techniques in Deep submicrometer CMOS circuits,"Proceedings of IEEE,vol.91,No.2,Feb 2003.
[5] NdubuisiEkekwe, Ralph Etienne-Cummings, "Power dissipation sources and possible control techniques in ultra deep submicron CMOS technologies" Microelectronics journal37,2006, pp.851-860.
[6] J. Xue, T. Li, Y. Deng and Z. Yu, "Full-chip leakage analysis for 65 nm CMOS technology and beyond", Integration, the VLSI Journal, Vol. 43 (4), pp. 353-364, 2010.
[7] Preeti Verma and R.A. Mishra, "Leakage power and delay analysis of LECTOR based circuits", ICCCT, 2011
[8] A. Rjouband M. Al-Ajlouni," Efficient multi-threshold voltage techniques for minimum leakage current in nanoscale technology," Int. J. Circuit Theory Appl., vol. 39, 1049, 2011
[9] Dr. B.T. Geetha,et.al, " Design Methodologies and Circuit Optimization Techniques for Low Power CMOS VLSI Design", ICPCSI, 2017
[10] V. K. Sharma, S. Patel and M. Pattanaik," High Performance Process Variations Aware Technique for Sub- threshold 8T-SRAM Cell," Wireless Pers. Commun., vol. 78, 57, 2014
[11] Marc Belleville, Olivier Thomas, Alexandre Valentian and Fabien Clermidy," Designing digital circuits with nano- scale devices: challenges and opportunities," Solid-State Electronics, vol. 84, pp. 38-45, June 2013.
[12] Chandra, K. S., & Kishore, K. H. (2023). Design and Analysis of Low Power FinFET SRAM with Leakage Current Reduction Techniques. Wireless Personal Communications, 1-22.
[13] SRI, C. K., & KUMAR, M. C. A. ANALYSIS AND COMPARISON OF LEAKAGE POWER REDUCTION TECHNIQUES FOR VLSI DESIGN.
[14] Banu, S., & Gupta, S. (2022). Design and Leakage Power Optimization of 6T Static Random Access Memory Cell Using Cadence Virtuoso. IJEER, 10(2), 341-346.
[15] Xu, H. (2022, December). A Method for Leakage Current and Power Reduction of Buffer in 65-nm CMOS Technology Based on the Pileup-Effect. In Journal of Physics: Conference Series (Vol. 2383, No. 1, p. 012055). IOP Publishing.
[16] Harshey, V., Das, P. K., & Sharma, S. LOW POWER DYNAMIC CMOS INVERTER AND SRAM CELL DESIGN USING LECTOR AND LECTOR-B TECHNIQUE.
[17] Mistry, T., & Yadav, S. (2022, August). Analysis of Leakage Power Reduction Using LECTOR and ONOFIC Technique in Clock Gated Flip-Flop. In 2022 2nd Asian Conference on Innovation in Technology (ASIANCON) (pp. 1-7). IEEE.

[18] Pathak, P., &Kourav, S. (2022). A Circuit Approach for CMOS VLSI Circuit Leakage Power Reduction.

[19] Khmailia, S., Rouabeh, J., & Mami, A. (2022). Design of a Low Power CMOS Inverter with the VBB Stack Approach. Engineering, Technology & Applied Science Research, 12(4), 8891-8895.

[20] Jain, A., & Ghosh, A. (2022, December). A Novel Circuit technique for Leakage Reduction in Ultra Deep Sub-Micron CMOS Technology. In 2022 3rd International Conference on Communication, Computing and Industry 4.0 (C2I4) (pp. 1-5). IEEE.

[21] Jayaram, C., & Rao, P. S. (2022, December). A 10-MHz CMOS-based Ring Oscillator with Low Power consumption For On-chip IC Applications. In 2022 IEEE International Symposium on Smart Electronic Systems (iSES) (pp. 53-56). IEEE.

[22] Saxena, N., & Soni, S. (2013). Leakage current reduction in CMOS circuits using stacking effect. International Journal of Application or Innovation in Engineering & Management, 2(11), 213-216.

[23] Surendra, C. S., & Yashwanth, N. (2023, October). Design and implementation of a Low power Adder Circuit Using LECTOR Technique. In Journal of Physics: Conference Series (Vol. 2571, No. 1, p. 012028). IOP Publishing.

[24] Priyanka, M. S., Manikanta, G., Bhaskar, K., Ganesh, A., & Swetha, V. (2017). High Performance and Low Power VLSI CMOS Circuit Design Using ONOFIC Approach. ISSN, 7, 71-76