IJCRT.ORG ISSN : 2320-2882

INTERNATIONAL JOURNAL OF CREATIVE RESEARCH THOUGHTS (IJCRT)

An International Open Access, Peer-reviewed, Refereed Journal

MODELING, ANALYSIS AND IMPLEMENTATION OF AN IMPROVED INTERLEAVED BUCK-BOOST CONVERTER

[1]Vinothkumar V, [2]Kanishka P, [3]Sujith M, [4]Nithya G

[1]B.E-Final Year Student, [2]B.E-Final Year Student, [3] B.E-Final Year Student, [4]Assistant Professor

[1]Department of Electrical and Electronics Engineering,

[1]Bannari Amman Institute of Technology, Sathyamangalam, India.

Abstract: The proposed paper analyses and models an interleaved Buck-Boost conversion using a PID controller. The Buck-Boost voltage converter is becoming prevalent in many applications due to the increasing need for energy. These methods have a broad variety of applications, including fuel cell power systems, solar energy systems (PV), uninterruptible electrical supplies (UPS), and electric vehicles. The BBC is still a crucial part of many technological systems, despite the issues. Because of its capacity to efficiently change voltage levels, it is helpful in many systems mentioned earlier. Researchers are still working to push beyond its boundaries and realize its full promise in a number of fields. Researchers have examined a variety of ways to address the issues of input current ripple, transient response, and efficiency to improve the performance of the BBC. This converter's capacity to be operated through shifting signals that are interleaved, have the identical frequency, but various phases, makes it stand out from other converters. The simultaneous operation of converters, which disperse current from the input across inductors, results in increased effectiveness and dependability in power electronics and also a reduction in ripples. This synergy considerably boosts the converter's conversion performance. The control approach for this converter is PID-based. In this work, we thoroughly simulate the interleaved Buck-Boost converter while carefully highlighting the results attained with the PID controller method was used.

Keywords **- PID Controller, interleaved, Buck-boost, Ziegler-Nichols Tuning, efficiency, performance.**

I. INTRODUCTION

The process of interleaving, often referred to as multiphasing, is effective for reducing the measurement of filter components. Multiple power switches are used in interleaved circuits, with a crucial phase difference of 180 degrees between two switches. The interleaving strategy systematically connects many changing cells by coordinating a number of discrete sources with comparative phase shifts, raising the optimal pulse frequency. This technique is important for improving converter performance, taking into account factors including size, conductivity, and electromagnetic emissions [1]. Interleaving also offers benefits including increased power capacity, adaptability, and improved dependability. However, using interleaving could result in the extra expenses related to output rectifiers, Inductors, capacitors, and electrical switchgear. Although many energy losses in an electromagnetic component that are reduced by using bigger inductors, minimal energy loss and low form factors are still in demand. The use of this interleaving dates back to the early days of high-power electronics, notably in high-end energy applications. Power electronics may not be able to handle the current as well as the voltage stresses in applications that require high power. One solution is to link many power sources in parallel or series. However, a better strategy includes parallelizing power converters rather than power devices [2]. Interleaving happens naturally as a result of this. Harmonics are successfully reduced by interleaving, and efficiency is improved along with high energy density and efficient thermal efficiency. It is common practice in high-power applications to parallelize converter power stages in order to use more compact power converters and inductive devices to provide the required output power. Parallelization distributes temperature stresses and losses of electricity across semiconductors in addition to the physical distribution of the given magnetic components and the corresponding energy losses and thermal tensions since each paralleled energy stage has a lower power burden. The elimination of "hotspots" in power supply is therefore made possible through parallelization [9]. Additionally, paralleling enables the use of quicker, lower power semiconductor switches in individual power stages, which may result in switching rates that are greater than those seen in equivalent single high-power processing stages. As a result, paralleling offers a chance to make magnetic components smaller [10]. The important goal of PID controller model is to manage the cycle of duties of the Interleaved Buck inverter switch such that the voltage if the baseline voltage for the resultant DC part is zero. Despite changes in input voltage or load, this regulation must not change [3]. The constrained duty cycle, which ranges from zero to one, also places limitations on controller design. The solution to this issue is to model the proposed Interleaved inverter by incorporating the technique of field average for states strategy.

II. FLOW DIAGRAM OF THE PROPOSED DC-DC CONVERTER MODEL

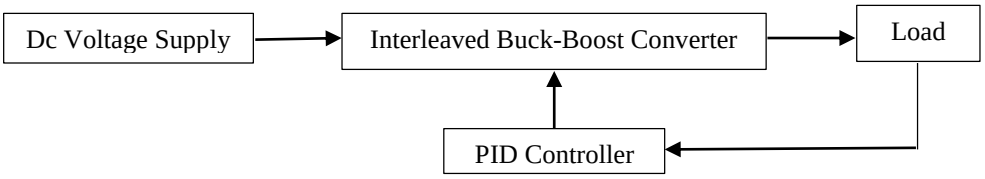

Fig. 1: Flow diagram of the proposed interleaved dc-dc converter

The detailed schematic representation of the proposed converter with a PID control system is represented in Figure 1 [8]. The proposed converter, which has two individual conventional converters stacked in parallel, receives a DC power source. By dividing the current across the two switches, this parallel arrangement significantly reduces current strains. A PID algorithm controls the feedback loop before the planned converter output is transmitted to the load being controlled [3]. The Ziegler-Nichols tuning technique is implemented by the PID controller, which uses the DC power source as its input. By implementing the PID controller, the number of harmonics and disturbances is minimal. The output that has less voltage ripple is then delivered to the load after being fed back into the converters.

III. PROPOSED METHODOLOGY

A. Conventional Model for DC-DC Converter

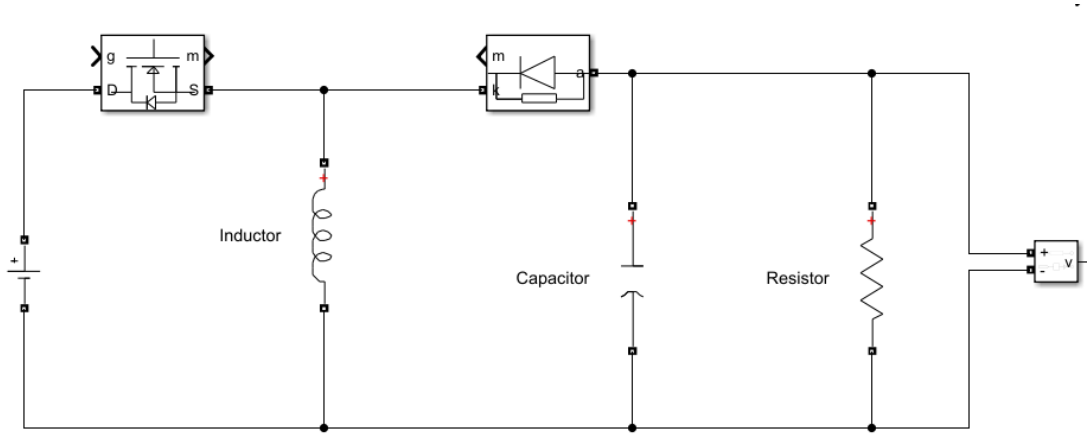

Fig. 2: Conventional design for buck-boost regulator

The circuit schematic for a standard traditional buck-boost converter, which is frequently employed for DC-DC voltage converting applications, is represented in Figure 2. Then output side of a traditional buck-boost inverter either increases or decreases the DC supply potential [6]. Considering the electrical polarity of the inductor changes as it is discharged, the charge of the generated voltage is precisely the reverse of the polarity of the source supply. Another name for it is an inverting converter. Although, the traditional DC-DC converter's key benefit is its greater effectiveness. For that, the following formulae is considered to calculate the converter's transformer value L also the value of a capacitor C.

$$Vo = -Vs*D/(1-D) \quad (1)$$

$$L = Vs*D/ (\Delta I_L*f_s) \quad (2)$$

$$C = Io*D/ (\Delta V_C* f_s) \quad (3)$$

$$Ro = Vo/Io \quad (4)$$

$$\eta = V_{out}/V_{in} \quad (5)$$

Where Vo represents the converter's resulting voltage, The value of its duty cycle is D, its toggle frequency is fs, its inductance rippling current is il, and its inductance and capacitance values are L and C, Ro is its load-side resistor, is its converter efficiency, and Pout and Pin are its output and input powers.

B. Converter Design for the Proposed Interleaved DC-DC Converter

The interleaved DC-DC inverter is made up of two different converters that are linked in parallel. The switching signals in this interleaved form display a 180o phase divergence from one another [8]. Essentially, the interleaved configuration is made up of two independent buck-boost shifting units. The shift-close and shift-open phases are two separate switching phases that are included in every one of these boost shift units [7]. The inductor's current starts to increase while the diode blocks during the switch-close phase. It starts the inductor's charging. The inductive component then starts discharging while in the switch-open

period, sending the electrical current flowing through the transistor to the electrical load [5].

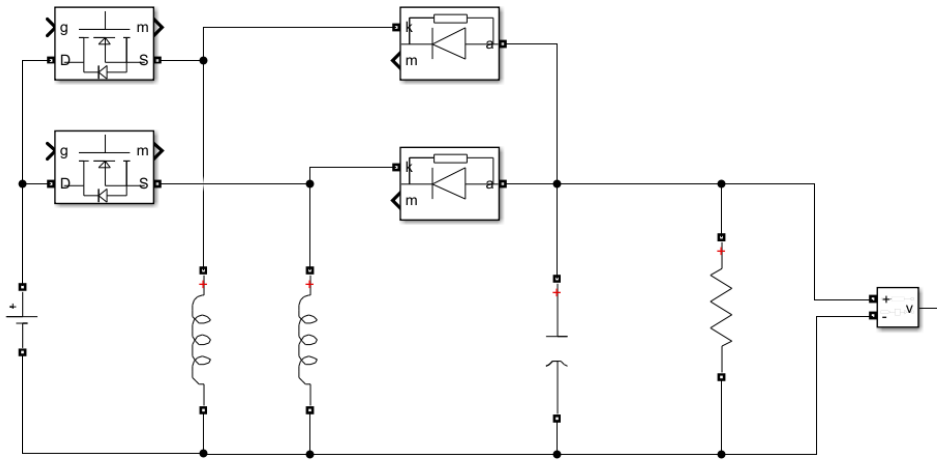

Fig. 3: Converter model of the proposed interleaved dc-dc converter

The L as well as C parameters for this regulator may also be determined using the following formula. The nominal values of the inductive component L and the capacitance C are identical as the typical converter based on formulas (2), (3), (6), and (7).

$$L1 = L2 = Vs*D/ (\Delta I_L*f_s) \quad (6)$$

$$C = Io*D/ (\Delta V_C* f_s) \quad (7)$$

The following table lists the interleaved buck-boost converter's determined design parameters:

Table 1. Design parameters for the proposed Converter

S. No.	Parameters	Symbols	Values
1.	Supply voltage	V_{in}(min) & V_{in}(max)	12V – 18V
2.	Output Voltage	V_{out}	-15V
3.	Output Power	Pout	22.5W
4.	Inductance	L1 & L2	$250e^{-6}$ H
5.	Capacitance	C	$470e^{-6}$ F
6.	Switching Frequency	f_w	50k Hz
7.	Ripple Voltage for Capacitor	ΔV_C	0.03
8.	Ripple Current for Inductor	ΔI_L	0.25
9.	Load Resistance	Ro	10Ω

IV. THEORITICAL MODELING OF THE PROPOSED CONVERTER

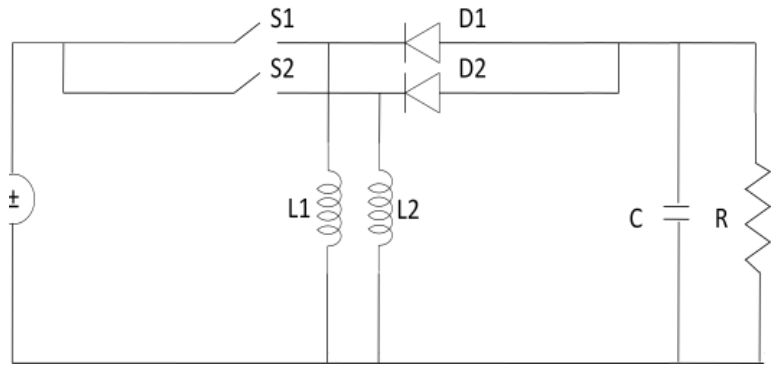

Fig. 4: Circuit diagram of the proposed converter

When the Switching devices are ON:

$$v_{in} = \mathrm{L}\frac{\mathrm{di}}{\mathrm{dt}} \quad (8)$$

$$\frac{di}{dt} = \frac{v_{in}}{L} \quad (9)$$

$$i_L + i_o = 0 \quad (10)$$

$$\frac{dv}{dt} = -\frac{v_c}{RC} \quad (11)$$

$$\begin{bmatrix} i_L \\ v_c \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} v_{in} \quad (12)$$

When the switches are off

$$v_L + v_c = 0 \quad (13)$$

$$\frac{di}{dt} = -\frac{v_C}{L} \quad (14)$$

$$-i_L + i_C + i_o = 0 \quad (15)$$

$$C\frac{dv}{dt} = i_L - \frac{v_C}{R} \quad (16)$$

$$\begin{bmatrix} i_L \\ v_c \end{bmatrix} = \begin{bmatrix} 0 & \frac{1}{L} \\ \frac{-1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} v_{in} \quad (17)$$

From equation (12) & (17)

$$A_1 = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix} \quad (18)$$

$$A_2 = \begin{bmatrix} 0 & \frac{1}{L} \\ \frac{-1}{C} & -\frac{1}{RC} \end{bmatrix} \quad (19)$$

$$B_1 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \quad (20)$$

$$C = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \quad (21)$$

Where $C=C_1 = C_2$

$$A = A_1D + A_2(1-D) \quad (22)$$

$$A = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{D}{RC} \end{bmatrix} + \begin{bmatrix} 0 & \frac{(1-D)}{L} \\ \frac{-(1-D)}{C} & -\frac{(1-D)}{RC} \end{bmatrix} \quad (23)$$

$$A=\begin{bmatrix} 0 & \frac{(1-D)}{L} \\ \frac{-(1-D)}{C} & \frac{-1}{RC} \end{bmatrix} \quad (24)$$

$$y(s) = C\left[[SI-A]^{-1}[A_1-A_2]X + [B_1-B_2]V_g\right]d(s) + [C_1-C_2]xd(s) \quad (25)$$

$$I=\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \quad (26)$$

$$SI=\begin{bmatrix} S & 0 \\ 0 & S \end{bmatrix} \quad (27)$$

$$SI\text{-}A=\begin{bmatrix} S & 0 \\ 0 & S \end{bmatrix}-\begin{bmatrix} 0 & \frac{(1-D)}{L} \\ \frac{-(1-D)}{C} & \frac{-1}{RC} \end{bmatrix} \quad (28)$$

$$SI\text{-}A=\begin{bmatrix} S & \frac{-(1-D)}{L} \\ \frac{(1-D)}{C} & S+\frac{1}{RC} \end{bmatrix} \quad (29)$$

$$[SI\text{-}A]^{-1}=\frac{1}{s\left(s+\frac{1}{RC}\right)+\frac{(1-D)^2}{LC}}\begin{bmatrix} S+\frac{1}{RC} & \frac{(1-D)}{L} \\ \frac{-(1-D)}{C} & S \end{bmatrix} \quad (30)$$

$$A_1-A_2=\begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix}-\begin{bmatrix} 0 & \frac{1}{L} \\ \frac{-1}{C} & -\frac{1}{RC} \end{bmatrix} \quad (31)$$

$$A_1-A_2=\begin{bmatrix} 0 & \frac{1}{L} \\ \frac{-1}{C} & 0 \end{bmatrix}\begin{bmatrix} i_L \\ v_c \end{bmatrix} \quad (32)$$

$$B_1-B_2=\begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}-\begin{bmatrix} 0 \\ 0 \end{bmatrix} \quad (33)$$

$$B_1-B_2=\begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}v \quad (34)$$

$$\text{Where } [A_1-A_2]X+[B_1-B_2]v_g=\begin{bmatrix} \frac{-v_c}{L} \\ \frac{i_L}{L} \end{bmatrix}+\begin{bmatrix} \frac{dv}{L} \\ 0 \end{bmatrix} \quad (35)$$

When v_g is consider

$$[A_1-A_2]X+[B_1-B_2]v_g=\begin{bmatrix} -\frac{v_c}{L}+\frac{dv}{L} \\ \frac{i_L}{L} \end{bmatrix} \quad (36)$$

$$y(s)=\frac{1}{s\left(s+\frac{1}{RC}\right)+\frac{(1-D)^2}{LC}}\begin{bmatrix} S+\frac{1}{RC} & \frac{(1-D)}{L} \\ \frac{-(1-D)}{C} & S \end{bmatrix}\begin{bmatrix} -\frac{v_c}{L}+\frac{dv}{L} \\ \frac{i_L}{L} \end{bmatrix} \quad (37)$$

$$y(s)=\begin{bmatrix} \left(S+\frac{1}{RC}\right)\left(-\frac{v_c}{L}+\frac{dv}{L}\right)+\left(\frac{i_L}{L}\right)\left(\frac{(1-D)}{L}\right) \\ \left(\frac{-(1-D)}{C}\right)\left(-\frac{v_c}{L}+\frac{dv}{L}\right)+\left(\frac{i_L}{L}\right)S \end{bmatrix} \quad (38)$$

When v_g=0

$$C=[0 \quad 1] \quad (39)$$

$$y=[0 \quad 1]\begin{bmatrix} i_L \\ v_c \end{bmatrix} \quad (40)$$

$$y=v_c \quad (41)$$

$$[B_1-B_2]v_g=0 \quad (42)$$

$$C[[SI-A]^{-1}[A_1-A_2]X] \quad (43)$$

$$y(s)=\frac{1}{s\left(s+\frac{1}{RC}\right)+\frac{(1-D)^2}{LC}}\begin{bmatrix}0 & 1\end{bmatrix}\begin{bmatrix}S+\frac{1}{RC} & \frac{(1-D)}{L}\\ \frac{-(1-D)}{C} & S\end{bmatrix} \quad (44)$$

$$y(s)=\begin{bmatrix}\frac{-(1-D)}{C} & S\end{bmatrix}\begin{bmatrix}-\frac{v_{c+Dv}}{L}\\ \frac{i_L}{L}\end{bmatrix} \quad (45)$$

$$y(s)=\frac{-(1-D)}{C}+\frac{(Dv-1)}{L}+\frac{i_L}{L}S \quad (46)$$

$$y(s)=\frac{-(Dv-v_c-D^2v+D)}{LC}+\frac{i_L}{L}S \quad (47)$$

The derived interleaved DC-DC converter's computed CTO function is shown below.

$$y(s)=\frac{\frac{(D^2v+D(v-1)-v_c)}{LC}+\frac{i_L}{L}S}{s^2+\frac{S}{RC}+\frac{(1-D)^2}{LC}} \quad (48)$$

V. CONTROLLER MODELING

Figure 5 shows the PID controller based closed-loop control system diagram with a controller that uses PID feedback.

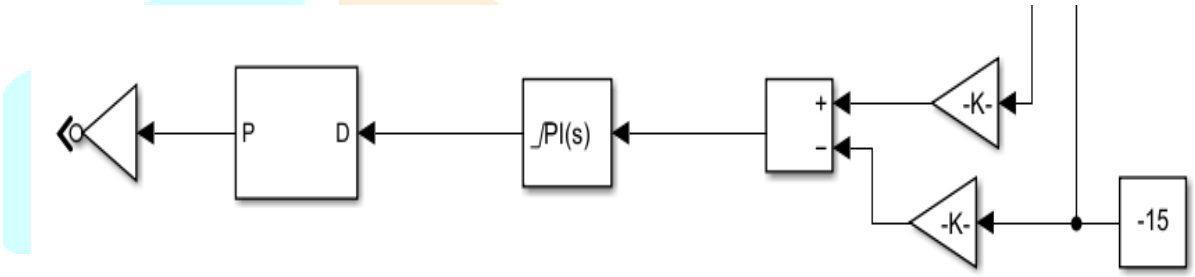

Fig. 5: PID controller matlab design

In buck-boost conversion devices, the use of a PID (Proportional-Integral-Derivative) controller is a common feedback control method used to manage and stabilize the output voltage. It works by continually computing a value for error as a variance among the baseline voltage, the intended setpoint, and the actual outcome voltage, determined by the process variable [4]. The control action, in this case the operation cycle of the switchable component of the proposed DC-DC converter, is, so adjusted using this error value in order to minimize the error. The PID controller's component formulae in detail are as follows:
The output value produced by the proportional (P) term is proportionate to the current error value. It decides how to react right away if the mistake changes. In mathematics, it is denoted by:

$$P(t) = Kp * e(t) \quad (49)$$

In this case,
P(t) represents the proportional element at time t.
Kp, a constant that controls the intensity of the proportional reaction, is the proportional gain.
The mistake that occurred at time t is represented by the expression e(t)**, where e(t)** = setting - process variable.

The word integral (I) deals with the gradual accumulation of prior mistakes. It gets rid of the steady-state inaccuracy that the proportional term can't fix on its own.

$$I(t) = Ki * \int(e(\tau)\, d\tau) \quad (50)$$

Where:

The integral phrase at the time t is denoted by I(t).
The integral gain, or Ki, controls how much the controller reacts to previous mistakes.
The value of the integral of the mistake over time from the beginning to time t is represented as "(e() d"."

Based on the pace at which the error has been evolving, the derivative (D) term forecasts the error's future behaviour. It aids in foreseeing and preventing the buildup of subsequent errors. It may be calculated mathematically as follows:

$$D(t) = Kd * de(t)/dt \quad (51)$$

Where:
The derived term at time t is D(t).
Kd is the derivation gain, which regulates how the change of mistake variation affects the desired outcome.
The error's rate of change over time is shown by the formula de(t)/dt.

The total of the following three variables represents the control output:

$$PID(t) = P(t) + I(t) + D(t) \quad (52)$$

The performance of the controller relies on adjusting the PID values (Kp, Ki, Kd) to get the response you want, which is a quick reaction with little overflow and error in the steady-state. The performance of the PID algorithm in the interleaved DC-DC converter system may be tuned using a variety of techniques, including Ziegler-Nichols or trial-and-error.

Table 2. Ziegler-Nichol tuning method for PID controller

Type of Controller	K_p	T_i	T_d
P	$0.5\ K_{cr}$	∞	0
PI	$0.45\ K_{cr}$	$1/1.2\ P_{cr}$	0
PID	$0.6\ K_{cr}$	$0.5\ P_{cr}$	$0.125\ P_{cr}$

VI. RESULTS AND DISCUSSION

With the help of MATLAB/SIMULINK, the proposed interleaved converter's anticipated closed-loop performance has been emulated. The major goal is to create a robust controller that can retain stability despite uncertainty and significant load variations. The designed interleaved dc-dc converter can be tested in the Matlab/Simulink simulation atmosphere, which enables you to assess the system's efficiency, validate the controlling algorithm, and refine the controller's settings for robustness. This greatly aids in the analysis of the explained performance under various conditions. The diagram of the newly proposed alternating converter with a feedback controller using a PID.

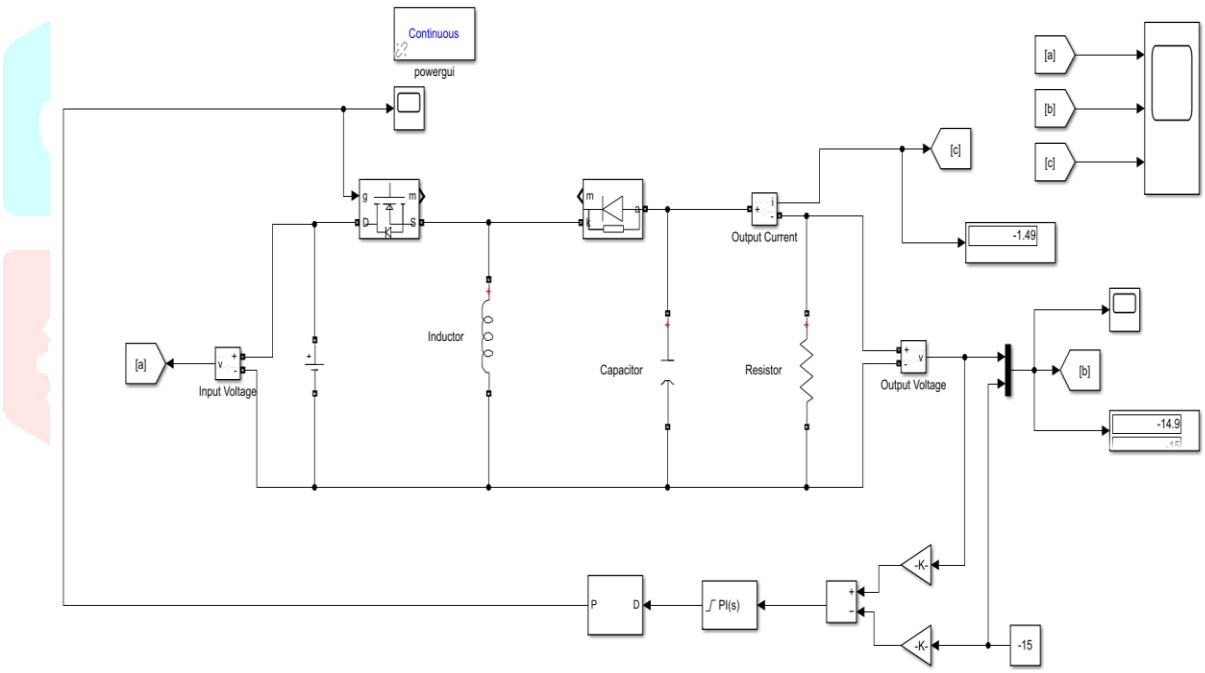

Fig. 6: Circuit model of conventional dc-dc converter

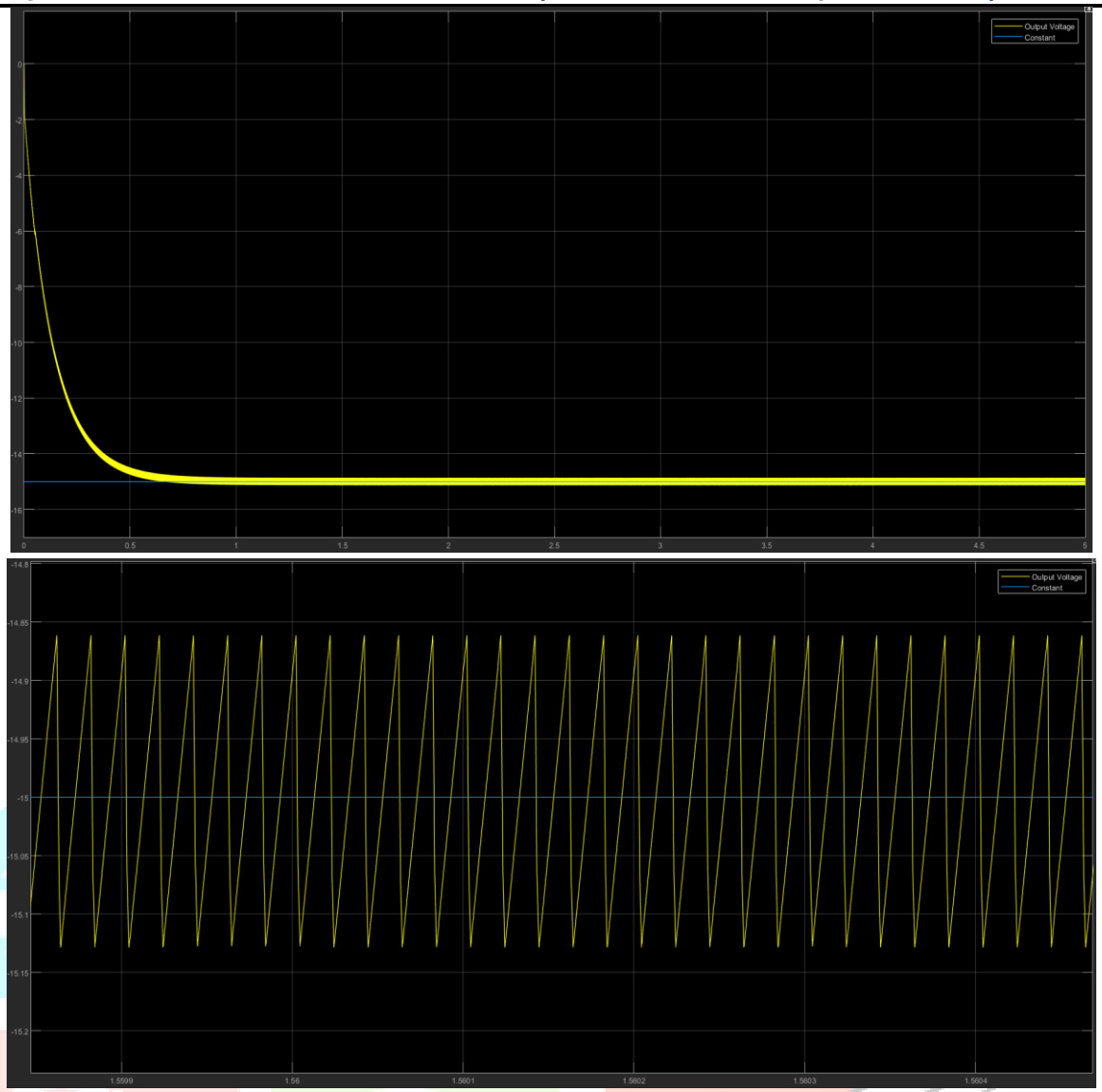

Fig. 7 Simulation output voltage waveforms of traditional dc-dc converter

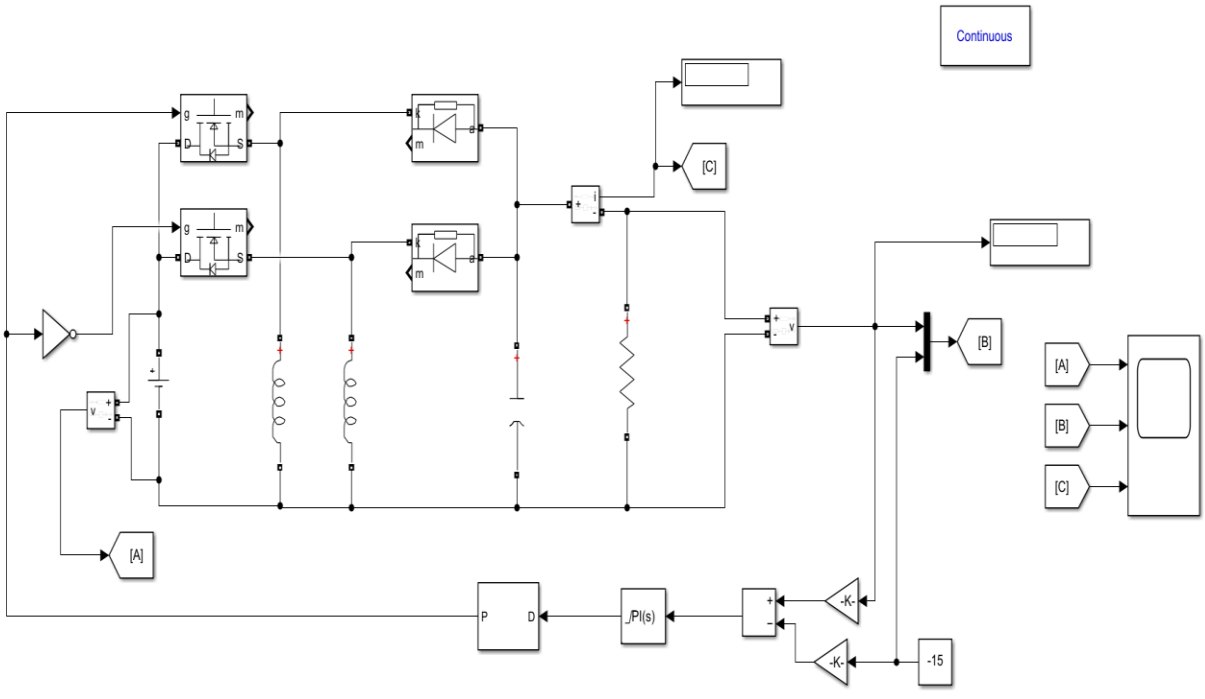

Fig. 8: Circuit model of interleaved dc-dc converter

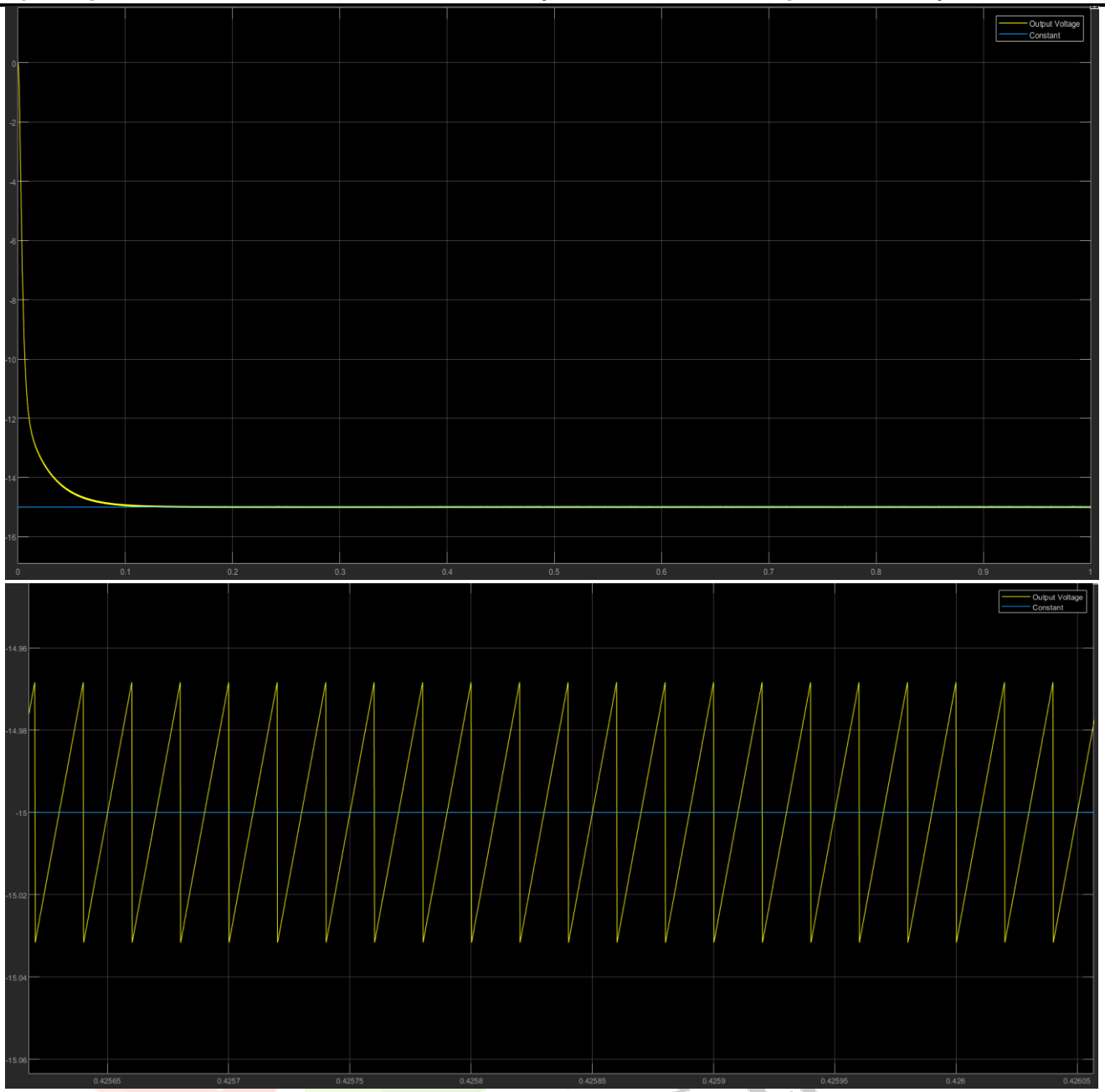

Fig. 9: Simulated output voltage waveforms of interleaved dc-dc converter

The following table summarizes the full analysis between the proposed interleaved dc-dc converter and also the traditional buck-boost converter according to performance metrics including the highest voltage overshoot, rising time, settling time, and steady-state error:

Table 3. Comparative analysis between BBC and IBBC

S.No.	Performance metrics	BBC	IBBC
1.	Maximum voltage overshoot (M_p)	0.87%	0.21%
2.	Rise time (t_r)	0.654 sec	0.116 sec
3.	Settling time (t_s)	1.150 sec	0.210 sec
4.	Steady-State error (e_{ss})	0	0

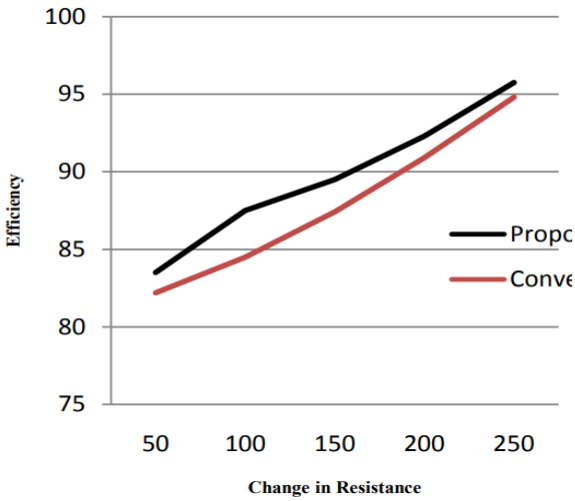

Fig. 10: Efficiency vs load resistance

As shown in Figure 7, the effectiveness of the traditional dc-dc Converter and the proposed interleaved dc-dc Converter has been assessed under various load resistance conditions [7]. It is clear that when compared to a regular dc-dc Converter, the Interleaved dc-dc Converter demonstrates much improved efficiency.

VII. CONCLUTION

This research offers a unique Interleaved Buck-Boost converter using a PID controller for increased voltage regulation. The research smoothly mixes mathematical calculations with MATLAB Simulink-based simulations to completely analyses the proposed technology. Through mathematical research, modelling studies, and realworld testing, the findings continuously indicate the controller's capacity to produce exact output voltage regulation, remarkable dynamic performance, and heightened overall efficiency. One of the important takeaways from this study is the considerable decrease in output voltage ripples provided by the interleaved Buck-Boost converter. This ripple reduction adds to a cleaner and more consistent power output, vital for applications sensitive to voltage variations. Additionally, the converter's structure utilizing twin switches significantly decreases switching losses. This benefit occurs from the alternation of switching between the two switches, resulting to greater overall energy efficiency. Moreover, a remarkable finding is the lack of input current ripple, showing the converter's efficiency and capacity to produce stable power. This paper underscores the potential benefits of adopting the interleaved Buck-Boost converter, offering not only enhanced efficiency and voltage regulation but also a substantial reduction in output voltage fluctuations, which is instrumental for applications demanding precise and stable power delivery.

VIII. ACKNOWLEDGEMENT

This is a great pleasure and immense satisfaction to express my deepest sense of gratitude and thanks to everyone who has directly or indirectly helped me in completing our paper work successfully. I express my gratitude towards guide Mrs. G. Nithya who guided and encouraged me in completing the work in scheduled time.

IX. REFERENCES

[1] M. R. Banaei and H. A. F. Bonab, "A High Efficiency Non isolated Buck–Boost Converter Based on ZETA Converter," in IEEE Transactions on Industrial Electronics, vol. 67, no. 3, pp. 1991-1998, March 2020, doi: 10.1109/TIE.2019.2902785.

[2] T. -R. Granados-Luna et al., "Two-Phase, Dual Interleaved Buck–Boost DC–DC Converter for Automotive Applications," in IEEE Transactions on Industry Applications, vol. 56, no. 1, pp. 390-402, Jan.-Feb. 2020, doi: 10.1109/TIA.2019.2942026.

[3] X. -F. Cheng, Y. Zhang and C. Yin, "A Zero Voltage Switching Topology for Non-Inverting Buck–Boost Converter," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 66, no. 9, pp. 1557-1561, Sept. 2019, doi: 10.1109/TCSII.2018.2887105.

[4] C. -m. Lee, Y. -l. Liu, H. -w. Shieh and C. -c. Tong, "LabVIEW Implementation of an Auto-tuning PID Regulator via Grey-predictor," 2006 IEEE Conference on Cybernetics and Intelligent Systems, Bangkok, Thailand, 2006, pp. 1-5, doi: 10.1109/ICCIS.2006.252318.

[5] S. Ding and F. Wang, "A New Negative Output Buck–Boost Converter with Wide Conversion Ratio," in IEEE Transactions on Industrial Electronics, vol. 64, no. 12, pp. 9322-9333, Dec. 2017, doi: 10.1109/TIE.2017.2711541.

[6] V. Paduvalli, R. J. Taylor and P. T. Balsara, "Analysis of Zeros in a Boost DC–DC Converter: State Diagram Approach," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 64, no. 5, pp. 550-554, May 2017, doi: 10.1109/TCSII.2016.2585642.

[7] S. Gangavarapu, A. K. Rathore and D. M. Fulwani, "Three-Phase Single-Stage-Isolated Cuk-Based PFC Converter," in IEEE Transactions on Power Electronics, vol. 34, no. 2, pp. 1798-1808, Feb. 2019, doi: 10.1109/TPEL.2018.2829080.

[8] Kasat, Ms. Kashmira Rathi and Dr. M. S. Ali. “Design and Simulation of PID Controller for Power Electronics Converter Circuits.” (2016).

[9] Lakshmi, D., Syed Zabiullah, M. Tech and Dr. Venu gopal. “Improved Step-down Conversion in Interleaved Buck Converter and Low Switching Losses.” (2014).

[10] M. Usman Iftikhar, P. Lefranc, D. Sadarnac and C. Karimi, "Theoretical and experimental investigation of averaged modeling of non-ideal PWM DC-DC converters operating in DCM," 2008 IEEE Power Electronics Specialists Conference, Rhodes, Greece, 2008, pp. 2257-2263, doi: 10.1109/PESC.2008.4592277.