DESIGN AND IMPLEMENTATION OF A LOW POWER HIGH PERFORMANCE TCAM USING LECTOR APPROACH

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Abstract: Memory is critical in current computing systems, and tackling its speed constraints is critical for basic system design. A content addressable memory (CAM) structure with simultaneous seek operations is widely utilized to boost memory and gain access to time. Ternary content TCAM is a specialized subsystem that uses content addressing in research tables to efficiently retrieve information from memory. The Lector approach, a low-energy way for designing AND gates and inverters within the CAM cellular. This structure, built in the CMOS era, achieves outstanding improvements in power consumption and delay parameters. The results for an 8x8 memory subsystem architecture demonstrate the efficiency of this strategy.

Index Terms - **TCAM, CAM, CMOS, Precharge elimination, Memory subsystem, Memory design, Lector approach, Low power techniques.**

I. INTRODUCTION

A CAM compares supplied hunt data to a table of stored data and delivers the address of the matching data. CAMs feature a single timepiece cycle outturn, which makes them faster than other tackle- and software-based hunt systems. CAMs can be employed in a wide range of operations involving high-hunting pets. At the moment, the primary marketable function of CAMs is to categories and advance Internet protocol (IP) packets in network routers. As AI approaches mortal-brain settings of speed and delicacy, systems rely less and less on centralised waiters to connect actions from the edge to the centre
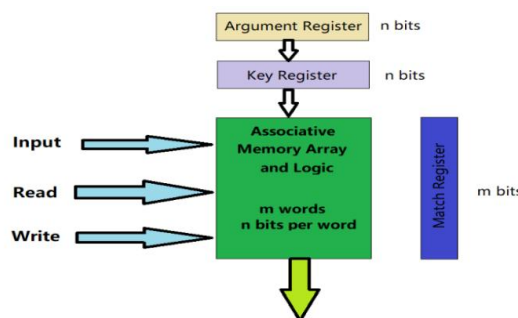
Fig 1 Block Content addressable memory

CAMs compare hunt data against a table of stored data and return the address of the matching data. A CAM hunt function operates important faster than its counterpart in software, and therefore CAMs are replacing software in hunt ferocious operations similar as address lookup in Internet routers, data contraction, and database acceleration. CAMs are considered a tackle perpetration of this construct. The direct hunt of a list is analogous to walking through all locales of a memory and comparing against a key in a periodical hunt.This is innately important briskly, although more complex to make.
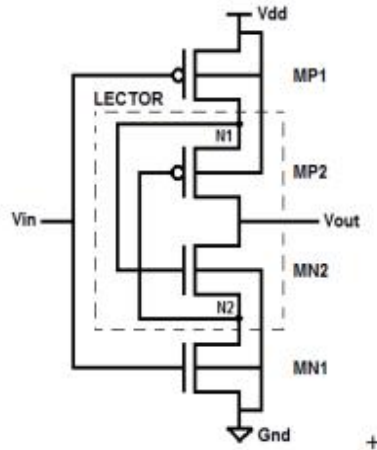

Fig 2 Inverter with Lector Technique

It has two LCTs, MP2 (PMOS) and MN2 (NMOS), which are connected between N1 and N2. The gate of MP2 is given to knot N2, which is the source of MN2, and the gate outstation of MN2 is given to knot N1, which is the source of MP2. PMOS transistors (MP1 and MP2) are connected to Vdd, and MN2 is connected to Gnd. When Vin = 0, N1 and P2 are likewise switched off, and when Vin = 1, N2 and P1 are turned off, leakage power is minimized.

II. LITERATURE REVIEW

Hongtao Zhong et al[1] "Dynamic Ternary Content-Addressable Memory Is Indeed Promising: Design and Benchmarking Using Nanoelectromechanical Relaysa" Ternary Content-Addressable Memory (TCAM) has held pivotal significance in cache systems, routers, and more, where achieving a balance between density, speed, power efficiency, and reliability remains crucial design goals. Traditional designs have led to low-write-power that are voluminous, as well as denser but potentially less reliable or higher-write-power TCAMs using nonvolatile memory (NVM) devices.

Rao .Met al[2] "Design and Implementation of a Low Power Ternary Content Addressable Memory (TCAM)Memory has evolved into a critical resource in today's computing systems. Memory speed remains a constraint in the overall design of various computer systems. Parallel search operations employing content addressable memory architecture are commonly used to improve memory access time. Ternary Content Addressable Memory (TCAM)subsystem offers search operation via content addressing in the defined look up table to fetch actual data from memory.

Vishakha H. Rane et al.[3] "Basic CMOS Gates using Lector Technique to Reduce Leakage Current in Tanner Tool" ,In this paper, we present the lector technique for reducing leakage current. In this research, we implement basic cmos gates and compare them to a novel proposed circuit using the lector approach, which inserts a p-type and an n-type leakage control transistor (LCT) between the transistor networks. The proposed approach has a lower leakage current than the simple circuit.

FishAetal.[4]"Leakagepowerattack-resilientsymmetrical8tsramcell",By enabling hidden data extraction utilizing side-channel leakage information, power analysis attacks have become a severe danger to security systems. Many of these systems rely on embedded memories, which are commonly implemented.

Conventional SRAM cells, are vulnerable to side-channel leakage power attacks. reduce the correlation between stored data and leakage currents. Both cells were built in a 65-nm CMOS technology to demonstrate the improved security memory array.

Avital M et al[5]. "Cmos based gates for blurring power information," Power analysis attacks have emerged as one of the most serious security vulnerabilities to current cryptographic digital systems. In this research, we describe a new CMOS-based blurring gate (BG) that improves a cryptographic system's resistance to these assaults. The BG alternates between static and dynamic operating modes at random.

Zackriya V M et al[6]. "Precharge-free, low-power content addressable memory," Systems, The hardware allowing concurrent lookup/search is called content-addressable memory (CAM). The parallel search system promises fast search operations at the expense of significant power consumption. Parallel NOR- and NAND-type matchline (ML) CAMs are appropriate for high-search-speed and low-power-consumption applications, respectively. Because the NOR-type ML CAM consumes a lot of power, numerous documented designs aim to reduce it.

III. PROPOSED METHODOLOGY

A. INVERTER GATE

The inverter gate is a key component in CMOS logic design. It functions as a NOT gate, switching '0's to '1's and vice versa. This is accomplished by the use of two crucial transistors: the NMOS, which connects the output to ground for a logical'0' input, and the PMOS, which connects the output to the supply voltage for a logical'1' input.

The result is where these paths intersect. The NMOS conducts for a '1' input, causing the output to be '0'. In contrast, a '0' input causes the PMOS to conduct, raising the output to a '1'. The interaction of NMOS and PMOS transistors provides power efficiency and noise resilience, making CMOS circuits trustworthy in terms of minimizing power consumption and resisting external disturbances.
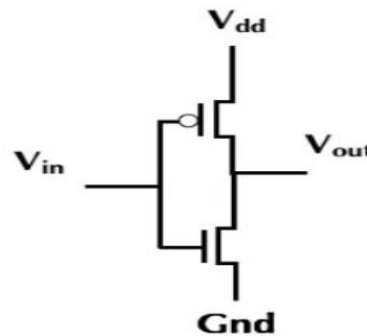

Fig 3 CMOS inverter structure

B. LECTOR INVERTER GATE

Fig 2 shows an LECTOR grounded CMOS inverter. It has two LCTs, MP2 (PMOS) and MN2 (NMOS), coupled between N1 and N2. The gate of MP2 is given to knot N2, which is the source of MN2, and the gate outstation of MN2 is given to N1, source of MP2. PMOS transistors (MP1 and MP2) is given to Vdd, and MN2 is given to Gnd. When Vin = 0, N1 and P2 are also turned off, and when Vin = 1, N2 and P1 are turned off, leakage power reduced.
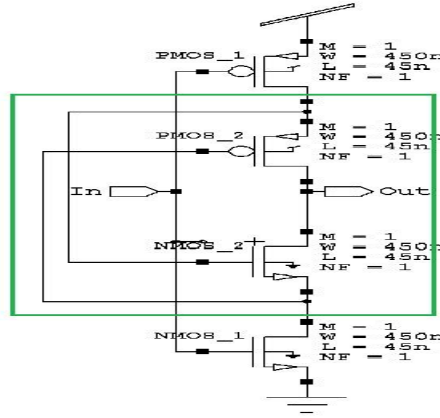
Fig 4 CMOS inverter structure with Lector Technique

We are implementing basic CMOS inverter gate and compare the simple circuit to the new proposed TCAM circuit with lector method, in which a p-type and an n-type leakage control transistor (LCT) are put between the pull-up and pull-down network. In comparison to the basic circuit, the proposed approach has a lower leakage current.

C. **AND GATE**

AND Gate is a logic gate in digital electronics that produces a TRUE output if and only if all of its inputs are FALSE. The AND gate is a key component in digital electronics, acting as a building block for different digital circuits and systems. The AND gate performs the logical AND operation with two binary inputs (0 or 1), generating a '1' output only when both inputs are '1'; otherwise, the output is '0'. Its truth table represents this behaviour, displaying all conceivable input combinations and their matching output values.
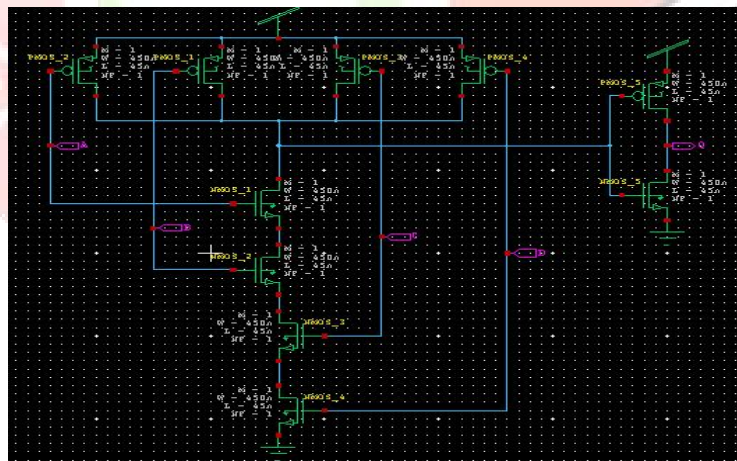

Fig 5 4-input AND gate Structure

D. **LECTOR AND GATE**

The AND gate's structure is based on CMOS technology and employs a lector method. The Lector approach is used in low power methodologies. We also used the Lector technique in inverter gate used in the CAM cell.There are numerous low-power techniques available, including power gating, clock gating, and transistor stacking. The leakage currents in the MOSFET transistor are mostly responsible for static power consumption. It is caused by undesirable current (sub-threshold current) flowing in the transistor's

channel even when the transistor is turned off. This has a substantial impact on the transistors' threshold voltages in the circuits devised a slew of power-gating strategies.
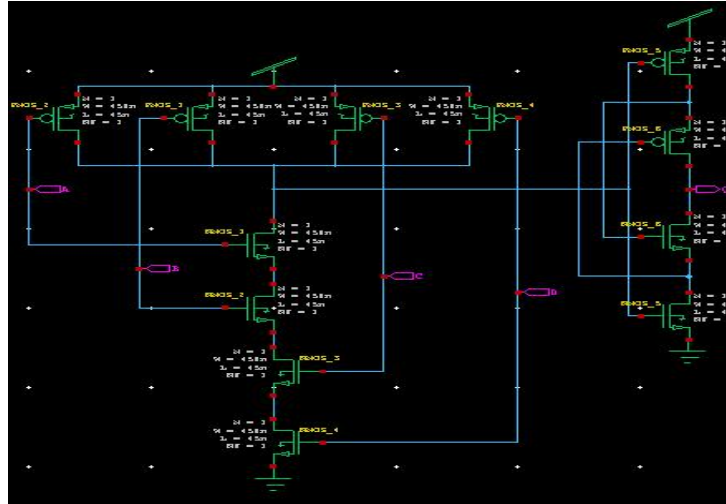

Fig 6 4-input AND gate Structure using Lector approach

E. PROPOSED Ternary CAM

In the Lector Ternary CAM, the main end is to achieve better power and detention results compared to the being TCAM structure. The insertion of LCT transistors by espousing the Lector approach. The Area will be more compared to the being system. Then, Area is defined as the count of transistors used in the design. TCAM has a wide range of operations. TCAM is generally set up in networking outfit, similar as high-performance routers and switches, to increase the speed of route look-up, packet bracket, packet forwarding, and access control list-grounded commands, it also has a wide range of operations in Artificial intelligence and the pall.
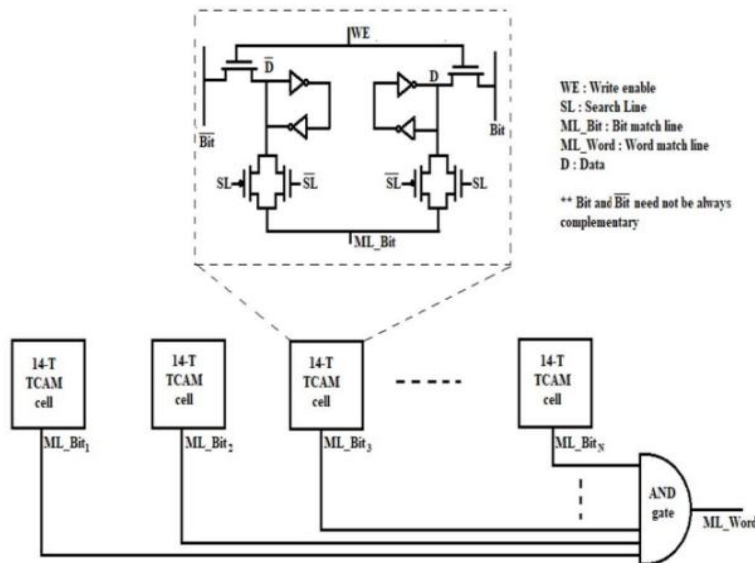

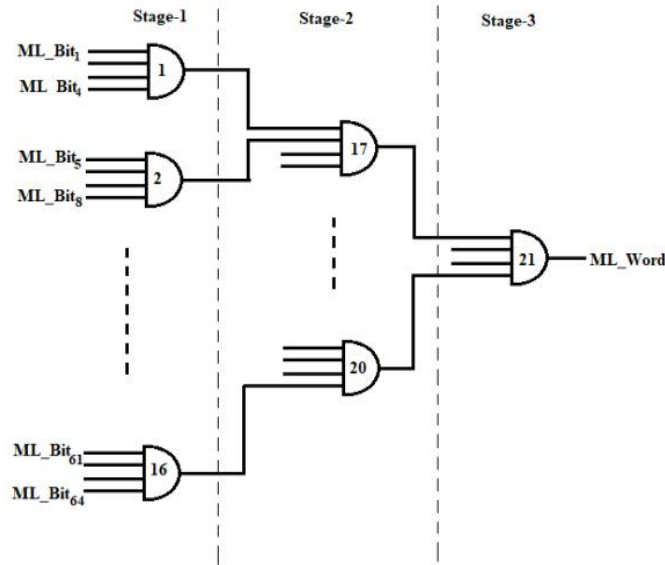**Fig 7** Proposed Ternary CAM

F. 64 bit AND Gate

Fig 8 64-input 'AND' Gate using 3-stage 4-input AND Gate

the transmission gate giving rail-to-rail voltage swing can be utilized instead of the pass transistors in the single CAM cell. Rather than establishing a series pass transistor circuit, the individual match lines are sent directly into a CMOS AND gate, the match line for a word bit is generated from all the match line bits.

The word match lines can be efficiently scaled up, as in Fig 3.6 , to create the match-line structure for a 64-bit word without significantly increasing the time because the AND gates in a particular stage running in parallel. In general, when the match lines are that is initialize charged up to v dd and to gnd during a search is made to a mismatch of stored data and search data, power consumption is a big problem.
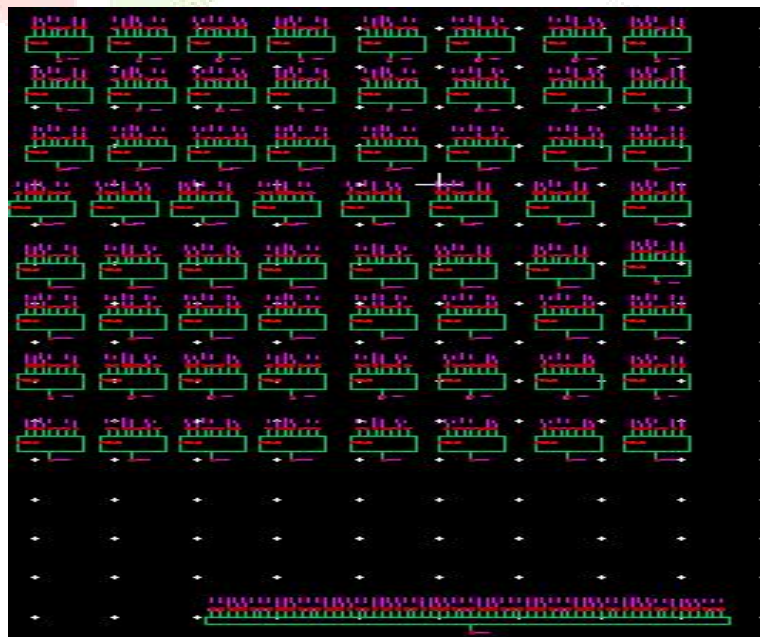
G. PROPOSED 8*8 TCAM

Fig 9 Proposed 8*8 TCAM

An 8x8 TCAM can be used in routers and switches to make real-time packet forwarding decisions based on matching predetermined rules or Access Control Lists (Ac Ls) in networking situations. The TCAM offers speedy and accurate matching by concurrently running parallel searches on all memory cells, making it suited for high-speed data processing environments. Despite their benefits in pattern matching efficiency, T Cams are more power-intensive and expensive than regular RAM, limiting their deployment to networking devices where their speed and hardware-based matching capabilities justify the extra costs.

IV. RESULTS AND DISCUSSION
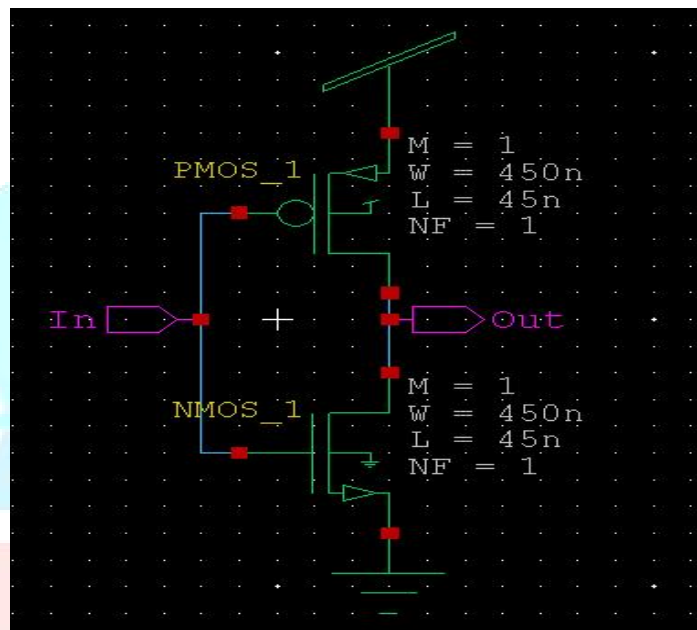
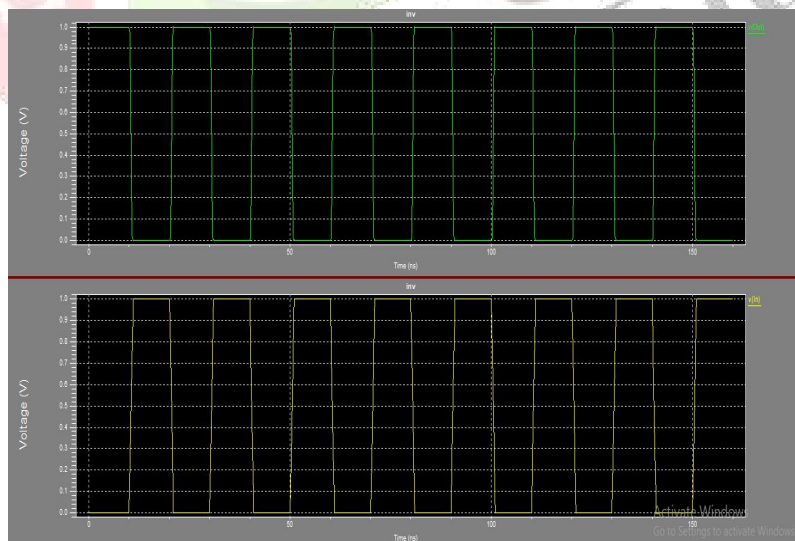**Fig 10** Schematic diagram of CMOS inverter

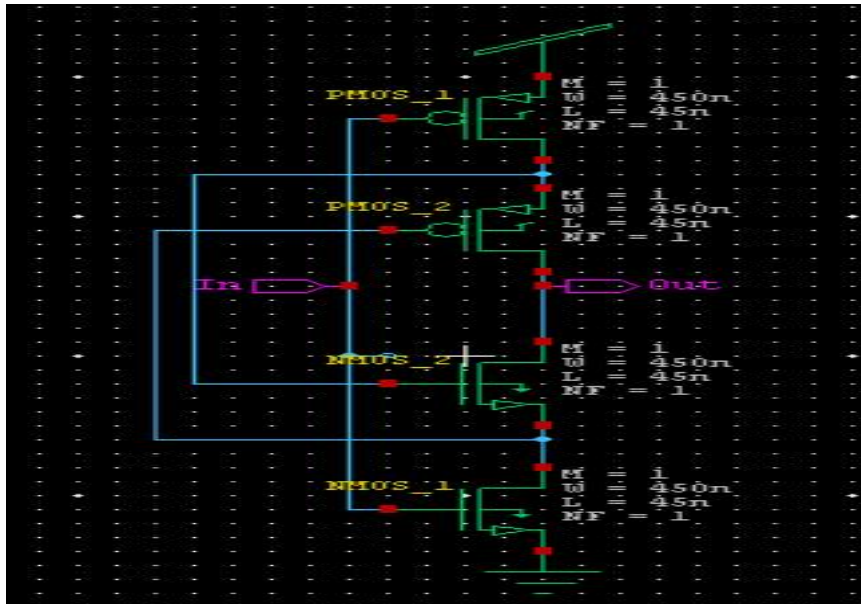**Fig 11** Waveform of CMOS inverter

Fig 12 Schematic diagram of CMOS inverter with Lector Technique
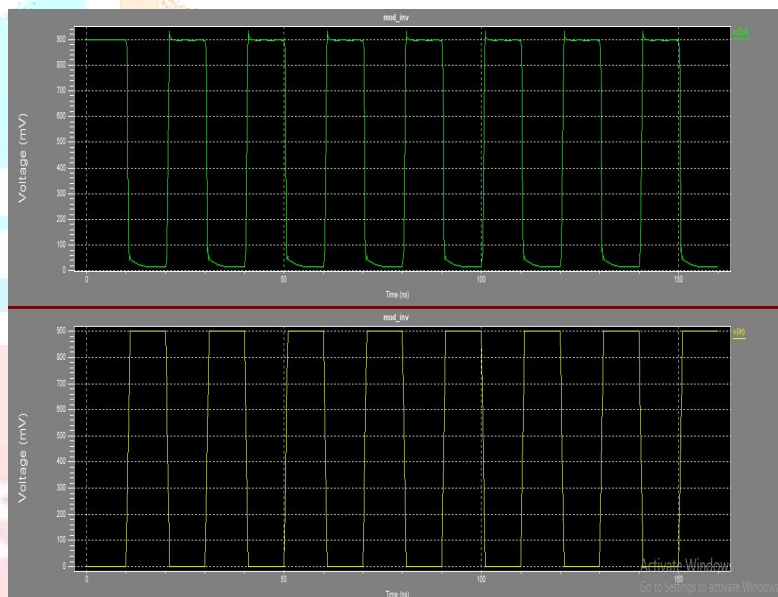

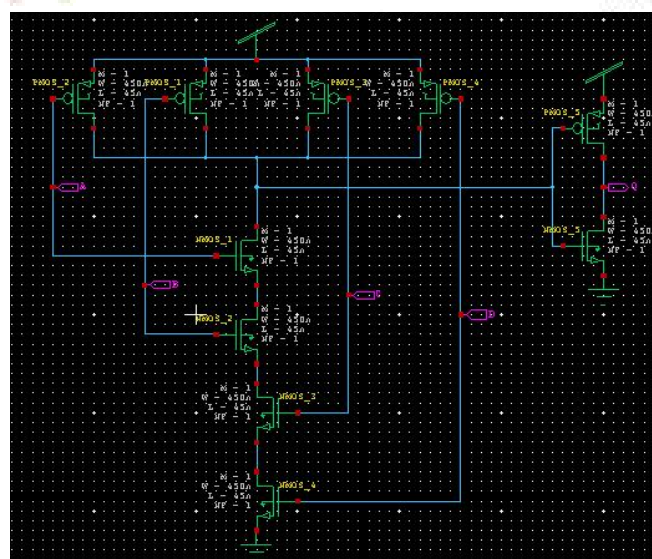**Fig 13** Waveform of CMOS inverter with Lector Technique

Fig 14 Schematic diagram of 4-input AND gate Structure
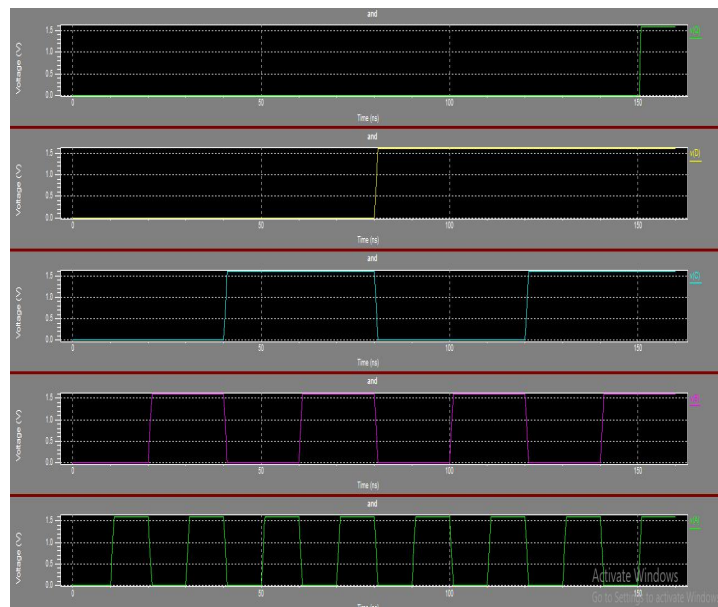
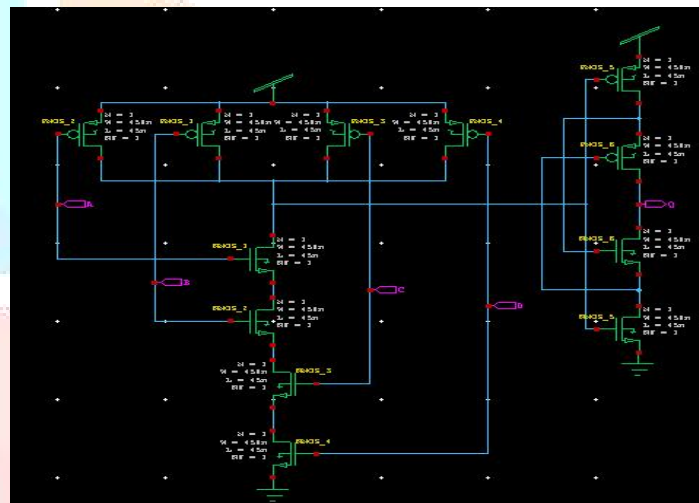**Fig 15** Waveform of 4-input AND gate Structure

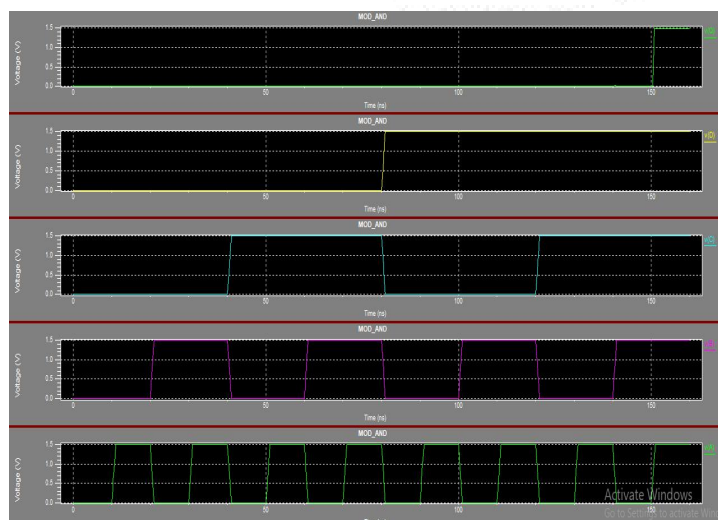**Fig 16** Schematic diagram of 4-input AND gate using Lector approach

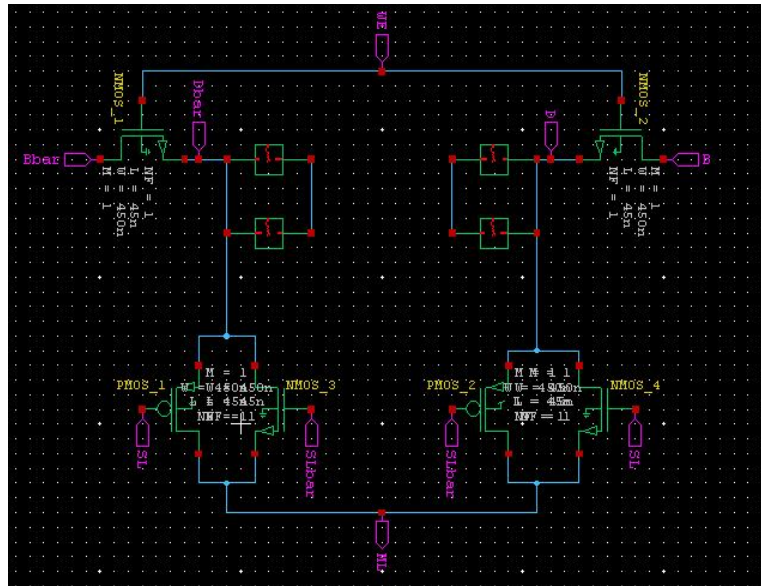**Fig 17** Waveform of 4-input AND gate using Lector approach

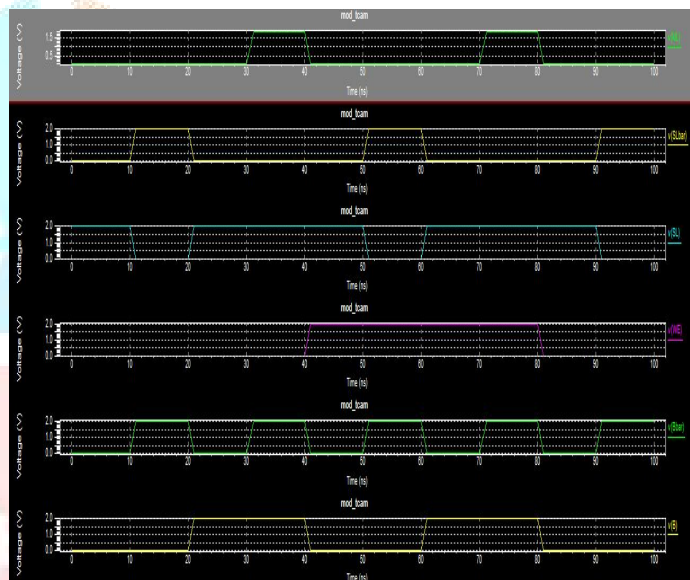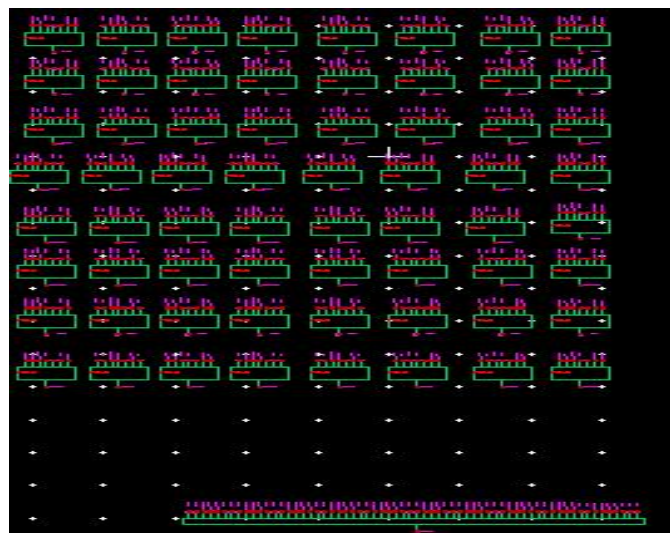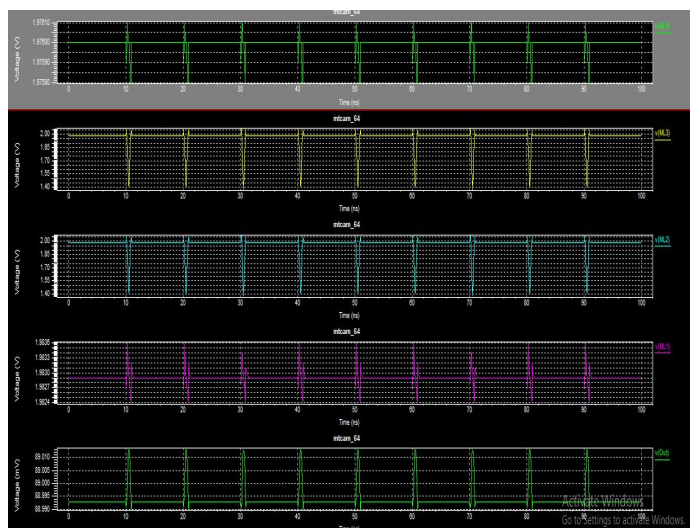**Fig 18** Schematic of Implemented Ternary

Fig 19 Waveform of Implemented Ternary

In Tanner EDA, an 8*8 TCAM is implemented, and power and delay values are calculated, as well as output waveforms, to illustrate the Match and Mismatch Condition condition.

Fig 20 Schematic diagram of 8*8 Implemented TCAM

Fig 21 Waveform of 8*8 TCAM

A planned 8*8 TCAM is constructed, and Table 1,2,3 compares metrics such as power, latency, and device and node counts. The presented analysis is responsible for the power consumption reduction. The proposed Ternary CAM is compared to the existing Ternary CAM with Inverter Gate & 'AND' Gate. The overall improvement in delay and power savings over other architectures.

Table 1: Comparison of Inverter Gate Architecture

Parameter	INVERTER GATE	LECTOR INVERTER GATE
Average Power consumed (W)	2.37 u	1.69 u
Delay (PS)	26.71	3.25

Table 2: Comparison of AND Gate Architecture

Parameter	AND GATE	LECTOR AND GATE
Average Power consumed (W)	61.31 u	17.53 u
Delay (us)	14.07	13.99

Table 3: Comparison of CAM Architecture

Parameter	Existing TCAM(8*8 CAM)	Proposed TCAM(8*8 CAM)	Existing Ternary	Proposed Ternary
Average Power consumed(W)	945.93 m	276.67 m	102.2 u	64.62 u
Delay(ps)	578.16	320.64	247.6	198
Device and node counts: MOSFET	1106	1660	14	22

IV. CONCLUSION

The suggested CAM and TCAM cells were deployed independently to create an 8*8 Ternary CAM memory subsystem. The provided analysis is recognized in reducing power consumption. The primary goal is to reduce power consumption by employing a lector approach in the designs of AND and Inverter gates in the TCAM schematic. The proposed architecture reduces the leakage power as well as delay parameters compared to existing structure of Inverter Gate, AND Gate & TCAM. When compared to the existing TCAM structure, the proposed architecture minimizes power dissipation as well as delay characteristics. Tanner EDA is used to simulate the complete design, which uses 45nm technology.TCAM has a diverse set of operations. TCAM is commonly used in networking equipment, such as high-performance routers and switches, to boost the speed of route look-up, packet bracketing, packet forwarding, and access control list-grounded commands. It also has a wide variety of operations in artificial intelligence and pall. Different CAM cells can be added, and power and detention can be achieved with low-power methods. For transistor count enhancement, a technique known as gate incorporating can be used.

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