



An Evaluation Of Model-Free Time-Delay Compensation Methods

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ABSTRACT :

Recent advancements in digital signal processing technology have facilitated the utilization of digital microprocessors for the regulation of grid-connected inverters. Nonetheless, the digital manifestation is hindered by phase lag resulting from temporal delays. This phase lag evaluates the stability and resilience of the inverter controller. This study offers a comprehensive assessment of time-delay compensation methodologies for both model-free and model-based inverter controllers in the context of grid connections. MF methodologies predominantly employ proportional-integral and proportional resonance controllers, alongside various strategies aimed at mitigating time delay. In the interim, this study delineates the control strategies most frequently employed by MB, encompassing the Smith predictor and the modified Smith predictor. A comprehensive summary of various analogous strategies from the literature aimed at minimizing delays is presented, alongside a thorough examination of the notable issues related to the MF and MB procedures. Ultimately, this study presents a hypothesis regarding the most favorable approach at present and suggests a hybrid technique that integrates the MF and MB procedures, thereby offering readers a direction for future inquiry.

Keywords: Digital Microprocessor, Inverter Controller, Compensation Method, Digital Signal Processing.

1. INTRODUCTION

Recently, conventional power systems are undergoing a transformative change in their operational paradigms due to the increasing global demand for energy. Consequently, in light of the growing global demand, it is imperative that networks undergo liberalization to accommodate emerging energy sources, including solar and wind. The utilization of these renewable energy resources holds the promise of making a significant contribution to the main grid, provided they are fully harnessed and effectively managed within a regulated environment. Distributed generation (DG) is increasingly recognized as a viable solution to meet this demand, wherein DG systems are methodically interconnected through power electronic devices known as grid-connected inverters, thereby forming what is referred to as the

microgrid. The concept of integrating individual distributed generation is aimed at achieving system flexibility, thereby enhancing system optimization, reliability, protection, integrity, security, and power quality control. Recent regulations concerning safe operation, power quality, and islanding protection are delineated in [2], as the interacting devices encounter specific challenges with the grid, especially in instances of grid inadequacy [1]. Consequently, the challenges associated with interconnections have recently attracted considerable scrutiny, leading to an increase in research efforts. This surge is largely attributable to the implementation of real-time-based controllers capable of executing intricate and advanced control algorithms, alongside the emergence of power electronic devices designed to manage high power levels and facilitate rapid switching [3]. Utilizing real-time-based controllers presents various drawbacks, such as a latency in the control loop and a lag during the transition between islanded and grid-connected modes. The capacity of a physical system to react to an exerted force with a temporal lag is referred to as time-delay [4]. Whenever energy or a control signal is transmitted from one point to another, a propagation delay is invariably present along the channel. The velocity of the transmitted signal and the nature of the medium through which it traverses are intrinsically linked to the extent of the propagation delay. Consequently, an extended latency in the digital control loop of the inverter, or during the transition between grid-connected and islanded modes, complicates the design and implementation of the controller, while also intensifying frequency and voltage anomalies. Conversely, a minor postponement can be effectively navigated through an array of adaptive methodologies. A voltage, current, or direct power controller, or a combination of these controllers arranged in a cascaded loop with either an inner-loop or outer-loop topology, can be employed in grid-connected inverters that utilize LCL filters. A multitude of studies employ inner current control to achieve accurate current tracking, adequate control bandwidth, and rapid transient response. Conversely, the existing controller is employed in voltage source inverters (VSI) to facilitate the inverter's operation as a current amplifier within the bandwidth of the current loop [5]. Conversely, within the outer-loop framework, the voltage controller functions to mitigate disturbances originating from the grid and input sources, thereby ensuring the stability of power flow within the system. Nonetheless, the presence of time-delay within the control loop, especially in digital implementations, constrains the control bandwidth of the current controller.

Furthermore, due to the progress in digital signal processing technology, digital microprocessors are employed to manage grid-connected inverters [6]. The digital realization offers numerous advantages, including enhanced reliability, greater flexibility in control, and rapid reprogrammability, when compared to analog control systems. This digital implementation presents several challenges, the most notable being the phase lag introduced by the time delay within the control loop.

The incorporation of supplementary control loops will further exacerbate this delay. Grasping the fundamental causes of time-delay in the control loop of a grid-connected inverter is crucial prior to exploring various commonly employed strategies for compensating such delays. The primary causes of time delays in the implementation of digital controllers include the zero-order hold effect of digital pulse-width modulation [8], the calculation time of the controller [7], and the sampling and updating of voltage and current values for control purposes [9]. Consequently, achieving optimal performance appears to be rather difficult when the control loop experiences a significant time delay. Consequently, the controller

exhibits a diminished control bandwidth, an increased overshoot due to an insufficient phase margin, and a reduced transient response characterized by a low-gain cross-over frequency.

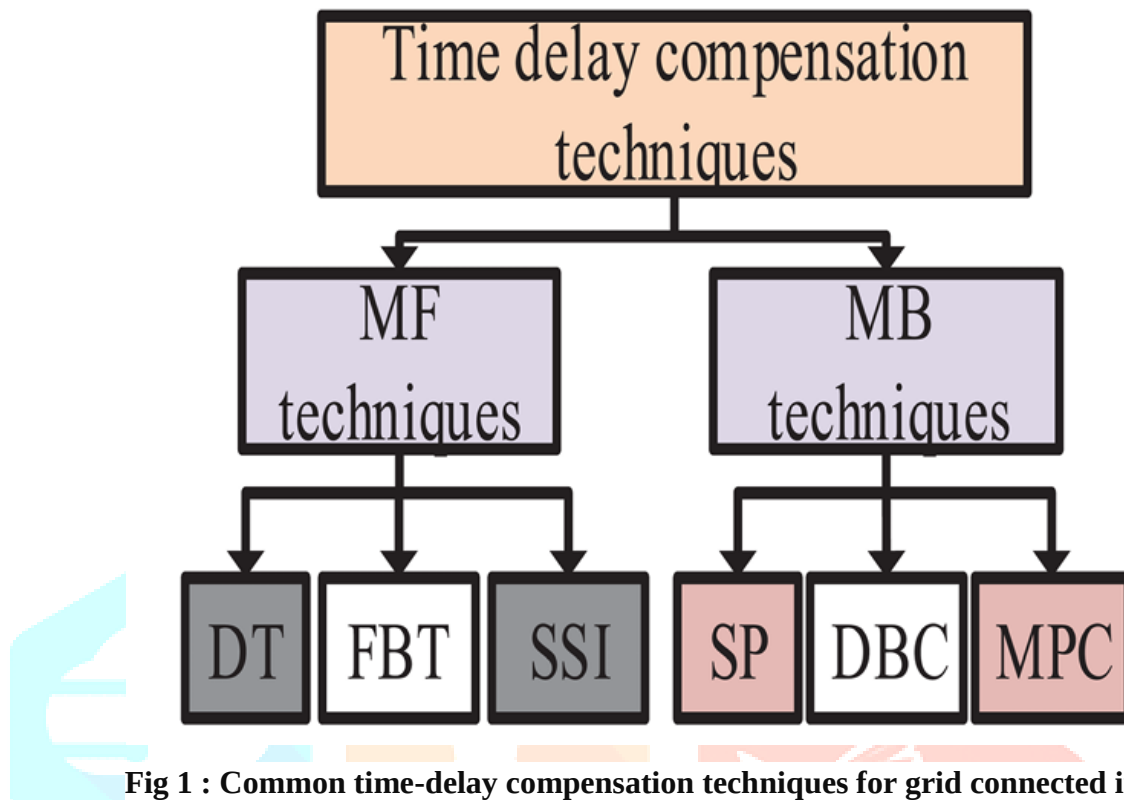


Fig 1 : Common time-delay compensation techniques for grid connected inverter

Furthermore, this will exacerbate the controller's performance and result in instability, among other concerns. As a result, compensators are employed to mitigate or entirely eliminate delays to effectively respond to these effects. Figure 1 illustrates the diverse array of time-delay compensation strategies that have been presented in the literature, which can be classified into two main categories: model-based (MB) and model-free (MF) strategies [6]. MF approaches, while exhibiting lower accuracy, remain impervious to the model's quality. In contrast, MB techniques demonstrate greater accuracy, yet they are susceptible to the precision of system modeling. The Smith predictor, modified Smith predictor, deadbeat controller, model predictive controller, and various others exemplify techniques for compensating time delays in model-based systems. On the other hand, the methodologies pertaining to MF encompassed the filter-based technique (FBT), the alteration of the sampling instant (SSI) of the control variable, and the damping technique (DT) [6]. The objective of this paper is to highlight contemporary challenges and strategies aimed at mitigating the effects of time delay within the control loop of grid-connected inverters. It further indicates a direction for subsequent investigation into the minimization of time delays.

2. MODEL-FREETIME-DELAY

The LCL filter, with its ability to mitigate high-frequency switching harmonics at the inverter's output, has increasingly supplanted the conventional L-type filter in grid-connected inverter applications. This arises from the inherent capabilities of the LCL filter. Conversely, this advantage is accompanied by a significant drawback: its implementation may induce system instability due to the zero impedance observed at the resonance frequency [10]. Should the time-delay effect be factored into the control loop of

the inverter, this vulnerability will be significantly exacerbated. Consequently, considerable effort has been expended by various researchers to concurrently tackle the oscillation challenge associated with the LCL filter while also reducing the time delay within the control loop. The forthcoming subsections will elucidate the most frequently employed MF strategies for time-delay compensation.

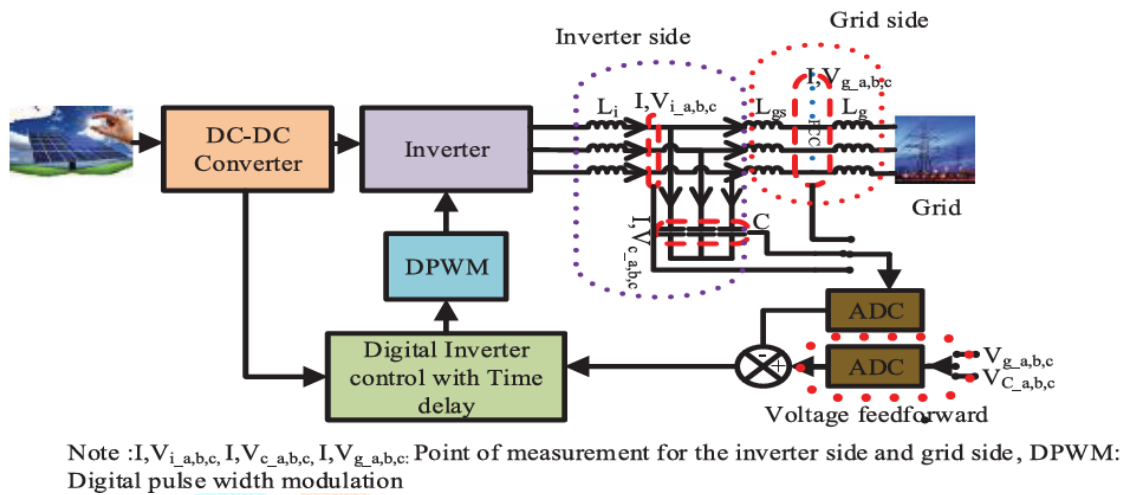


Fig 2 : Schematic diagram of a grid-connected inverter

3. TECHNIQUES

3.1 Damping techniques

The oscillation problem of the LCL filter and the time delay in the control loop are addressed through damping techniques, categorized into passive and active damping strategies. Incorporating a resistor in series with the filter inductor or capacitor facilitates passive damping, effectively mitigating the resonant peak and enhancing system stability. This approach is straightforward and offers a fair cost. Nonetheless, the introduction of the additional resistor results in power loss, diminished filter efficacy, and a reduction in overall system performance [11]. As a result, these drawbacks diminish the viability of this damping strategy, especially within an inadequately structured distribution grid. The active damping methodology presents a viable alternative to passive damping, wherein oscillations are mitigated and time delays are addressed through the utilization of observed state variables instead of relying on a resistor. This approach is further divided into two distinct categories: grid-side active damping and inverter-side active damping. As indicated in references [12–15], the active damping methodology on the inverter side employs feed-forward current or voltage state variables, as well as single, double, or multi-loop feedback mechanisms, to enhance damping performance and minimize time-delay within the control loop. Figure 2 illustrates that measurements of state variables are conducted on the filter capacitor or inductor located at the inverter side. The grid-side active damping technique employs a single, double, or multi-loop feedback or feed-forward mechanism for grid current or voltage, as illustrated in Figure 2, to effectively dampen system oscillations and alleviate time-delay issues. Nevertheless, despite the favorable outcomes associated with this technique, the single-loop approach does not ensure stability when disturbances occur. Concurrently, the necessity to monitor multiple state variables in double- and multi-loop configurations introduces cost implications, diminishes reliability, and tends to elevate the complexity of the control system [10, 11].

Reports indicate that the grid-side active damping approach renders the system inherently unstable [16]. Consequently, a temporal delay is incorporated into the control loop to achieve stability. The authors employed this technique in [10], asserting that the incorporation of time-delay enhances the stability of the system in a notably effective way. The system exhibits instability when the time-delay deviates from the designated range; however, the stability outlined in [10] holds true solely within a specific time-delay interval. Grid-connected inverters requiring a rapid controller with minimal latency are unable to adopt this method.

3.2 Filter-based techniques

In this approach to compensation, the observed state variables are transmitted to the controller through the utilization of a filter. Alternatively, one might position a filter within the cascade alongside the primary controller, or it could be connected to refine the voltage reference directed towards the modulator. The filter effectively compensates for the phase lag introduced by the time delay across various modes, a methodology employed in references [14, 17–20]. This approach was selected due to its independence from supplementary sensors. Nevertheless, this approach is not without its drawbacks. It tends to amplify noise, presents challenges in tuning the filter parameters, exhibits sensitivity to fluctuations in those parameters, and is particularly responsive to variations in grid impedance.

3.3 Control variable sampling instant shift or PWM updating instant approaches

In the application of pulse width modulation (PWM), it is customary to sample the state variables at the midpoint of each turn-on or turn-off cycle. In this manner, the mean values of variables such as inductor current, capacitor current, or grid current are sampled, as illustrated in Figure 3(a). Here, ms represents the single-update PWM wave, while $ms(K-1)$ denotes the single-update PWM wave of the $(K-1)$ th carrier cycle, which is positioned at the apex of the $(K-1)$ th triangular carrier. The duty cycle is articulated as $M(K) = ms(K-1)$, where $ms(K-1)$ is derived from the duty cycle calculated by sampling values at the peak of the $(K-1)$ th triangular carrier [20]. The three sample points encompassed within a singular update are as follows: $ms(K)$, $ms(K-1)$, and $ms(K-2)$. This observation is illustrated in Figure 3(a). Conversely, there exist five sample points, represented as $ms(K)$ to $ms(K-5)$, which are observable in the context of double-updating, as illustrated in Figure 3(b). Moreover, as illustrated in Figure 3(c), there exist nine sample points in the multi-updating process, spanning from milliseconds (K) to milliseconds $(K-9)$. Nonetheless, the practice of single sampling and updating frequently leads to a lag of one switching period, thereby constraining the bandwidth accessible to the controller at that particular moment.

The delay associated with this one-switching period can be minimized to half of the switching period through the implementation of the double-update mode, as illustrated in Figure 3(b). In this configuration, the control variables are sampled on two occasions, with the update executed at both the apex and trough of the triangular carrier, occurring twice during the midpoint of the turn-on and turn-off intervals of the pulse width. An alternative approach involves employing the double-update mode. Furthermore, several researchers have proposed that adjusting the timing of control variable sampling to align more closely with the duty cycle update moments could enhance the reduction of time delay; this approach has been applied in [21–23]. When implementing this method, it is important to acknowledge that the asynchronous sampling procedure may inadvertently introduce undesirable harmonics [6].

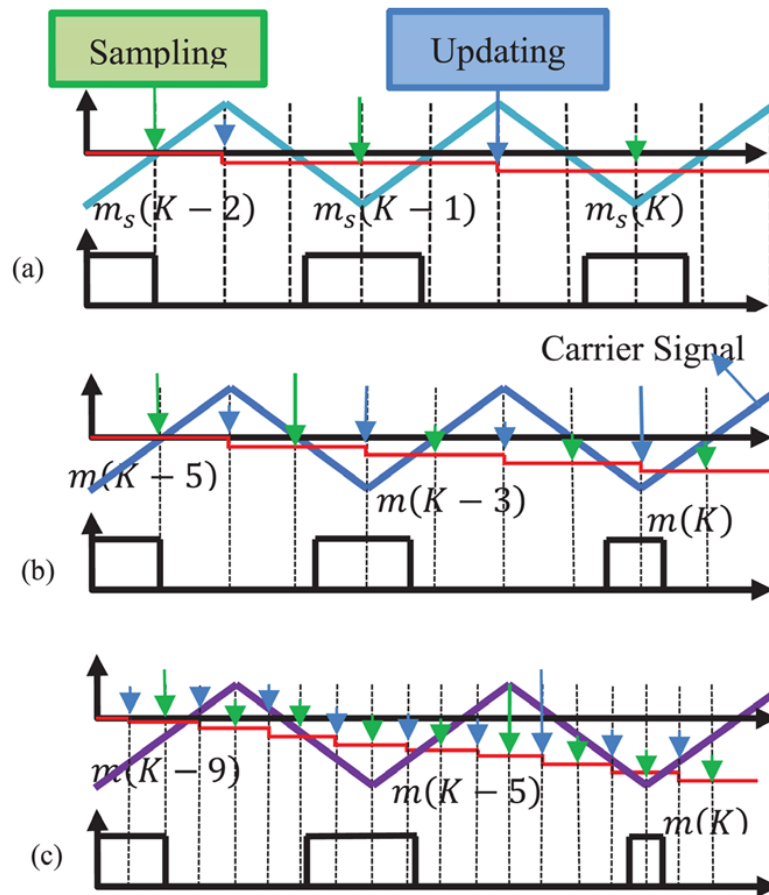


Fig 3 : (a)Single updating, (b)double updating and (c) multi-updating

Nevertheless, although the authors in [21] employed the approach of sampling the control variables at the duty cycle updating moments, they posited that the traditional sampling at the midpoint of the turn-on and turn-off periods of the PWM is more effective in diminishing harmonic disturbances compared to the adjustment towards the duty cycle updating moments. This was the inference they reached. The sampling of state control variables and the frequent updating of the duty cycle within a single switching period represents an additional approach that can be employed to minimize wasted time effectively. This observation is illustrated in Figure 3(c). This methodology is recognized as the multi-sampling, multi-updating approach. This methodology is particularly well-suited for deployment on a field-programmable gate array (FPGA), as indicated in the referenced material.

4. CONCLUSIONS

This study aims to deliver a comprehensive overview of the analytical insights contributed by previous research regarding time-delay compensation strategies within the control loop of grid-connected inverters. MF has emerged as a more widely embraced approach in this domain of inquiry, attributed to its straightforwardness and moderate efficacy, notwithstanding the complexities associated with the stability of the system in both inverter-side and grid-side configurations. This analysis is categorized according to the reliance of the controller on the system's model (MF and MB). In this discourse, I shall elucidate the distinctions between the two models. The reliability of these types of controllers cannot be assured when faced with disturbances or when the system is connected to a weak grid. Although various methods have been proposed to address time-delay and enhance system stability while minimizing sensor usage and

complexity, the reliability of these controllers remains uncertain. Upon examination of the model-based strategies, it became evident that the Smith predictor and its modified variant were the initial approaches utilized to mitigate the effects of time delays in conjunction with traditional PID controllers. This was uncovered as a result of the application of the Smith predictor as the initial method employed. This approach holds diminished significance for grid-connected inverters, primarily owing to the constraints of these controllers, which encompass their incapacity to manage time-varying signals and a limited capacity for disturbance rejection. DBC has recently garnered attention owing to its ability to facilitate rapid current monitoring, eliminate steady-state error, compensate for time delays, and reject disturbances. This methodology is categorized into two distinct groups, based on the insights presented in this article, contingent upon the inclusion or exclusion of time delay effects during the controller design phase. The analysis of research studies examining the effects of time delay revealed that a considerable portion of these works operated under the assumption that both the DC-link voltage and the grid voltage were held constant. Moreover, the outer loop was excluded from the controller design.

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