



LOW POWER 3-2 AND 4-2 ADDER COMPRESSORS IMPLEMENTED USING ASTRAN

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ABSTRACT

This project introduces a set of graph-based algorithms for efficiently 3-2 and 4-2 Adder VLSI circuits using simple cells. The proposed algorithms are concerned to, first, effectively minimize the number of logic elements implementing the synthesized circuit. Then, we focus a significant effort on minimizing the number of inverters in between these logic elements. Finally, this logic representation is mapped into a circuit comprised of only two-input NANDs and NORs, along with the inverters. Two-input XORs and XNORs can also be optionally considered. As we also consider sequential circuits in this work, flip-flops are taken into account as well. Additionally, with high-effort optimization on the number of logic elements, the generated circuits may contain some cells with unfeasible fanout for current technology nodes. In order to fix these occurrences, we propose an area-oriented, level-aware algorithm for fanout limitation. The proposed algorithms were applied over a set of benchmark circuits and the obtained results have shown the usefulness of the method. We show that efficient implementations in terms of inverter count, transistor count, area, power and delay can be generated from circuits with a reduced number of both simple cells and inverters, combined with XOR/XNOR-based optimizations. The proposed buffering algorithm can handle all unfeasible fanout occurrences, while (i) optimizing the number of added inverters; and (ii) assigning cells to the inverter tree based on their level criticality. When comparing with academic and commercial approaches, we are able to simultaneously reduce the average number of inverters, transistors, area, power dissipation and delay up to 48%, 5%, 5%, 5%, and 53%, respectively. As the adoption of a limited set of simple standard cells have been showing benefits for a variety of modern VLSI circuits constraints, such as layout regularity, routability constraints, and/or ultra low power constraints, the proposed methods can be of special interest for these applications. Additionally, some More-than-Moore applications, such as printed electronics designs, can also take benefit from the proposed approach.

Keywords: Graph-based algorithms. logic synthesis. technology 3-2 and 4-2 Adder. standard cell library. simple cells.

1. INTRODUCTION

Nowadays, low power-consumption, high-speed circuits, and area are the design trade-offs in VLSI industries. The evolution of portable electronics, computing devices is the importance of low-power circuit design methodologies. Low-power-dissipation, least delay, and area are to be needs one of them important design factors for VLSI designers. To increase the performance in VLSI circuits, there is required to be less the power saving and the area. Behind these designs, driving forces have the essential portable device different applications for less power-dissipation, minimum delay and higher throughput. An addition is an arithmetic operation, extensively used in several low-power VLSI circuits, like as specific application DSP architectures and microprocessors. These modules are used for many arithmetic operations, like as addition, subtraction [1]. Thus, these facts of view, the design of a 3-2 and 4-2 Adder circuit are having low- power-dissipations, lower the delay, and high speed performance [1-15]. Many researchers are emphasizing on circuit performance through the minimum level of transistor count. XOR-XNOR circuit are the basic structures block of F-A. The increasing the performance of an XNOR-XOR circuit can be significantly increases the better perform of the F-A design. Static RAM memories (XNOR-XORs) are hardware search engines that are much faster than algorithmic approaches for search-intensive applications. XNOR-XORs are composed of conventional semiconductor memory (usually XNOR-XOR) with added comparison circuitry that enables a search operation to complete in a single clock cycle. The two most common search- intensive tasks that use XNOR-XORs are packet forwarding and packet classification in Internet routers. I introduce XNOR-XOR architecture and circuits by first describing the application of lookup in Internet routers. Then we describe how to implement this lookup function with XNOR- XOR.

2. LITERATURE SURVEY

STATIC RAM MEMORY (XNOR-XOR) CIRCUITS AND ARCHITECTURES: A TUTORIAL AND SURVEY

In this system to design XNOR-XOR circuits and architectures, with an emphasis on high-capacity XNOR-XOR. First, to motivated discussion by showing how XNOR-XORs can be applied to packet forwarding in network routers. At the circuit level, reviewed the two basic CMOS cells, namely the NOR cell and the NAND cell. Also shown how the cells are combined in a match line structure to form a XNOR-XOR word. explored the conventional recharge-high scheme for sensing the match line, as well as several variations that save match line power including low- swing sensing, the current-race scheme, selective precharge, pipelining, and current saving scheme. We have also reviewed the conventional approach for driving search lines, and the power- saving approaches which eliminate the search line precharge or employ hierarchical search lines. At the architectural level, we have reviewed three architectures for reducing XNOR-XOR power, namely bank-selection, pre-computation, and dense encoding. Finally, have presented our views of future development in the XNOR-XOR field.

A MISMATCH-DEPENDENT POWER ALLOCATION TECHNIQUE FOR MATCH-LINE SENSING IN STATIC RAM MEMORIES

To use this architecture, the ML sensing circuits need to distinguish MLs with high impedance from MLs with low impedance. Conventionally, this ML sensing has been performed by recharging all MLs to and then applying the search data on the SLs. Matches (MLs with high impedance) remain at while mismatches (MLs with low impedance) discharge to GND. This sensing method achieves a higher search speed than the NAND sensing method, but at the price of higher power consumption, since all MLs are charged to and then discharged to GND in every cycle (except for the few MLs that are matched). In addition, the SL pairs contribute to the dynamic power consumption as one of the two SLs in a pair is always cycled between GND and. To reduce power while maintaining speed, several sensing techniques have been developed around the NOR ML architecture. One technique is to limit the voltage swing on the MLs to a value less than, hence, reducing the ML portion of the dynamic power consumption. Another technique is to minimize the switching activity of the SLs, hence reducing him SL portion of the dynamic power consumption. In our previous work, proposed a sensing scheme that limits the voltage swing on the MLs to. Also, by pre-charging the MLs to GND (instead of to), we eliminated the need for SL reset, hence, reducing the SL power consumption. In this work, we propose a new sensing scheme that distributes power no uniformly to MLs, with MLs containing larger number of mismatched bits consuming less power. The overall effect of this technique is a 60% power reduction did not compare to the conventional NOR architecture and 40% compared to our previous work.

A LOW-POWER STATIC RAM MEMORY (XNOR-XOR) USING PIPELINED HIERARCHICAL SEARCH SCHEME

Proposed XNOR-XOR architecture with pipelined match-lines and hierarchical search-lines. The match-lines are divided into two pipeline segments, each segment with its own MLSA to decide if there is a match and its own pipeline flip-flop to store the outcome of the match operation for the segment. Segmenting the match-lines saves power because most words will miss in the first segment, eliminating the need to activate the subsequent segments. To save search-line power, one would ideally use low-swing signaling on the SLs. For example, one could limit the SL swing to output voltage, where v_{th} is the threshold voltage of an NMOS transistor and is a small incremental voltage above the threshold. This would reduce the SL energy consumption to from the original when is applied to SL. The price of this reduction in power is a major reduction in match-line speed, caused by a lower gate over-drive voltage on the compare transistors. To mitigate this problem, propose the two-level search-line hierarchy. The global search-lines (GSLs) drive the full height of the XNOR-XOR and feed into the local search-lines (LSLs) which drive only a subset of XNOR-XOR cells. Low-swing signals drive the GSLs and local low-swing receivers amplify the GSL signal to the corresponding LSL. However, only LSL receivers feeding an active ML segment are enabled. LSLs feeding an inactive ML segment are disabled. In a large XNOR-XOR block, many match-line segments are inactive leading to savings in search-line power.

LEAKAGE CURRENT MECHANISMS AND LEAKAGE REDUCTION TECHNIQUES IN DEEP-SUB MICROMETER CMOS CIRCUITS

To achieve higher density and performance and lower power consumption, CMOS devices have been scaled for more than 30 years. Transistor delay times decrease by more than 30% per technology generation, resulting in doubling of microprocessor performance every two years. Supply voltage has been scaled down in order to keep the power consumption under control. Hence, the transistor threshold voltage has to be commensurately scaled to maintain a high drive current and achieve performance improvement. With the continuous scaling of CMOS devices, leakage current is becoming a major contributor to the total power consumption. In current deep- sub micrometer devices with low threshold voltages, sub threshold and gate leakage have become dominant sources of leakage and are expected to increase with the technology scaling. GIDL and BTBT may also become a concern in advanced CMOS devices. To manage the increasing leakage in deep-sub micrometer CMOS circuits, solutions for leakage reduction have to be sought both at the process technology and circuit levels. At the process technology level, well-engineering techniques by retrograde and halo doping are used to reduce leakage and improve short-channel characteristics. At the circuit level, transistor stacking, multiple, dynamic, multiple, and dynamic techniques can effectively reduce the leakage current in high-performance logic and memory designs.

A CROSS-LAYER FRAMEWORK FOR DESIGNING AND OPTIMIZING DEEPLY-SCALED REDUCED T-BASED CACHE MEMORIES

Seven reduced T devices optimized for a 7-nm process technology along with three XNOR-XOR cells were evaluated and compared using our cross-layer design framework. The high_1 device has the lowest OFF current and the highest ON/OFF current ratio. Moreover, the 8T XNOR-XOR cell achieves the highest noise margins, which guarantees its robust operation. At the cache level, it is observed that L1 cache memory made of high_1 devices operating at the near-threshold regime achieves the minimum energy operation point, whereas cache memories made of high (high-top) devices for the 8T (6T-1) XNOR-XOR cell operating at the super-threshold regime achieve the minimum energy-delay product point. The 8T XNOR-XOR cell has an excellent read SNM, and thus, the 8T XNOR-XOR is the preferred choice of memory cell due to reliability considerations. On the other hand, because of smaller layout area, the all single-fin 6T XNOR-XOR cell achieves higher memory density and lower access latency and energy consumption. As a result, the efficient usage of (i) read/write-assist circuits and/or (ii) the independent gate control feature of reduced T devices (if such devices are provided by the underlying technology process) is significantly important in order to enhance the robust operation of the 6T-1 XNOR-XOR cell and, hence, to increase the energy efficiency of cache memories.

3. EXISTING SYSTEM

3.1. CORE CELLS AND MATCHLINE STRUCTURE

A XNOR-XOR cell serves two basic functions: bit storage (as in RAM) and bit comparison (unique to XNOR-XOR). Fig. 5 shows a NOR-type XNOR-XOR cell [Fig. 5(a)] and the NAND-type XNOR-XOR cell [Fig. 5(b)]. The bit storage in both cases is an XNOR-XOR cell where cross-coupled inverters implement the bit-storage nodes D and. To simplify the schematic, we omit the nMOS access transistors and bitlines which are used to read and write the XNOR-XOR storage bit. Although some XNOR-XOR cell implementations use lower area DRAM cells [27], [30], typically, XNOR-XOR cells use XNOR-XOR storage. The bit comparison, which is logically equivalent to an XOR of the stored bit and the search bit is implemented in a somewhat different fashion in the NOR and the NAND cells.

NOR Cell

The NOR cell implements the comparison between the complementary stored bit, D, and the complementary search data on the complementary search line, SL, using four comparison transistors, M1 through M4, which are all typically minimum-size to maintain high cell density. These transistors implement the pull down path of a dynamic XNOR logic gate with inputs SL and D. Each pair of transistors, M1/M4 and M2/M3, forms a pull down path from the match line, ML, such that a mismatch of SL and D activates least one of the pull down paths, Connecting ML to ground. A match of SL and D disables both pull down paths, disconnecting ML from ground. The NOR nature of this cell becomes clear when multiple cells are connected in parallel to form a XNOR-XOR word by shorting the ML of each cell to the ML of adjacent cells. The pull down paths connect in parallel resembling the pull down path of a CMOS NOR logic gate. There is a match condition on a given ML only if every individual cell in the word has a match.

NAND Cell

The NAND cell implements the comparison between the stored bit, D, and corresponding search data on the corresponding search lines, (SL, \overline{SL}), using the three comparison transistors, M1, MD and \overline{MD} , which are all typically minimum-size to maintain high cell density. We illustrate the bit-comparison operation of a NAND cell through an example. Consider the case of a match when SL=1 and D=1. Pass transistor is ON and passes the logic "1" on the SL to node B. Node B is the bit-match node which is logic "1" if there is a match in the cell. The logic "1" on node B turns ON transistor. Note that is also turned ON in the other match case. In this case, the transistor passes logic high to raise node B. The remaining cases result in a miss condition, and accordingly node B is logic "0" and the transistor is OFF. Node B is a pass-transistor implementation of the XNOR function. The NAND nature of this cell becomes clear when multiple NAND cells are serially connected. In this case, the and nodes are joined to form a word. A serial nMOS chain of all the transistors resembles the pulldown path of a CMOS NAND logic gate. A match condition for the entire word occurs only if every cell in a word is in the match condition. An important property of the NOR cell is that it provides a full rail voltage at the gates of all comparison transistors. On the other hand, a deficiency of the NAND cell is that it provides only a reduced logic "1" voltage at node B, which can reach only when the search lines are driven to (where is the supply voltage and is the nMOS threshold voltage).

When the bit comparison succeeds in this cell, one of the transistor paths between and is ON. Thus, when multiple cells are shorted together these transistor paths appear in series just as in the pulldown network of a CMOS NAND gate. Since this NAND cell doubles the number of transistors in series, the 9-T NAND is usually preferred. For the remainder of this paper discuss only the 9-T NAND cell and the 10-T NOR cells as they are in predominant use today

XNOR-XOR CELL (reduced T)

The XNOR-XOR cells are organized into rows (word) and columns (bit). Each cell has the same number of transistors as the conventional P-type NOR XNOR-XOR and use a similar ML structure. However, the —COMPARISON unit, i.e., transistors M1 to M4, and the —XNOR- XOR unit, i.e. the cross coupled inverters, are powered by two separate metal rails, namely VDDML and the VDD, respectively. The VDD is independently controlled by a power transistor Px and a feedback loop that can auto turn-off the ML current to save power. The purpose of having two separate power rails of (VDD and VDDML) is to completely isolate the XNOR-XOR cell from any possibility of power disturbances during COMPARE cycle. The gated-power

transistor P_x , is controlled by a feedback loop, denoted as Power Control which will automatically turn off P_x once the voltage on the ML reaches a certain threshold. At the beginning of each cycle, the ML is first initialized by a global control signal EN. At this time, signal EN is set to low and the power transistor P_x is turned OFF. This will make the signal ML and C1 initialized to ground and VDD, respectively. After that, signal EN turns HIGH and initiates the COMPARE phase. If one or more mismatches happen in the XNOR-XOR cells, the ML will be charged up. Interestingly, all the cells of a row will share the limited current offered by the transistor P_x , despite whatever number of mismatches. When the voltage of the ML reaches the threshold voltage of transistor M8. Voltage at node C1 will be pulled down. After a certain but very minor delay, the NAND2 gate will be toggled and thus the power transistor P_x is turned off again. As a result, the ML is not fully charged to VDD, but limited to some voltage slightly above the threshold voltage of M8.

4. PROPOSED SYSTEM

Power dissipation due to memories has become a major concern of modern digital design. Scaling of CMOS technology has led to short channel effects. Here XNOR-XOR cells are designed using reduced T which have better gate control over drain to source current. The XNOR-XOR cells designed with 30nm LG are used in multi-segment hybrid XNOR-XOR architecture. The results are compared with the original hybrid XNOR-XOR. It is observed that the energy metric of proposed architecture is 7% less compared to hybrid XNOR-XOR. In Static RAM Memory (XNOR-XOR), the input is associated with the data stored in the memory and output is the location where the content is stored. XNOR-XOR can be used as a search engine for finding the matched contents in a database or a table. In XNOR-XOR applications where more than one word may match, a priority encoder is used¹. Internet is a combination of routers and switches. Packets are sent from source to destination with the help of router. The task of a router is to connect multiple networks and compare the destination of packets such that the packet reaches proper destination. Routers use lookup operation which demands fast search operation thus lookup can be implemented using XNOR-XOR. But there is tradeoff among the speed of XNOR-XOR, silicon area and power consumption. ICs use a few percentage of world's electricity today but power per chip is growing. If power consumption is not reduced, industry's future growth will be at risk. To achieve performance, lower power consumption and portability, CMOS devices have been scaling down for years. To control the power consumption, the supply voltage is scaled down but leads to several problems such as short channel effects, drain induced barrier lowering, sub threshold slope degradation, and punch through, hot electron effect and leakage power³. Memory consumes 60–70% of the total power consumption in a chip². Leakage power is a major concern in memories. reduced T can enhance the drive current of MOS structures and can improve the very daunting short channel effect that affects I-V characteristics of the device⁴. In this paper, shorted gate reduced T is used in which the two gates are shorted together to give high current drive (ION). The multi-segment hybrid-type XNOR-XOR was implemented in 30nm reduced T technology, the compact model used is BSIMCMG107.0.0_20130712 (Berkeley Short-Channel IGFET Model Common Multi-Gate). Asymmetric Short Gate (ASG) reduced T has no effect on parasitic capacitance. The experimental results show impressive reduction in the search power consumption. The Match delay of all the design is also calculated to obtain the Energy Metric.

Reduced T Devices The main component that distinguishes the reduced T process from the planar CMOS counterpart is the fin, which provides the channel for conducting current when the device is switched on. This vertical fin is surrounded on three sides by the gate, and hence, a more efficient control over the channel is established, which in turn helps to reduce SCE. Key geometric parameters of a reduced T device include the fin height (H_{FIN}), the fin width, also known as the silicon thickness (TSI), the gate or fin length (LF_{IN}) and the gate underlap (ul), which is the distance between the edge of the gate strip and source (or drain) terminal. This gate underlap is introduced to mitigate the direct source-to-drain tunneling (DSDT) current, which subsequently diminishes source and drain controls over the channel, thereby further improving the immunity of reduced T devices to SCE. The effective channel width of a single-fin reduced T is equal to $W_{min} = 2 \times H_{FIN} + TSI$, which is the minimum achievable channel width in reduced T. However, in order to increase the width (strength) of a reduced T device, more fins in parallel are added. Hence, the layout area of a reduced T device is proportional to:

- (i) the number of fins; and
- (ii) the value of PF_{IN} , which is dictated by the underlying reduced T technology.

7 nm reduced T Devices: In this paper, we intend to investigate the power and performance behaviors of advanced reduced T devices on memory designs. Accordingly, reduced T devices with an actual gate length of 7 nm are adopted. However, since no industrial data for such deeply- scaled reduced T devices are publicly available, our 7-nm reduced T devices are modeled and simulated using Synopsys Sentaurus Device [10]. Table 1 reports the design parameters of the baseline (standard) 7-nm reduced T device. More precisely, the gate length of the baseline device is 7 nm, with 1.5-nm gate underlap on each side, resulting in a channel length of 10 nm. Furthermore, the supply voltage, V_{dd} , is 0.45 V for super-threshold, and 0.3 V for near- threshold operations.

In addition to the baseline device, we developed six other variations of 7-nm reduced T devices with only one geometry changed per device. In order to avoid significant changes in the layout structure and manufacturing steps, we selected 10%–15% variation from the nominal value of LF_{IN} , TSI and tox . However, the value of ul has been aggressively (50%) increased in order to better study the impact of the gate underlap on reduced T characteristics. $|IDS|$ vs. the VGS characteristics of baseline, $high_{tsi}$, and $high_{lreduced}$ T devices. The threshold voltage values, V_t , of our reduced T devices are between 0.2 V and 0.25 V.

4.1 Static RAM Memory (XNOR-XOR)

The XNOR-XOR mainly consists of an array of memory cells. Each cell has two units, store unit and compare unit. The store unit, which uses Cross-Coupled 6T XNOR-XOR, is used for storing the bit. The compare unit made of pass transistor logic is used to compare the search bit and stored bit. The XNOR-XOR cell can be of either XOR or XNOR type. The output of compare unit is fed to gate terminal of pull-down transistor $N5$. Based on the output of compare unit, the transistor may turn ON or OFF. Match line is connected to the pull-down transistor. If the transistor is ON (OFF), the match line discharges (charges)². Conventionally, there are two types of XNOR-XOR designs: NOR type and NAND type. In any XNOR-XOR design, there are two phases precharge and evaluation. In precharge phase, the match line is charged to high voltage level and in evaluation phase, the data in store unit and compare unit are compared. In the current age of technology advancement, it is necessary to design different new concepts to reduce area of the cell as well as power consumption. The adders are always meant to be the most fundamental requirements for process of high performance and other multi core devices. In present work a new XNOR gate using three transistors has been designed, which shows power dissipation of 0.03866W in 90nm technology with supply voltage of 1.2V. A single bit 3-2 and 4-2 Adder using eight transistors has been designed using proposed XNOR cell and a multiplexer, which shows power dissipation of 0.07736W. It is implemented by using synopsys tool (Version-L- 2016.06-8) using custom compiler with 90nm technology.

The low-power design has become a major design consideration. The design criterion of a 3-2 and 4-2 Adder cell is usually multi-fold. Transistor count is, of course, a primary concern which largely affects the design complexity of many function units such as multiplier and algorithmic logic unit (ALU). The limited power supply capability of present battery technology has made power consumption an important figure in portable devices. The speed of the design is limited by size of the transistors, parasitic capacitance and delay in the critical path. The driving capability of a 3-2 and 4-2 Adder is very important, because, 3-2 and 4-2 Adder s are mostly used in cascade configuration, where the output of one provides the input for other. If the 3-2 and 4-2 Adder s lack driving capability then it requires additional buffer, which consequently increases the power dissipation. In the last decade, the 3-2 and 4-2 Adder has gone through substantial improvement in power consumption, speed and size, but at the cost of weak driving capability and reduced voltage swing. However, reduced voltage swing has the advantage of lower power consumption.

Initially the electronics started their evolution with the invention of vacuum tubes. But with the help of Vacuum tubes only the movement of electrons were studied. After vacuum tubes transistors and diodes were introduced. But for larger circuits it was difficult to fabricate them in a board as they occupied larger space and consumed more power. The 3-2 and 4-2 Adder circuit performance is dependent on the approach for designing the circuit. The speed of operation of a circuit is indirectly found with the help of delay time calculation which directly depends on the transistor count, the logic depth and other criteria. The power consumption depends on the switching activity and the number and the transistor size. The transistor size and routing complexity helps to know the area of a die. Circuit realization for low area has become an important issue with the growth of integrated circuit towards very high integration density and high operating frequencies. Due to the important role played by XNOR gate in various circuits especially in arithmetic

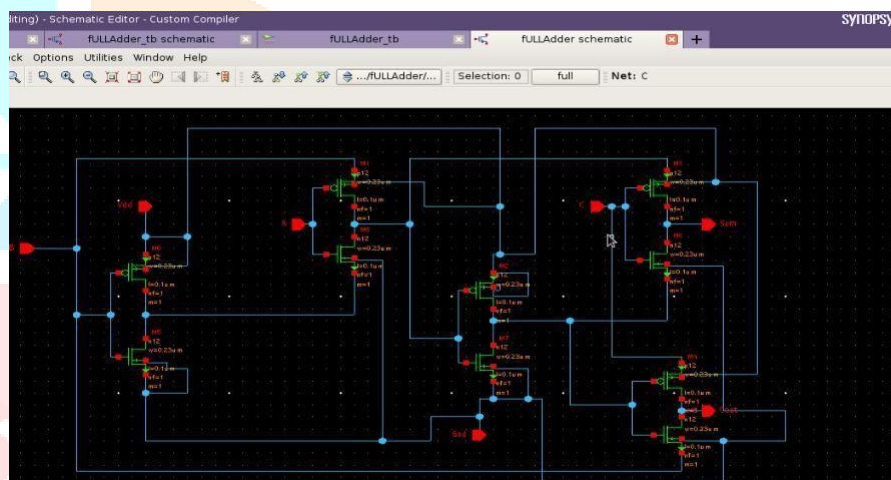
circuits, optimized design XNOR circuit to achieve small size and delay is needed. The primary concern to design XNOR gate is to obtain low power consumption and delay in the critical path and full output voltage swing with low number of transistors to implement it. A survey of literature reveals a wide spectrum of different types of XNOR gates that have been realized over the years. The early designs of XNOR gates were based on either 4 transistors [3] or

3 transistors that are conventionally used in most designs. 3-2 and 4-2 Adder acts as the basic block of all adders which are used to perform multi bit additions. There are also various ways to design the 3-2 and 4-2 Adder circuit in terms of CMOS logic. With increasing demand in speed and power, our main aim is to design 3-2 and 4-2 Adder circuit so that it consumes less power and faster. Most of the power in any circuit is being consumed by the power given to the data path of the circuit which consists of the transistors. Hence by reducing the number of transistors we can reduce the power consumption also by reducing the data path, the circuit can be made faster.

5. METHODOLOGY

5.1 CONVENTIONAL 10T 3-2 AND 4-2 ADDER

The schematic of the conventional 10T CMOS 3-2 and 4-2 Adder. The 10T CMOS 3-2 and 4-2 Adder circuit design is optimized to consume less power and less fabrication area with lesser internal capacitance. Respective simulation results showing the output waveform and output power of 10T 3-2 and 4-2 Adder design with 90nm CMOS technology are depicted.



5.2 PROPOSED 3-2 AND 4-2 ADDER: BASIC BUILDING BLOCKS

1. THREE TRANSISTOR XNOR GATE

The XNOR gate (sometimes, EXNOR, ENOR, and, rarely, NXOR, XAND) is a digital logic gate whose function is the logical complement of the exclusive OR (XOR) gate. A high output (1) results if both of the inputs to the gate are the same. If one but not both inputs are high (1), a low output (0) results.

2. XNOR GATE WORKING

In the proposed XNOR cell 1 PMOS transistor and 2 NMOS transistors. The systems behavior for different inputs are described: The presented design comprises of three transistors, out of which two are NMOS and one is PMOS. The W/L ratios are maintained such that the area is minimum by keeping the output voltage swing maximum. The body terminal of the PM0 is connected to the VDD while the body terminals of the NM0 and NM1 are connected to the GND terminal. This ensures the body effect to be least. The PM0 passes a strong „1“ and a weak „0“. Whereas the NM0 and NM1 passes a strong „0“ and a weak „1“. The functionality of the 3T XNOR gate is described below:

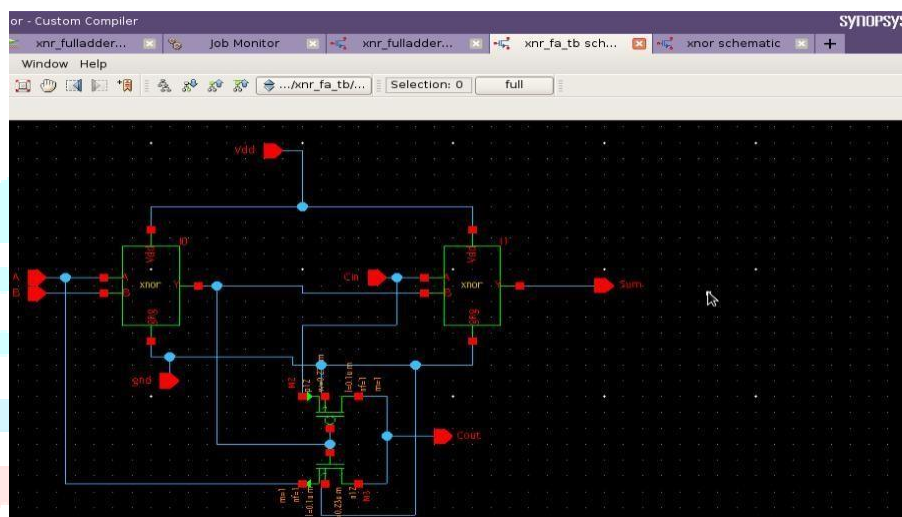
Case 1: When A=0 and B=0. When both the inputs are at 0V, the NM0 and NM1 are turned OFF the VDD appears across the PMOS. This results in an 1V output across the output terminal Y and GND

Case 2 and 3: When (A=0 and B=1) or (A=1 and B=0). When either of the input is „1“ and the other is „0“. The NMOS which is turned ON will pass a strong „0“ to the output. This results as „0“ for both the cases.

Case 4: When A=1 and B=1. When both the NMOS are turned ON by providing „1“ for both the input terminals, the output across the output terminal is generated by both the NMOS and PMOS. The NMOS generates a weak “1” whereas the PMOS generates a strong “1”. As a result, a strong “0” is obtained at the output. The output waveforms of proposed xnor gate.

5.3 DESIGN & IMPLEMENTATION OF 3-2 AND 4-2 ADDER CIRCUIT

3-2 and 4-2 Adder circuit can be implemented with different combinations of XOR/XNOR modules and two multiplexers but this approach has not been used in current work as XNOR/XOR cell shows high power consumption than single XNOR gate. Proposed 3-2 and 4-2 Adder circuit has been implemented by two XNOR gates and one multiplexer block. Sum is generated by two XNOR gates and Cout is generated by two transistors multiplexer block. The single bit 3-2 and 4-2 Adder using proposed XNOR gates with eight transistors has been implemented. For multiplexer section typical values of width (Wn & WP) 0.23 μ m & 0.23 μ m for NMOS and PMOS transistors have been taken with gate length of 0.9 μ m. Simulations have been performed using SPICE based on SAE (Simulation and Analysis Environment) 0.9 μ m CMOS technology with supply voltage of 1.2V.



6. EXPERIMENTAL RESULT

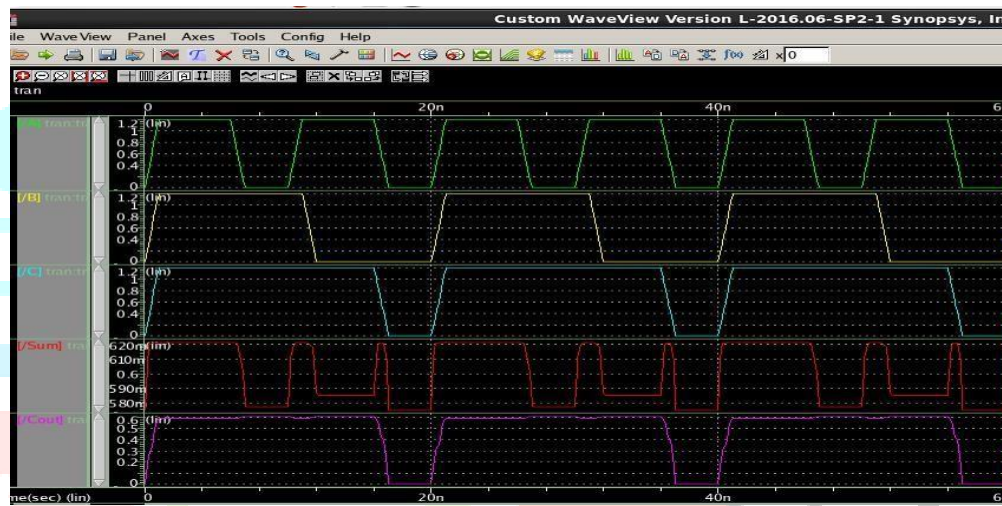
Output wave forms of conventional and proposed 3-2 and 4-2 Adders



Fig 1: Output Waveform of proposed 3T XNOR Gate



Fig 2: Output Waveform of Conventional 10T 3-2 and 4-2 Adder



6.1. TABULATION OF SIMULATION RESULTS: XNOR GATE

Supply Voltage (V)	Power Dissipation(W)
3	0.62536
2.5	0.377959
2	0.210017
1.2	0.03866

6.2 TABULATION OF SIMULATION RESULTS: PROPOSED 3-2 AND 4-2 ADDER

Supply Voltage (V)	Power Dissipation(W)
1.5	0.178589
2.5	0.756103
2	0.42
1.2	0.07736

In this proposed paper, a new low power XNOR gate using three transistors has been presented, which shows power dissipation of 0.03866W in 90nm technology. Compared with earlier reported XNOR gates, proposed circuit shows less power consumption and better output signals with reduce transistor count. A single bit 3-2 and 4-2 Adder using eight transistors has been designed using proposed XNOR cell, which shows power dissipation of 0.07736W. Power consumption of proposed XNOR gate and 3-2 and 4-2 Adder circuits shows better performance in terms of power consumption and transistor count.

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