IJCRT.ORG ISSN : 2320-2882

INTERNATIONAL JOURNAL OF CREATIVE RESEARCH THOUGHTS (IJCRT)

An International Open Access, Peer-reviewed, Refereed Journal

RESEARCH AND ANALYSIS ON INTEGRATED CIRCUIT TESTING AND FAULT DIAGNOSIS IN VLSI

Sompalli Nithin, Student, electronics and communication, sir m Visvesvaraya institute of Technology Bangalore 562157

ABSTRACT:

Fault detection systems in the pre-silicon stage have become increasingly important in ensuring the dependability of IC designs as the scale and complexity of VLSI designs continue to increase.Testing is very important for the diagnosis of faults at an earlier stage for any system, in particular, it is critical for the integrated circuits as the replacement is highly expensive. It is very complex to scaled-down the technologies due to the non-availability of mature models. In this thesis, various test and fault diagnosis techniques are studied, and modified algorithms for improvements are applied to chosen FinFET-based circuits. The effectiveness of the Built-in Self-Test (BIST) in finding faults is analysed concerning salient figures of merit including maximum fault coverage, speed, power dissipation, and test area overhead leading to improved design performance. A systolic array multiplier 94X4 is designed with reversible gates and Built-In Logic Block Observer (BILBO) logic is used for fault injection. Further, in this thesis suitability of PODEM algorithm for fault location is explored It is found that the application of AXI BIST results in significant improvement in speed (74%) and consumes power by 50%. Fault coverage (> 95%) is maximized through ROBDD. A reduced setup time could be achieved (2.3 ns) through selected Vedic algorithms.

Keywords: Fault diagnosis, Built in Self- Test (BIST), FinFET, Built-In Logic Block Observer (BILBO).

1. INTRODUCTION

Now a days VLSI Devices have almost reached boundaries of Moore's law. The feature size reached almost sub 7nm. With increased complexity in design, higher frequency of operation, larger device density and more reliable performance lead to multi core device technologies posing several challenges in testing [2, 3] to find correctness of design meeting specifications and fault free operation facilitating defect free delivery of chips. Diagnosis and early detection of the faults reduces cost almost ten times that may escalate at every subsequent state of percolation as per rule of Ten [4]. Testing ensures enhanced yield with improved quality and reliability though it is cumbersome and not feasible at device level. Testing and Fault diagnosis has become very important constituent for VLSI circuit designs. Also, design for testability has become mandatory [5] to increase the controllability and observability. Towards this end, several failure mechanisms are diagnosed and testing algorithms including built in self-test (BIST) [6] are being adopted to achieve maximum fault coverage, reduced power consumption and area overhead without compromising speed.

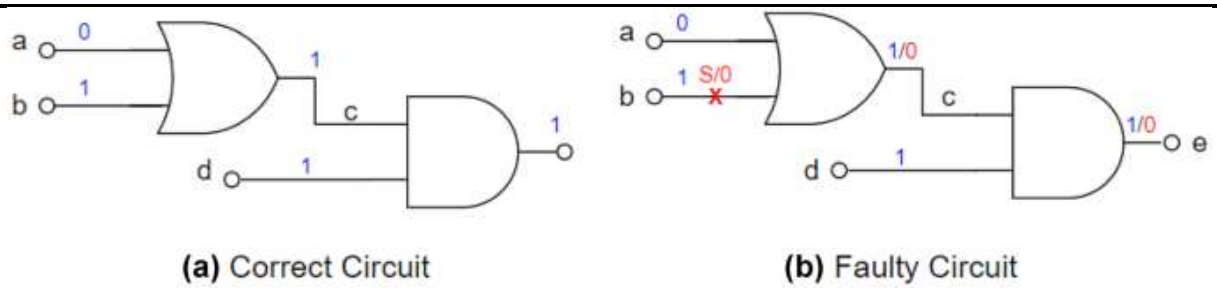

Fig 1.Simple example of correct Circuit in **a** and faulty circuit in **b**

Figure 1 shows a basic, correct circuit (Circuit a) and a faulty circuit (Circuit b).The scaled down technologies suffer from substantial leakage current [7]. This problem is addressed through FinFET technology. The structure of the FinFET is compact, thin, and sophisticated.The fin is blocked from the short channel effect by being encased between the gate's front and back halves. Due to its easy manufacturing process and strong compatibility with planar MOSFET [9], FinFETs are regarded as one of the most practical multi-gate devices [1, 8].FinFET based circuits become more effective while performing numerous switching operations that require high speed, reduced power even though they occupy 94% of the chip area [10]. For diagnosing critical faults, There are various types of fault models available in FinFET's [11]. On the other hand, fault modeling for single planar was investigated extensively through bridging, stuck-at, delay and stuck-open faults [12]. All faults in FinFET logic gates cannot be accounted for by these CMOS fault models [13]. The stuck-at fault model is commonly used for fault detection. Defects are detected in the behaviour of both combinational and sequential circuits [14], but testing and bridging of delay faults become crucial as technology scales. Delay tests in combinational logic and sequential circuits are analysed and predicted using statistical timing analysis [15], which also creates novel advancements in fault identification.

1.1 Motivation

The processing stages involved in VLSI circuits are exceedingly complicated and expensive, which is why manufacturers are placing a greater emphasis on testability as a requirement tool. This is done to ensure that each of their designed circuits is both reliable and able to perform as intended. Various testing, fault diagnostic techniques and heuristic algorithms are being employed to find out stuck at faults, delay faults, bridging faults, toggle or transition faults missing gate faults etc., to achieve max faultcoverage, less power consumption, increased speed of testing, smaller area over head. Incremental computation algorithm with max operator is employed to find out target path delay fault PDF that suffers from limitation in computation time of testing. SSTA was performed using Skew Normal Canonical Model to mitigate non skewness in gate delay distribution in Planar CMOS based Circuits. Non-incremental Genetic Algorithm instead of Monte carlo or Max operator was preferred to find Target Path Delay Fault PDF of FinFET based VLSI circuits to achieve fast computation time.

1.2 Research Objectives

- This thesis aims to perform testing and fault diagnosis on VLSI circuits with improved speed, fault coverage, reduced power and area constraints.
- To find faults: Stuck at faults (SAF) and Multiple SAF (MSAF), Delay Faults (DF), Transition Faults (TF), Bridging Faults(BF), Fault Detection or Location and Missing Gate Faults(MGF).
- To design target circuits: FinFET based Combinational circuits and CPU sub-blocks

2. LITERATURE SURVEY

Maintenance and its associated tasks have long been crucial in a manufacturing setting. With repeated processing cycles comes wear and tear on the production system's machinery, which reduces its technical efficiency compared to

when it was operating under ideal conditions [K. Gandhi, 2018,[1]].

A maintenance process can be managed in a number of different ways (Figure 1): When anything happens that hinders, even temporarily, the continuation of an activity, an interruption of a service, or the degradation of a service to the point where it can no longer be supplied in a safe or efficient manner, corrective maintenance becomes necessary.

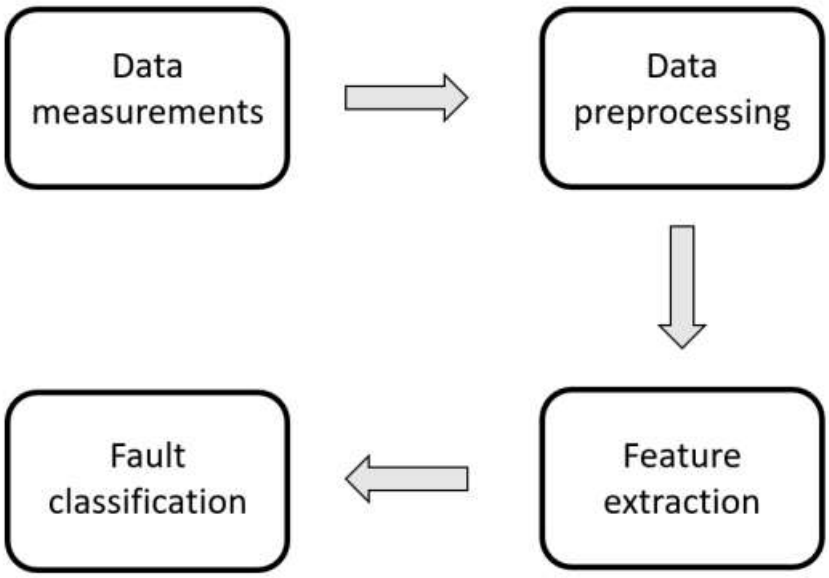

Figure 2. Scheme of a typical fault diagnosis process.

Jiang et al. [2] have used RNNs to diagnose problems with rolling bearings. By employing the frequency spectrum sequences of the vibrational signals as input, the scientists were able to reduce the quantity of data that had to be kept while still ensuring its reliability. Extracting characteristics from input spectrum sequences automatically and the repeating hidden layer has been implemented, and during the training phase, an adjustable learning rate has been implemented in order to improve the model's overall performance.

LSTMs were utilised by Yang et al. [3] for the purpose of diagnosing transmission faults in wind turbines. The study authors utilised a strategy that exploited the correlations between space and time in the measurement signals collected by a plethora of sensors installed in rotating machinery. This allowed them to identify the various fault kinds and move forward with classifying them.

To evaluate an LSTM-based fault detection model, An et al. [4] employed a dataset consisting of vibration signals from bearings of rotating machines operating at varying speeds and loads across time. Throughout the research, the speeds and loads were changed. Segmenting the data is the first step, sending the classification labels to the LSTM is the second, and determining the failure probability is the responsibility of the output network.

Liu et al. [5] looked at rotating machines once more in their research and applied LSTMs to the problem of finding defects. After taking readings of the vibration signals, the authors subdivided those readings in order to reduce the total length of the timeline. Utilising a cellular structure with a forgetting gate allowed them to circumvent the issue of an LSTM's need for a large number of parameters and calculations, which was another issue they tackled.

Liang et al. [6] created a model based on a recurrent convolutional neural network to solve the challenge of accurate problem detection in a high-speed train's bogie. After picking up on vibratory signals from

the cart, scientists used convolutional layers to sift through the data and extract relevant information. The features are then sent to the recurrent layers through a simple recurring cell, which logs results that are better than a CNN's and models based on the ensemble's learning.

After that, Huang et al. [7] utilised a model that was built on an LSTM in order to solve the identical problem. The authors generated the fault data with the help of the simulation software SIMPACK. After that, the information was used to train and test a network, and it proved adept at discovering the spatial and temporal correlation of fault characteristics in vibration signals without any additional data preprocessing or prior experience.

RNNs were utilised by Shahnazari et al. [8] for the purpose of defect detection and isolation in an HVAC system. Heating, Ventilating, and Air Conditioning is an abbreviation for those systems. In order to include the plant data into the filters used by the diagnosis system, the authors created prediction models. The method was validated by putting it through its paces using both simulated data and actual data on a test bench.

Linear Feedback Shift Registers, or LFSRs for short, are typically put to use in traditional BIST circuits in order to generate test patterns. It is possible to build four different kinds of test patterns: deterministic, algorithmic, exhaustive, and pseudo-exhaustive. Share mode allows the BIST controller to function when testing many CPUs [9]. The 'Test Result' is determined by the ORA's comparison of the actual signature value from the CUT with the expected signature value.Reinaldo Silveira and others [9] came up with the idea of a flexible BIST architecture, which they used to improve the already-existent basic design and cut down on the amount of circuit area.

3. METHODOLOGY

3.1 Testing and Fault diagnosis in FinFET Combinational Circuits

FinFET circuits are subjected to testing and fault diagnosis, with a matching fault analysis provided utilising a non-incremental genetic algorithm. After creating the schematic for the NAND, NOT, and NOR gates in LT Spice with the PTM package, the net list was sent to MATLAB for further analysis. Using the mean, variance, and standard deviation values, the critical path delay for alogrithm 2.1-designed circuits is computed, and the PDF graph for the critical path delay is presented (Figures 3 and 4).

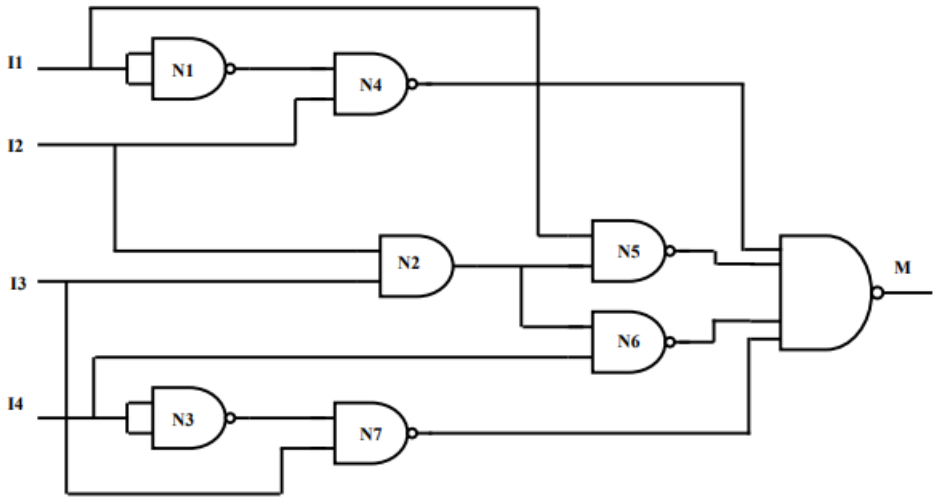

Figure 3. NAND gate design test circuit 1

Algorithm 3.1: Genetic Algorithm: GA(n, χ, μ)

1: Initialize generation 0 : K := 0;

2: PK : = a population of n randomly-generated individuals;

3: Evaluate PK:

4: compute Θ(i) for each I ε PK do

5: Create generation k + I :

6: I. Copy:

7: Select (l X z) x n members of P k and insert into P k + l;

8: Mutate::

9: Select μ X n members of PK; invert a randomly – selected bit in each;

10: Evaluate P k + l

11: Compute θ(i) for each iεPK;

12: Increment:

13: K : K + 1;}

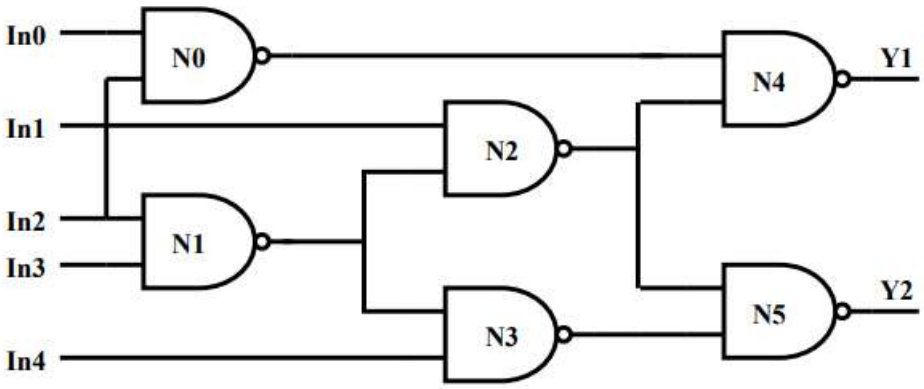

Figure 4. NAND gate design test circuit 2

3.2 Testing and fault diagnosis of sequential logic circuits

32-bit RISC architecture

A general-purpose 32-bit RISC processor is shown in Fig 5 consists of 5-stage pipelining implemented by fetch, decode, execute, memory, and write back stages for data read or write operations. This architecture is designed as separate data and instruction interface i.e., Harvard architecture which reduces hardware complexity. The address generation is done by

RAM when connected to the BIST controller, whereas it runs with test vectors with valid reads and writes.

3.3 Implementation of VMA on 32-bit RISC processor

VMA is implemented on RISC processor that follows concurrent testing sequences while entire memory can be grouped which are further subdivided into sub-groups. In each of the sub-group, primary faults are detected from all of the test vectors and forwarded to the groups. If more faults are detected, the group is selected individually and the last test vectors of the sub-groups are applied again till the diagnosis is finished.

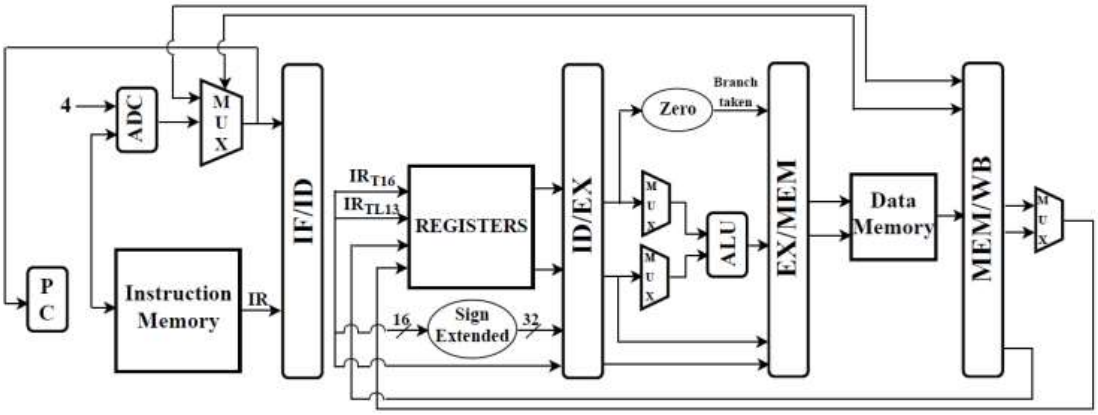

Figure 5. proposed method of 32 bit RISC Architecture.

4. RESULTS AND DISCUSSION

Transfer characteristics are presented once the simulation settings for each gate have been calculated.The formulas and computations for certain gates can then be found as depicted in Figures 6 and 7. Similarly, corresponging NOR and NOT gates of the transient and transfer curve are illustrated in Fig 8.The FinFET NAND gate's delay characteristics are depicted in Fig. 8.

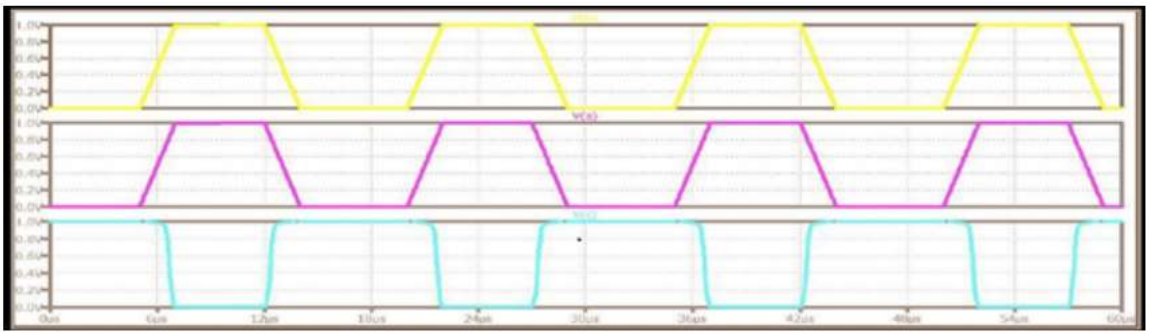

Figure 6 NAND GATE.

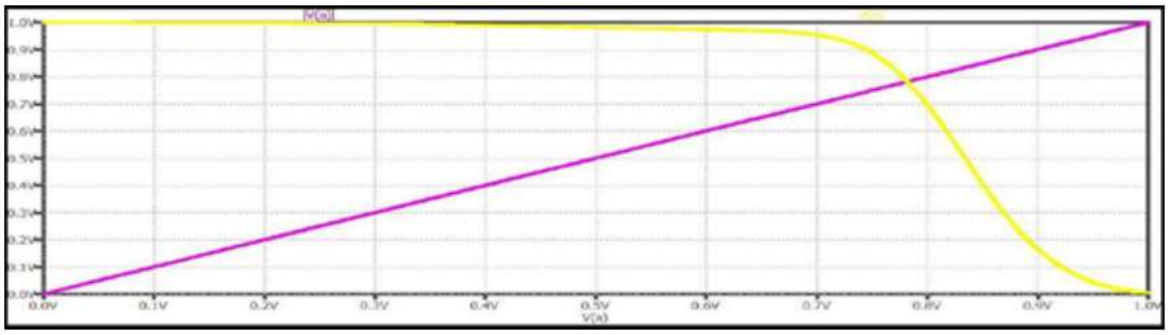

Figure 7 VTC Curve Delay calculations for NAND Gate.

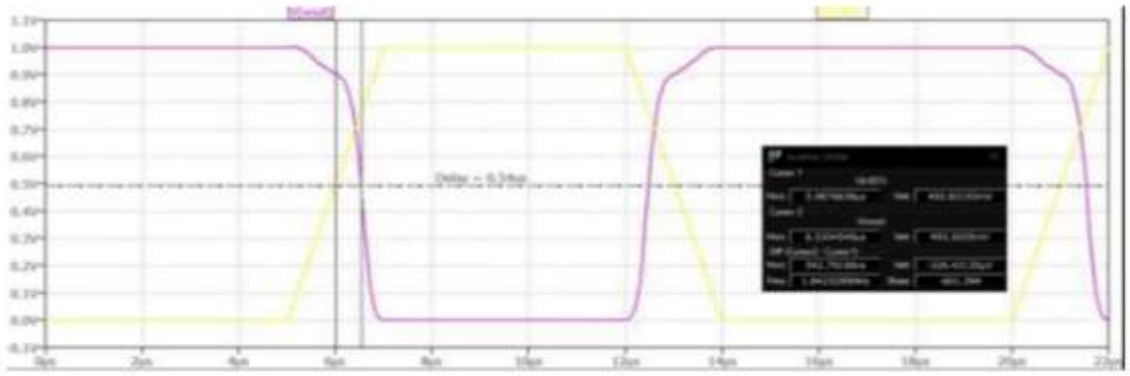

Figure 8. Propagation Delay (tp) for NAND Gate.

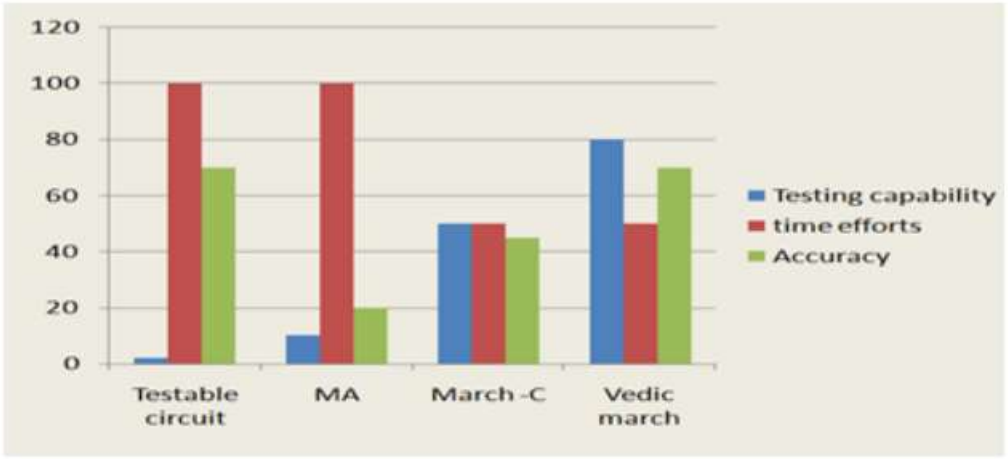

Figure 9. Performance chart for Modern approach testing compared with existing technologies

ROBBD can visualize the faults when tested across multiple corners by G11 and G22 operational blocks with reference to the Fig 9 for multiple read or write operations. It can detect the fault in the memory block whenever any bit or memory reached an undefined value.

Figure 10. Normal operation of DFF.

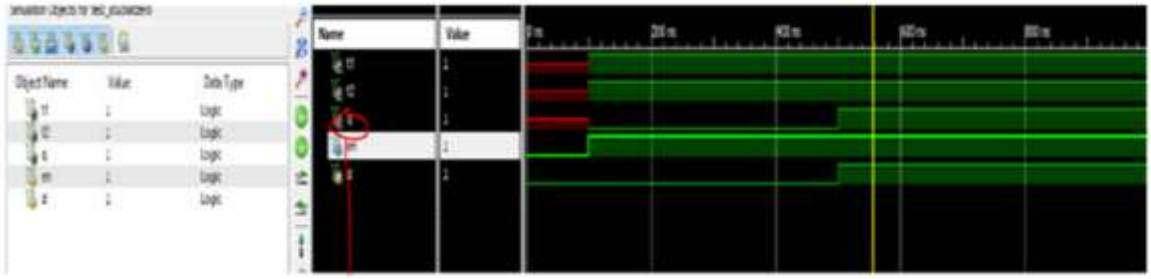

Figure 11. Stuck at '1' operation of DFF

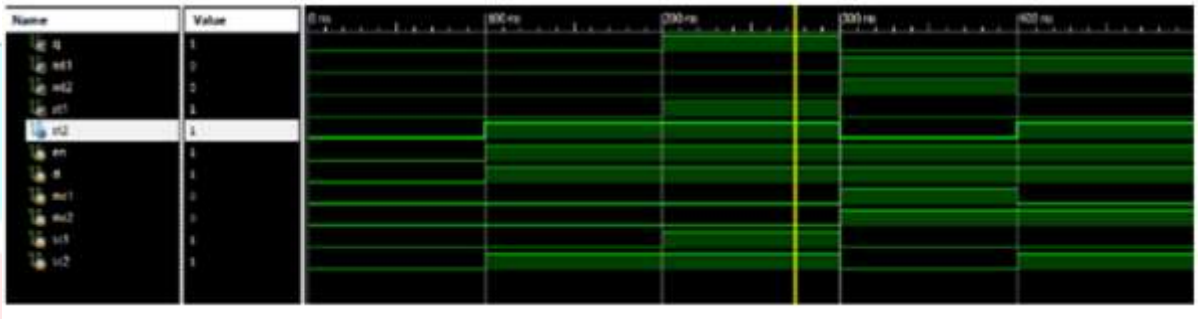

Figure 12. Bridge fault (loss of connection)

In Fig.10, we see DFF operating normally in the absence of a control signal, and in Fig.11, we see stuck-at faults forming.The loss of connection between the bridges is observed in Fig.12 is not the outcome which was expected.

CONCLUSION

Testing and fault diagnosys is viable to detect the faults in the circuits and also increase the device performance and reliability. The design of testability is applied on latest VLSI designs and implemented through BIST concepts to increase the effectiveness of finding faults like stuck at fault, fault location, delay fault, toggling fault, transition fault, bridging fault, missing gate fault etc. The proposed algorithms will take suitable actions to improve the design performance of the circuit and optimized the fault objectives like maximum fault coverage, higher speed of testing, less test power dissipation and less test area overhead.

REFERENCES

1. 2. K. Gandhi, A. H. Ng, Machine maintenance decision support system: a systematic literature review, in Advances in Manufacturing Technology XXXII: Proceedings of the 16th International Conference on Manufacturing Research, incorporating the 33rd National Conference on Manufacturing Research, September 11–13, University of Skövde, IOS Press, Sweden, 8 (2018), 349.
2. 141.H. Jiang, X. Li, H. Shao, K. Zhao, Intelligent fault diagnosis of rolling bearings using an improved deep recurrent neural network, Meas. Sci. Technol., 29 (2018), 065107. https://doi.org/10.1088/1361-6501/aab945
3. 143.R. Yang, M. Huang, Q. Lu, M. Zhong, Rotating machinery fault

diagnosis using long-short-term memory recurrent neural network, IFAC-PapersOnLine, 51 (2018), 228–232. https://doi.org/10.1016/j.ifacol.2018.09.582

4. 146.Z. An, S. Li, J. Wang, X. Jiang, A novel bearing intelligent fault diagnosis framework under timevarying working conditions using recurrent neural network, ISA Trans., 100 (2020), 155–170. https://doi.org/10.1016/j.isatra.2019.11.010
5. 147.W. Liu, P. Guo, L. Ye, A low-delay lightweight recurrent neural network (LLRNN) for rotating machinery fault diagnosis, Sensors, 19 (2019), 3109. https://doi.org/10.3390/s19143109
6. 148.K. Liang, N. Qin, D. Huang, Y. Fu, Convolutional recurrent neural network for fault diagnosis of high-speed train bogie, Complexity, 2018 (2018). https://doi.org/10.1155/2018/4501952
7. 149.D. Huang, Y. Fu, N. Qin, S. Gao, Fault diagnosis of high-speed train bogie based on LSTM neural network, Sci. Chin. Inf. Sci., 64 (2021), 1–3. https://doi.org/10.1007/s11432-018-9543-8
8. 150.H. Shahnazari, P. Mhaskar, J. M. House, T. I. Salsbury, Modeling and fault diagnosis design for HVAC systems using recurrent neural networks, Comput. Chem. Eng., 126 (2019), 189–203. https://doi.org/10.1016/j.compchemeng.2019.04.011
9. R. Silveira, Q. Qureshi, and R. Zeli, “Flexible architecture of memory bists,” in 2018 IEEE 19th Latin-American Test Symposium (LATS). IEEE, 2018, pp. 1–6.
10. Gaber L, Hussein AI, Moness M (2020) Incremental Automatic Correction for Digital VLSI Circuits. Presented at the Proceceeding 11th International Conference on VLSI (VLSI 2020)
11. Gaber L, Hussein AI, Moness M (2021) Fast Auto-Correction algorithm for Digital VLSI Circuits. Procedia Computer Science 182:95–102 Article Google Scholar
12. Osama M, Gaber L, Hussein AI, Mahmoud H (2018) An Efficient SAT-Based Test Generation Algorithm with GPU Accelerator. J Electron Test 34:511–527 Article Google Scholar
13. Rodríguez Gómez L (2017) Machine Learning Support for Logic Diagnosis. Doctoral dissertation, university of Stuttgart El Mandouh E, Wassal AG (2018) Application of Machine Learning Techniques in Post-Silicon Debugging and Bug Localization. J Electron Test 34:163–181 Article Google Scholar
14. Gaber L, Hussein AI, Mahmoud H, Mabrook MM, Moness M (2020) Computation of minimal unsatisfiable subformulas for SAT-based digital circuit error diagnosis. J Ambient Intel Humanized Comp pp 1–19.
15. Gaber L, Hussein AI, Moness M (2019) Improved automatic correction for digital VLSI circuits. In 2019 Proceeding 31st international conference on microelectronics (ICM), 2019, pp 18–22