IJCRT.ORG ISSN : 2320-2882

INTERNATIONAL JOURNAL OF CREATIVE RESEARCH THOUGHTS (IJCRT)

An International Open Access, Peer-reviewed, Refereed Journal

System Verilog Based Verification IP For Ethernet

[1] Kothapalli Hemanth Sekhar, [2]Dr. G. Mamatha

[1]PG Scholar, [2]Assistant Professor
Department of Electronics and Communication Engineering
JNTUA College of Engineering Anantapur, Ananthapuramu, India.

Abstract: Traditional guided test benches are no longer a practical testing solution due to the increasing design complexity of integrated circuits. Verification is a technique that can be used to show that a design is functionally sound. Automation reduces the likelihood of human error in the process. Automation completely eliminates human involvement from the Method. Automation, however, is not always feasible, particularly in poorly defined processes that nonetheless need for human intelligence and originality, like hardware design. There is an increasing need for guidelines and best practices to ensure successful verification IPs because testing has been replaced by verification utilizing verification IPs in modern times. In order to overcome the verification challenge of complicated Ethernet IP, a full truncation level verification environment is proposed in this paper. The most popular network architecture in use today is Ethernet. The project's primary goal is to test the Ethernet IP with various interfaces. Additionally, it covers the verification method and reuse of the design environment. Multiple degrees of reuse will be possible in the verification environment suggested by System Verilog, both inside and between projects. For simulation, we are utilising Mentor graphics Questasim.

Index Terms – Intellectual Property, Verification, Media Access Control, Media Independent Interface, Wishbone.

I. INTRODUCTION

Ethernet is a communication protocol that connects computers in networks called local area networks (LAN) and wide area networks (WAN). LANs and WANs connect different devices such as laptops and printers within homes, buildings, and even small areas. Ethernet is a lower layer of the Open Systems Interconnection (OSI) model. This facilitates physical layer and data link layer operations. Therefore, Ethernet is required for almost all electronic devices.

Verification IP (VIP) is a predefined functional block that you can insert into your testbench. It can be used to simulate the actual design which can be wither IP or SOC and verify its functional correctness. Development of this VIP includes development of transactions/sequences, drivers, configuration components, actual test plans for this interface, and test suites. This includes standalone verification of the VIP itself. This project aims to design and develop Verification IP for an Ethernet module connected to a processor through internal bus. The Ethernet module verification IP design and development is done in System Verilog,. By using this verification IP, we can guarantee the functionality of your Ethernet.

The main purpose of the project is to validate Ethernet IP on various interfaces. We also discuss verification strategies and design environment reuse related to Ethernet packet verification on the Ethernet Intellectual Property (IP) core. The proposed validation atmosphere provides multiple levels of reuse, both within and across projects. This approach met all the stringent requirements for validating this complex protocol. This verification environment can be reused in other projects.

II. ETHERNET

Ethernet is the industry-standard technology for connecting devices on a wired LAN or WAN. It enables devices to communicate with one another using a standard network language, set of rules, or protocol.

Ethernet is a term used to explain how network devices format and transmit data so that it may be seen, received, and processed by other hardware linked to the same LAN or campus network. An Ethernet cable is a physically jacketed data cable.

Ethernet may be used to connect devices when using cables rather than wireless connections to access geographically localized networks. The advantages of Ethernet connectivity, such as dependability and security, are relied upon by a variety of end users, including businesses and gamers. The interference potential of Ethernet is typically lower than that of wireless LAN technology. Because it needs physical wires to link devices. Compared to wireless technology, Ethernet provides a higher level of network security and control. This makes it more challenging for outsiders to access the data on your network or monitor the bandwidth usage of unwanted devices.

To connect devices to a network, Ethernet is still a widely utilized way of network access. Many organizations, including business offices, college campuses, and hospitals, use local area networks because of the speed, security, and dependability of Ethernet. Ethernet initially became popular because it was less expensive than competing technologies at the time, like IBM's Token Ring. Ethernet has continued to be popular because of its ability to adapt and provide higher levels of performance as network technology advanced.

III. WISHBONE

Wishbone is designed to facilitate the connection of various cores to various inners of a chip. Many designs within the OpenCores project utilize the Wishbone Bus.

Wishbone is intended to serve as a "logic bus". Electric records or the bus topology are not mentioned. The specification can also be written in terms of "signals," clock cycles, excessive levels of coffee, and so on. This ambiguity was deliberate. Wishbone is a tool for electronic design automation that enables designers to combine multiple designs created in common sense description languages like Verilog, VHDL, or others (EDA). A well-known method for designers to combine these hardware common sense designs is provided by Wishbone (known as "cores"). Wishbone is said to have buses that are 8, 16, 32, and 64 bits in size.

All signals are synchronized to an unmarried clock, but for best performance, some slave responses should be generated combinatorically. Wishbone enables the use of a "tag bus" in addition to the records themselves. However, reset, straightforward addressed reads and writes, block-by-block record movement, and indivisible bus cycles all function without tags. Wishbone is available. The Wishbone specification includes examples of prior art to show that its principles are in the public domain, preventing you from preemption of its technologies through competitive patenting.

Common topologies such as factor-to-factor, many-to-many, hierarchical, or even switched fabrics like crossbar switches are all well-suited for Wishbone. Wishbone requires a bus controller or arbiter in the more advanced topologies, but the devices still have the same interface.

IV. VERIFICATION ENVIRONMENT

Verification Environment includes five interfaces which are Wishbone master interface, Wishbone Slave interface, Mac transmission interface, Mac receiving interface, MMI interface. Wishbone interface is used for register programming and to perform register access tests. Figure 1 shows the verification environment for Ethernet DUT.

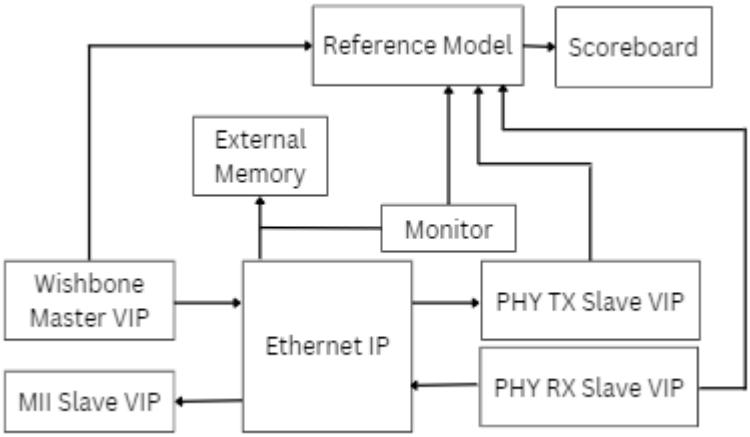

Fig.1

.Wishbone master interface is connected to external memory, Wishbone slave interface is connected to processor,MAC Transmission interface is a master interface which is connected to PHY, Mac receiving interface is a slave interface which is connected to PHY,MII Interface is a master interface which is connected to PHY.Master VIP includes driver, generator, monitor and coverage. Slave VIP includes only monitor and BFM. Reading all registers will be done by wishbone master generator. Read/Written values will be compared in reference model

V. TEST CASES

To verify the functionality of Ethernet IP four test cases are executed which are register reset, register read write, transmission in full duplex mode, transmission in half duplex mode, receiving in full duplex mode, collision detection

5.1 Register Reset

Accessed each register address and read reset value for each register. We can check register address on wb_dat_i. Register values are read on the signal wb_dat_o. In this test case all registers will configured to reset state and their values are read.

5.2 Register Read Write

Random data is written into random address and read from them. Data can verified from wb_dat_i and wb_dat_o signals.

5.3 Transmission in Half Duplex Mode

Transmitted Address in one time cycle and received data in next time cycle.Data is transmitted through wb_dat_o.

5.4 Transmission in Full Duplex Mode

Transmitted Address and data simultaneously in full duplex mode.Data is transmitted from DUT to MII through wb_dat_o and can be verified on mtxd_pad_o

5.5 Received in Full Duplex Mode

Received Address and data simultaneously in full duplex mode. .Data is transmitted from MII to DUT through mrxd_pad_i and can be verified on wb_dat_o.

VI. RESULTS AND DISCUSSION

After executing all test cases functionality of Ethernet is verified using waveforms obtained after simulation.

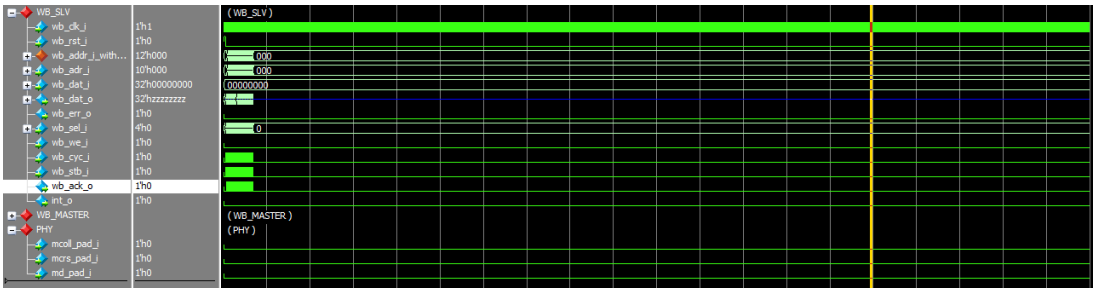

Fig.2. Register Reset Mode

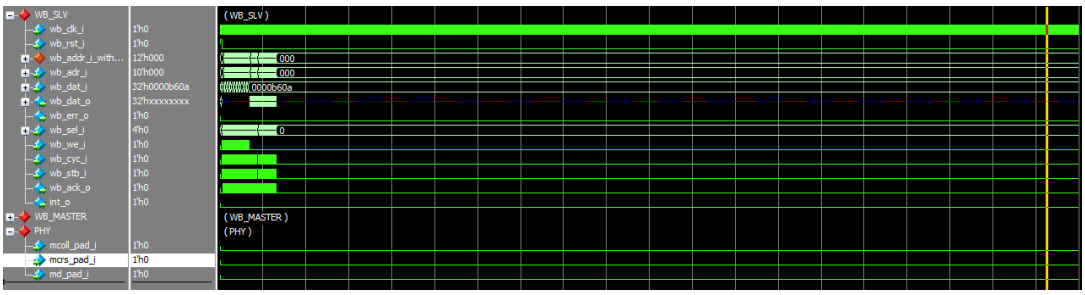

Fig.3. Register Read Write

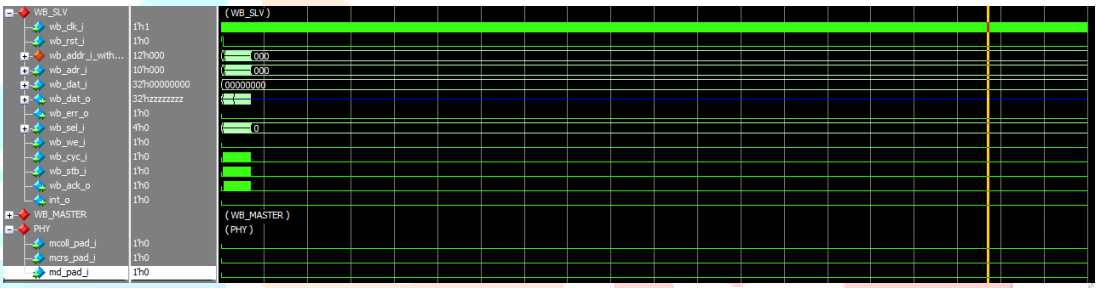

Fig.4. Half Duplex Transmission Mode

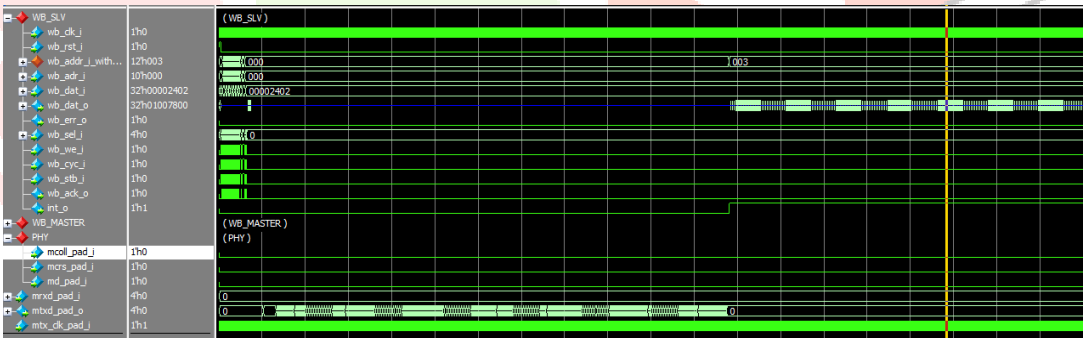

Fig.5. Full Duplex Transmission Mode

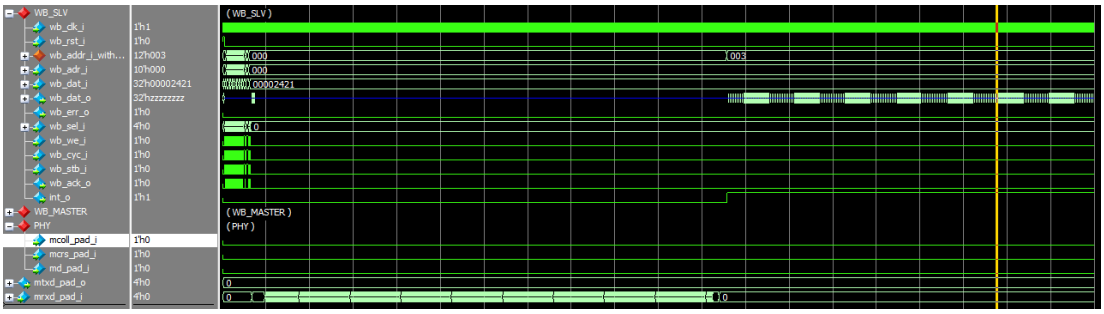

Fig.6. Full Duplex Receiving Mode

REFERENCES

[1]Shivleela G. Wadle ,Sanjaykumar K. Parchandekar , (2016) " Verification of Ethernet Protocol " , International Journal of Advance Computational Engineering and Networking (IJACEN) , pp. 1-3, Volume-4, Issue-8

[2]Selvakkani K, Venkatesan K, 2013, High Speed UVM B ased Verification IP For Gigabit Ethernet Protocol, INTERNATIONAL JOURNAL OF ENGINEERING RESEARCH & TECHNOLOGY (IJERT) Volume 02, Issue 12 (December 2013)

[3]Allu Jnana Prasuna, & D. P. Raju (2017, August). Design and Development of Gigabit Ethernet Verification IP (VIP) Using System Verilog. ISSN 2319-8885 Vol.06 Issue.27 Pages:5337-5340

[4]]Mentor Graphics, Verification Academy. UVM Cookbook. Mentor Graphics; 2012. p. 1-569.

[5]Spears C. System Verilog for Verification: A guide to learning the testbench language features. 2nd ed. Springer: Business Media LLC; 2007.

[6]Tonfat, J, Reis, R, "Design and Verification of a layer-2 Ethernet MAC classification Engine for a Gigabit Ethernet Switch", Proc IEEE Electronics, Circuits, and Systems doi.