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WALLACE TREE MULTIPLIER HAVING LOW POWER AND AREA EFFICIENT USING A BEC-1 CONVERTER

Shreya Sharma, Shreya Singh, Anamika Jha, Sonam Khan, Sneha Pandey

Graduate, Graduate, Graduate, Graduate, Professor

Electronics and Communication Engineering (B.Tech)

Noida Institute of Engineering Technology, Gautam Buddha Nagar, Uttar Pradesh, and India

Abstract: Multipliers are major blocks in most digital and high-performance systems such as Microprocessors, Signal processing Circuits, FIR filters, etc. In the present scenario, Fast multipliers with less power consumption are leading with their performance. Wallace tree multiplier with carry select adder (CSLA) is one of the fastest multipliers but utilizes more area. To improve the performance of this multiplier, CSLA is replaced by a binary excess1 counter (BEC) which not only reduces the area at the gate level but also reduces power consumption. Area and power calculations for the Wallace tree multiplier using CSLA with BEC are giving good results compared to the regular Wallace tree multiplier.

Index Terms - BEC Carry Select Adder (CSLA), Binary to Excess one converter (BEC), Square Root Carry Select Adder (SQRT CSLA), Field Programmable Gate Array (FPGA), Half Adder (HA), Full Adder (FA).

I. INTRODUCTION

Gone are the days when **gigantic** vacuum tube computers could **buzz in their private rooms** and do about 360 multiplications of 10 digits per **second**. It was hailed as the fastest computing machine of its time, but it certainly couldn't compete with today's machines. Modern computers are smaller, faster, cheaper, and more **energy efficient every** second. But what causes these changes? With the **advent** of Bardeen's (1947–48) semiconductor transistors and Shockley's (1949) bipolar junction transistors in Bell's **lab**, computer science heralded a new dawn in the **miniaturization of electronic devices as a whole**. Moore's **Law states that since Jack Kilby invented the first integrated circuit (IC) in the form of a flip-flop in 1958**, the ability to fit multiple transistors on a single chip has doubled about every 18 **months**. This exponential development has not been **seen** in any other **field** and **remains** an important area of **research**.

II. INTEGRATED CIRCUITS

A composite circuit or monolithic circuit (also known as a composite circuit, microchip, or microchip) is a set of electronic circuits in a small wafer ("chip") of semiconductor material, usually silicon. They can be made much smaller than separate circuits made of electronic components. Combined circuits may be small, with billions of transistors and other electrical components packaged in an area about the size of a claw. As technology evolves, the scope of each track in a circuit may be smaller and smaller. It dropped below 100 nanometers in 2008 and is now tens of nanometers. This was made possible by the discovery of experiments that semiconductor devices could perform vacuum tube function and advances in semiconductor device manufacturing technology during the 20th century. Integrating small transistors into a small chip is a major improvement in assembling circuits with different electronic components. The production capacity of integrated circuits, their reliability, and the basic design of the circuit led to the rapid adoption of standard integrated circuits instead of different transistor designs. Combined circuits have two main advantages over different circuits: cost and performance. Cheap because the chip is printed-image graphically with all components as a unit, rather than with each transistor. In addition, packaged ICs use much less material than separate circuits. IC components are highly efficient because they change rapidly due to the size and proximity of the components, and use very little energy compared to individual components. As of 2012, the average chip area ranges from a few millimeters to about 450 mm², with transistors up to 9 million per mm².

III. VLSI TECHNOLOGY

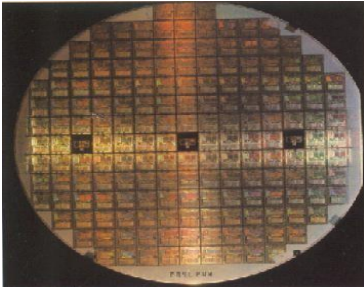
Integrated Circuit (IC): A combination of interconnected circuit elements that are inextricably linked to a continuous substrate.

Substrate: It is the base material on which the IC is fabricated or mounted.

Wafer: A wafer or slice is the basic physical unit used for processing. It usually consists of a large number of nos. Same IC.

Chip: A chip is one of the repeating chips on the wafer. The terms chip and die and desired are used interchangeably.

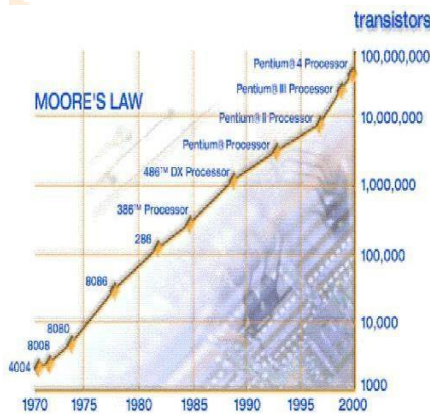
Wafer



5 Moore's Law

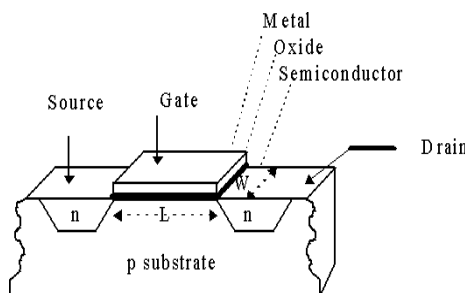
Gordon Moore: co-founder of Intel

As observed by Gordon Moore in 1965, the number of components in the most complex integrated circuit chips will double every year over the next decade. Transistors per Chip Expected to Grow Exponentially (Doubling Every 18 Months) Exponential technological advancement is a natural trend.



Trends in VLSI design

1. Shrinking device geometry
 2. Higher speeds of operation
 3. More logic on the die
-
1. CAD tools
 2. BiCMOS
 3. New methods of device construction



Feature Size

Field Programmable Gate Arrays (FPGA) Typical FPGA Design Flow FPGAs are programmable logic devices:

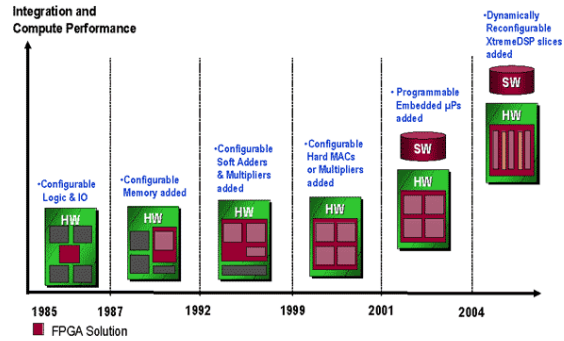
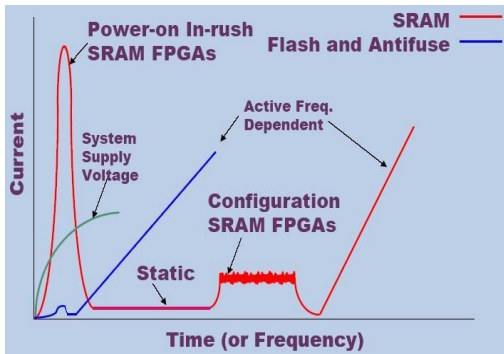
Logic elements + interconnect. FPGAs are standard parts:

Pre-manufactured.

Built for your application. Generally low power consumption. FPGA Fabric Elements

Logic.
Interconnect.
I/O pins table = SRAM used for truth table.

I/O block (IOB): I/O pin + associated logic and electronics. Programmable gate input terminals. Internal function. Particles are coarser than logic gates. There are usually 4 entrances. Registration is usually included. You can provide specialized logic. Adder of the transmission circuit.

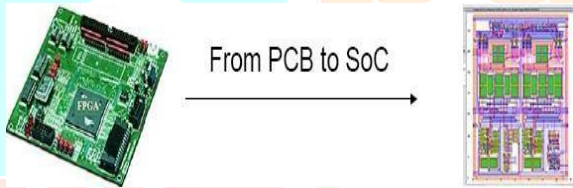


Study on FPGA (various technologies)

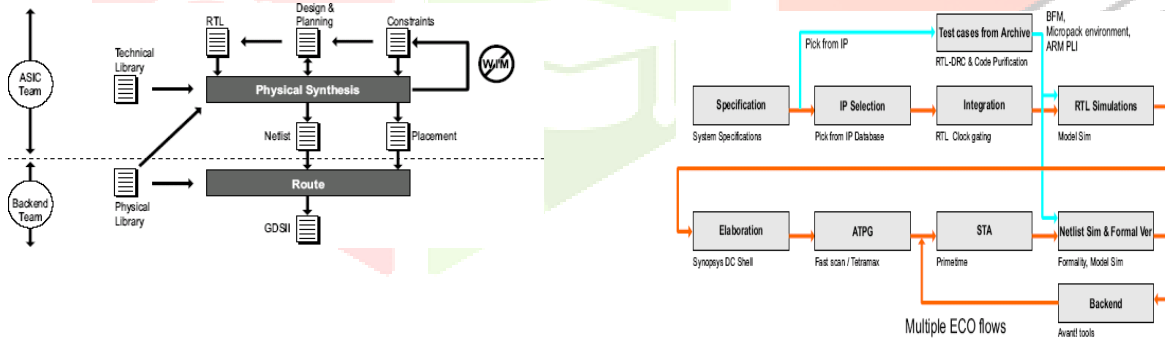
1. Xilinx Series XC3000 Series XC4000 Series Spartan Series Virtex Series
2. Altera Series System On Chip

Technological Achievements:
Microcircuits have millions of transistors. The measured in PCB components can now be integrated into a single chip.

length of the Transistor gate is nanometers.



A Typical SoC Design flow:
Physical design flow in designing System-on-Chip

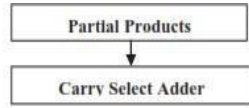


Research
Logic Synthesis
High-speed/Low-Power VLSI Arithmetic
Application Hardware Development [DSP, Encryption, Communication] Low-Power VLSI Design
Quantum Computing/DNA Computing Embedded System Development

IV. EXISTING WORK

PROPOSED WALLACE MULTIPLIER

WALLACE TREE MULTIPLIER USING CSLA



The partial products originating from Group 2 were converted into selective addition for transport. This is because this addition process reduces latency compared to traditional Wallace tree multipliers.

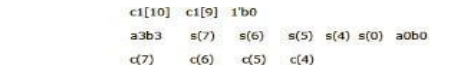
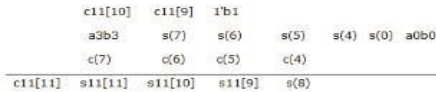
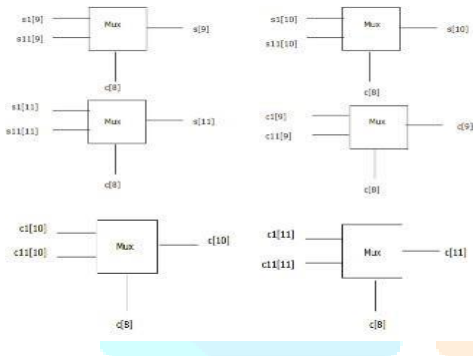


Fig.8. Partitioning and Addition of the Partial Products when input carry is zero



In the next case $c(8)$ as $1'b1$ is assumed to get the result as $a0b0$, $s(0)$, $s(8)$, $s11(9)$, $s11(10)$, $s11(11)$, $c11(11)$.



Depending on the value of carrier bit $c(8)$, a bit is selected from $1'b0$ if it is the required output or $1'b1$ if it is. Output selection using carry bit $c(8)$ is clearly stated below when using a multiplexer.

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	2	4056	0%
Number of 4-input LUTs	4	8512	0%
Number of bonded I/Os	8	232	3%

Wallace tree multiplier using CSLA with BEC

The main reason to use a carry select adder with BEC is to reduce the number. The gate is compared to a typical Wallace multiplier. Case $1'b1$ of generic CSA is replaced by BEC. The result of case $1'b0$ is fed to the input of the adder BEC.

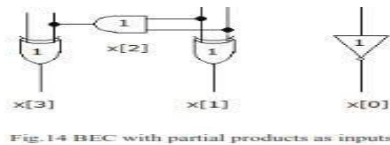
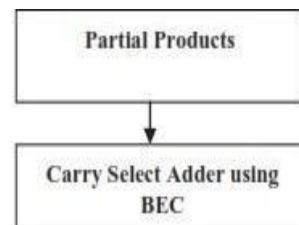
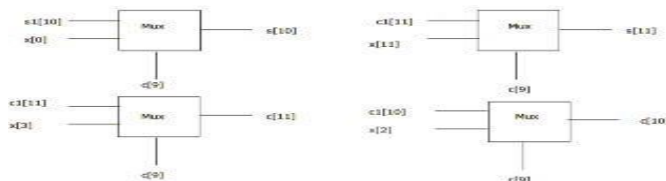


Fig.14 BEC with partial products as inputs



V. RESULTS AND DISCUSSION

Wallace Multiplier is synthesized using XILINX ISE Design Suite 12.2 and is implemented on FPGA device xc3s5005fg320 of Spartan 3E family.

input-output waveforms which are generated by using XILINX software and device utilization summary are shown.

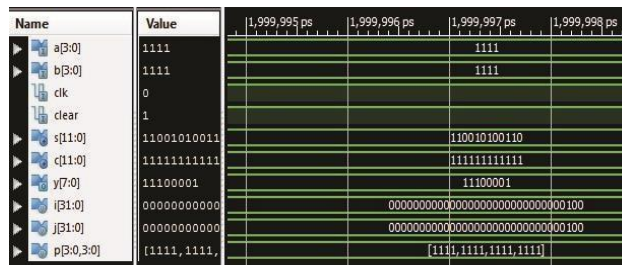


Fig.1 .simulation result for Wallace tree multiplier for 4bit

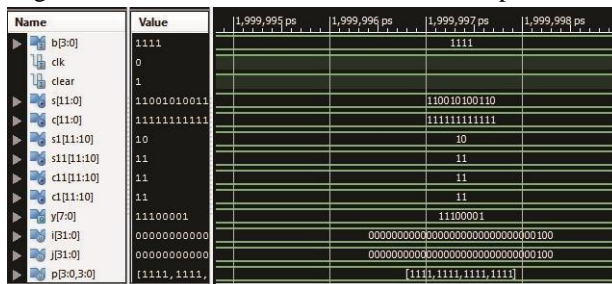


Fig.2. simulation result for Wallace tree multiplier using CSLA

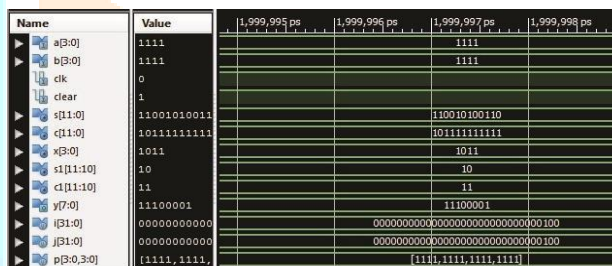


Fig.3. simulation result for Wallace tree multiplier using CSLA with BEC

Parameter	Wallace tree multiplier	Wallace Tree Multiplier using CSLA	Wallace tree multiplier using CSLA with BEC
Memory(KB)	13,7896	13,7768	103448
Delay(ns)	8.486	8.337	8.732
Power(mW)	83.22	82.88	80.98

Table.1. Comparison of Wallace tree multiplier using CSLA and BEC

The few pieces of RCA in the CSLA are two, while the number of pieces in the BEC is two. A total of 4 LUT inputs for RCA in CSLA and 4 for LUT input in 3 BEC. The number of ROBs combined in the RCA in the CSLA is eight and in the case of using the BEC it is six. From this point of view of local parameters, it is clear that the use of space in the Wallace tree multiplier using CSLA with BEC works well in the area.

VI. ACKNOWLEDGMENT

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