Survey on: An Efficient FPGA implementation of sorting network using unary processing for image processing application

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ABSTRACT: Sorting is a common task in a wide range of applications from signal and image processing to switching systems. For applications that require high performance, sorting is often performed in hardware with application-specified integrated circuits or field-programmable gate arrays. Hardware cost and power consumption are the dominant concerns. The usual approach is to wire up a network of compare-and-swap units in a configuration called the Batcher (or bitonic) network. Such networks can readily be pipelined. This paper proposes a novel area-efficient and power-efficient approach to sorting networks, based on "unary processing." In unary processing, numbers are encoded uniformly by a sequence of one value (say 1) followed by a sequence of the other value (say 0) in a stream of 0's and 1's with the value defined by the fraction of 1's in the stream. Synthesis results of complete sorting networks show up to 92% area and power saving compared to the conventional binary implementations.

Keyword: Low cost design, median filtering, sorting networks, stochastic computing

I. INTRODUCTION

SORTING is an important task in applications ranging from data mining to databases to ATM and communication switching to scientific computing, to scheduling, to artificial intelligence and robotics, to image, video and signal processing. For applications that require high performance, sorting is often performed in hardware with application-specified integrated circuits or field-programmable gate arrays. Based on the target applications, the hardware sorting units vary greatly in the way that they are configured. The number of inputs can be as low as nine for some image processing applications (e.g., median filtering) or as high as tens of thousands. Values, integers, or floating-point numbers ranging from 4- to 256-bit precision. Hardware cost and power consumption are the dominant concerns with hardware implementations. The total chip area is limited in many applications. As fabrication technologies continue to scale, keeping chip temperatures low is an important goal since leakage current increases exponentially with temperature.

Power consumption must be kept as low as possible.

Developing low cost, power-efficient hardware-based solutions to sorting is an important goal. The usual approach is to wire up a network of compare and-swap (CAS) units in a configuration called a Batcher (or bitonic) network. Such networks can readily be pipelined. The parallel nature of hardware-based solutions allows them to outperform sequential software-based solutions. The hardware cost and the power consumption depend on the number of CAS blocks and the cost of each CAS block. This paper proposes a novel area-efficient and power efficient approach to sorting networks based on "unary processing." Data are encoded as serial bit streams, with values represented by the fraction of 1's in a stream of 0's and 1's. This is an evolution of prior work on stochastic processing. Our designs inherit the fault tolerance and low-cost design advantages of stochastic processing while producing completely accurate and deterministic results. As with stochastic processing, however, the approach is handicapped in term of latency. A serial representation is exponentially longer than a conventional binary positional representation. To mitigate the long latency issue of unary processing, The approach is different to the work on continuous time mixed-signal designs in the sense that instead of converting data to (from) binary format using costly analog-to-digital (digital-to-analog) converters and processing in binary domain, the data is encoded in time using low-cost analog-to-time converters (ATCs) and processed in unary domain. We represent the data with time encoded pulse signals. The proposed approach is validated with two implementations of an important application of sorting networks: median filtering. Median filtering has been also used as a case study for processing time-encoded values but no result or discussion on the power consumption and energy efficiency of the designs is presented. The synthesis results show up to 92% area and power savings compared to conventional weighted binary implementations.

II. SORTING

A sorting network is a combination of CAS blocks that sorts a set of input data. Each CAS block compares two input values and swaps the values at the output, if required. There are two variants: 1) an "ascending" type and 2) a "descending" type. In a conventional design, each CAS block consists of an M-bit comparator and two M-bit multiplexers, where M is the data width of the inputs.

Sorting networks are fundamentally different from software algorithms for sorting such as quick sort, merge sort, bubble sort, etc. since the order of comparisons is fixed in advance; the order is not data dependent as is the case with software algorithms. The bitonic and odd–even merge sorting networks proposed by Batcher are the two popular configurations of sorting networks. Bitonic sorting have the lowest known latency for hardware-based sorting.

III.   UNARY PROCCESING

Weighted binary radix has been the dominant format for representing numbers in the field of computer engineering since its inception. The representation is compact; however, computing on this representation is relatively complex, since each bit must be weighted according to its position. Also, the representation is very susceptible to noise: a flipped bit can introduce a large error (if it is a significant bit in the representation.)

Clearly, a stochastic representation is much less compact than conventional weighted binary; this translates to high latency. However, complex functions can be computed with remarkably simple logic, e.g., multiplication can be performed using a single AND gate. Also, the representation can tolerate high clock skew timing errors and soft logic errors.
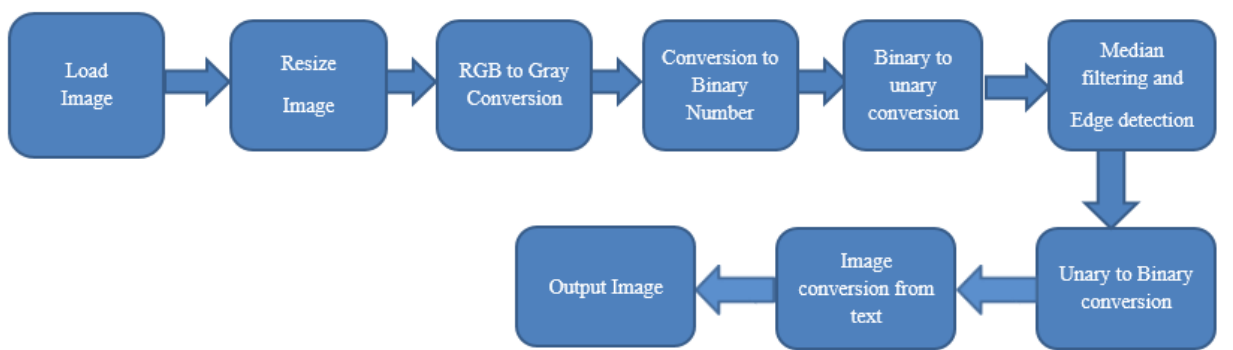

Figure: Block diagram for the Implementation of sorting network using unary processing for image processing application

Architectures consisting of a network of CAS blocks are one of the most common approaches. The incoming data is sorted as it passes the network. The middle element of the sorted data is the median. As the sorting network can be easily pipelined, the approach provides the best performance .The local neighborhood in median filtering is often a 3×3 or 5×5 window with the target input data at the center. 3×3 and a 5×5 median filters, respectively. We developed a nonpipelined and a pipelined structure of these median filters with both the CAS network for a 5×5 median filter made of 246 CAS blocks. conventional binary and the proposed unary design approach with 8-bit input data resolution.. A separate unary stream generator was used for converting each input data and a counter was used for converting the output median stream back to binary form in the unary designs. The overhead in pipelined designs includes pipeline registers and for unary designs include the required converters from/to binary. Similar to the results reported for the complete sort networks, the unary implementation of the median filters significantly improves the hardware cost, up to 90% for the 5×5 median filter architecture. The pipelined implementations have a higher working frequency and a higher throughput. Comparing the power consumption of the pipelined implementations show that, for the same working frequency, the unary designs have a significantly lower power consumption. For applications in which hardware cost and power consumption are the main priorities, the proposed unary

designs out perform.the conventional weighted binary designs. In unary processing, this binary data is first converted to a unary bit stream and then processed using unary circuits. Processing of image pixels with 8-bit resolution requires running the unary circuit for 256 cycles. Even with a higher working frequency, due to a large number of clock cycles running the circuit, the total latency of the processing using unary circuit is more than that of processing with the binary design.

IV.   LITERATURE SURVEY

[1] M. Hassan Najafi, David J. Lilja, Marc Riedel and Kia Bazargan (2017), "Power and Area Efficient Sorting Networks using Unary Processing", in IEEE 35th International Conference on Computer Design

The proposed system is CED scheme by which all errors caused by single faults in a concurrent checking sorting network can be detected. This scheme is the first one available to use significantly less hardware overhead than duplication without compromising throughput. From this scheme, we develop another fault detection scheme which sharply reduces the hardware overhead. A scheme for constructing concurrent checking sorting network (using MCSUls) is the first one available which detects all single non redundant faults with no throughput degradation and at the same time uses much less hardware overhead than duplication. Based on this technique, also developed another scheme which uses significantly less hardware overhead (10% - 30%) but still achieves nearly 100% fault coverage.

[2]   Ren Chen and Viktor K. Prasanna (2016), "Computer Generation of High Throughput Memory Efficient Sorting Designs on FPGA", in IEEE Transactions on parallel and Systems

In this work, system presented a hardware generator which automatically produces bitonic sorting architectures on FPGA. The proposed several optimizations incorporated into our hardware generator. The proposed hardware generator can be used to generate high performance designs with regarding to latency, throughput and energy efficiency accurate performance model for energy-efficiency estimation, which can be used for design space exploration to obtain power optimized sorting architectures with various constraints.

[3] Chaitali Chakrabarti, "Sorting Network Based Architectures for Median Filters", in IEEE Transactions on Circuits and Sytems

Sorting network based architectures for computing nonrecursive and recursive median filters   are presented. The proposed architectures are highly pipelined and consist of fewer compare-swap units than existing architectures. The reduction in the number of compare-swap units is achieved by minimizing computational overlap between successive outputs and also by using Batcher's odd-even merge sort (instead of bubble-sort).

[4] Colavita, A. Cicuttin, F. Fratnik, and G. Capello,"A VLSI Implementation of a Hardware Algorithm for Continuous Data Sorting A. A", in IEEE journal of solid-State circuits

The paper present a VLSI implementation of a hardware sorting algorithm for continuous data sorting. The device is able to continuously process an input data stream while producing a sorted output data stream. At each clock cycle, the device reads and processes a 48-bit word, 24 bits for the datum and 24 bits for the associated tag. The data stream is sorted according to the tags preserving the order of words with identical tags. Sequences up to 256 words are completely sorted and longer sequences are partially sorted.

[5] Kathy J. Liszka and Kenneth E,"A Generalized bitonic sorting network", in International Conference on Parallel processing

The bitonic sorting network will sort N-2m keys in O(log2 N) time with 0(Nlog2 N) comparators. Developments on the sorter enable the network to sort N--pq keys, a composite number. However, there has been no general method for sorting a bitonic sequence of N keys, N a prime, or N a composite that decomposes into primes larger than 3. The odd merge method removes this constraint while maintaining the same cost and delay, using a uniform and efficient decomposition.

[6] C.F. Chuah and T. Nandha Kumar (2020)," Fast and exact multiple-input unary-to-binary multiplier with variable precision for stochastic computing", in International Conference on Parallel processing

Stochastic computing offers an area-efficient solution for power-greedy computations in error-resilient applications such as image processing. However, stochastic computing produces only approximated results and suffers from long latency especially for multiplication. multiplier design technique for stochastic computing which guarantees exact output and has latency in the order of 2N (N = input precision), utilizing the counter for unary- to-binary conversion.

[7] McKenzie van der Hagen and Marc Riedel(2003),:" Unary Positional Computing", in IEEE Conference on signal and information processing

This paper introduces a novel representation that is a hybrid of unary and positional Systems. In contrast to the stochastic approach, the unary approach is completely accurate, with no random fluctuations. It requires less area and has much lower latency. However, compared to a conventional binary approach. The unary positional system proposed in this paper reduces the latency exponentially, with only a modest increase in the hardware complexity.

[8] Ghassan Mahmoud husien Amer, Dr. Ahmed Mohamed Abushaala(2014), " Edge Detection Methods in IEEE Conference on Very Large Scale Integrated circuits

This paper presents various edge detection methods**.** Edge detection is a type of image segmentation techniques which determines the presence of an edge or line in an image and outlines them in an appropriate way. The main purpose of edge detection is to simplify the image data in order to minimize the amount of data to be processed. paper present methods for edge segmentation of images; we used five techniques for this category; Sobel operator technique, Prewitt technique, Laplacian technique, Canny technique, Roberts technique, and they are compared with one another so as to choose the best technique for edge detection segment image. These techniques applied on one image to choose base guesses for segmentation or edge detection image.

V.   CONCLUSION

Data Confidentiality as well as integrity has been affected by eavesdropping and unauthorizedaccessing of information transmitted through the internet. That arise the need for informationsecurity. So the security is getting the major attention due to the increased use of internet. Asthe use of internet is increased, the rate at which the data is exchanged per day is also increased.The data that is exchanged every day may become the victim of hackers. To deal with this problem one of the effective solution is the Steganography. In this paper we have presented areview of some different video steganography techniques to deal with three big challenges ofsteganography that is imperceptibility, robustness and capacity to provide enhanced security for data hiding. And also results are evaluated based on parameters, PSNR and MSE.

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3. Biswajita Datta, "Robust High Capacity Audio Steganography using Modulo Operator",Computer, Communication, Control and Information Technology (C3IT), 2015 Third International Conference on 7-8 Feb. 2015.

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