OPEN AND CLOSED LOOP ANALYSIS OF BASIC SEPIC CONVERTER

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Abstract : This paper presents the Open loop & Closed loop analysis of SEPIC converter with coupled inductors which operates in Continuous Conduction Mode(CCM). This converter provides the needed, input to output gain and also can both step up and step down the input voltage, while maintaining the same polarity and same ground reference for the input and output. This proposed converter is similar to the traditional Buck-Boost converter but has an advantage of having non-inverted output. It has the same voltage polarity as that of input, by using a series capacitor to couple the energy from input to output. As the switching frequency increases the minimum size of the inductor to produce continuous current and minimum size of the capacitor to limit the output ripple both decreases. In this paper SEPIC converter is operated at a switching frequency of 25 kHz under Continuous Conduction Mode(CCM). Simulation has been carried out in MATLAB/Simulink software and hardware is implemented and the corresponding results are presented.

I. INTRODUCTION

Single Ended Primary Inductance Converter(SEPIC) is a DC to DC converter which allows the output voltage to be greater than or lesser than or equal to its input. The output of the SEPIC converter is controlled by the duty cycle of the control switch. A SEPIC converter is essentially a boost converter followed by buck-boost converter which has advantages of having non-inverted output, using a series capacitor to couple energy from the input to the output. SEPIC converter has the resists of having non-inverting polarity, easy to drive the switch & low input current pulsating for high precise switching. SEPIC converters are useful in applications in which the battery voltage can be above & below that of regulators intended output. Coupled inductor in the SEPIC converter requires half the inductance when compared to two separate inductors.
To derive the relationship between input & output voltage's following initial assumptions are to be made:

- Both inductors are very large & the current's flowing through them are constant.
- Both capacitors are very large & voltage across them are constant.
- The circuit is operating in a steady state where the voltage & current waveforms are periodic.
- For a duty ratio of "D", the switch is closed for "DT" time & open for "(1-D)T" time.
- The switch & the diode in the converter circuit are ideal.

II. PROPOSED SEPIC CONVERTER STRUCTURE

THE BELOW SHOWN FIGURE IS A SIMPLE CIRCUIT DIAGRAM OF SEPIC CONVERTER, CONSISTING OF COUPLED INDUCTORS LS & LP, COUPLING CAPACITORS CS & CP, A POWER MOSFET SX, AND A DIODE DX. FOR A DUTY RATIO OF *D*, THE SWITCH IS TURNED-ON FOR TIME *DT* AND TURNED-OFF FOR (1-*D*)*T*. THE INDUCTOR CURRENTS ARE ASSUMED TO BE CONTINUOUS FOR THIS ANALYSIS. OTHER ASSUMPTIONS ARE THAT, THE AVERAGE INDUCTOR VOLTAGES ARE ZERO AND THAT THE AVERAGE CAPACITOR CURRENTS ARE ZERO FOR STEADY-STATE OPERATION.

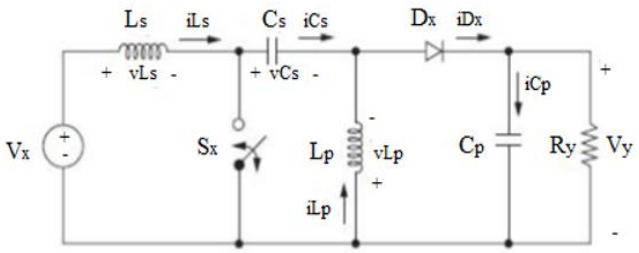

Fig.1 Proposed SEPIC converter schematic diagram.

This converter operates in two modes namely mode-1 in the time interval DT when switch is turned-on and mode-2 in the interval (1-*D*)T when switch is turned-off.

Mode 1 [Fig.2 (0< t < DT)] : When the switch is closed, the diode is off and capacitor supplies the power to load connected across the output terminal .The voltage across inductor Ls for the interval *DT* is given by,

$$VLs = Vx \qquad (2\text{-}1)$$

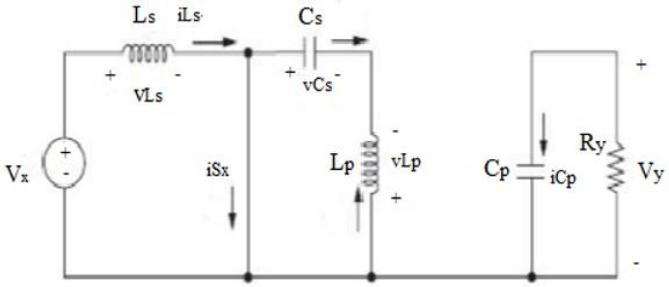

Fig.2 SEPIC Circuit with the switch closed

Mode 2 [Fig.3 (DT<t< (1-D)T)]: When the switch is open, the diode is on, and the circuit is as shown in Fig.3

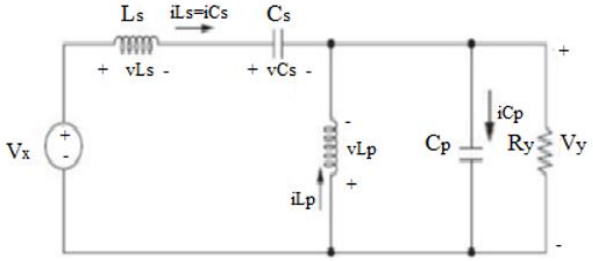

Fig.3 SEPIC Circuit with the switch open

On applying Kirchhoff's Voltage Law around the outermost path gives,

$$-Vx + VLs + VCs + Vy = 0 \qquad (2\text{-}2)$$

Assuming that the voltage across capacitor *C*s remains constant at its average value of Vx ,

$$-Vx + VLs + Vx + Vy = 0 \qquad (2\text{-}3)$$

$$VLs = -Vy \qquad (2\text{-}4)$$

Since the average voltage across the inductor is zero for periodic operation, equations (2-1) and (2-4) are combined to get,

$$Vx\,(DT) + Vy\,(1\text{-}D)\,T = 0 \qquad (2\text{-}5)$$

The output voltage is expressed as,

$$Vy = Vx \frac{D}{(1-D)} \qquad (2.6)$$

This result is similar to buck-boost and CUK converter equations, with no polarity reversal between input and output voltages. The ability to have an output voltage greater or less than the input without polarity reversal makes this converter suitable for many applications.

Expected waveforms of SEPIC converter is

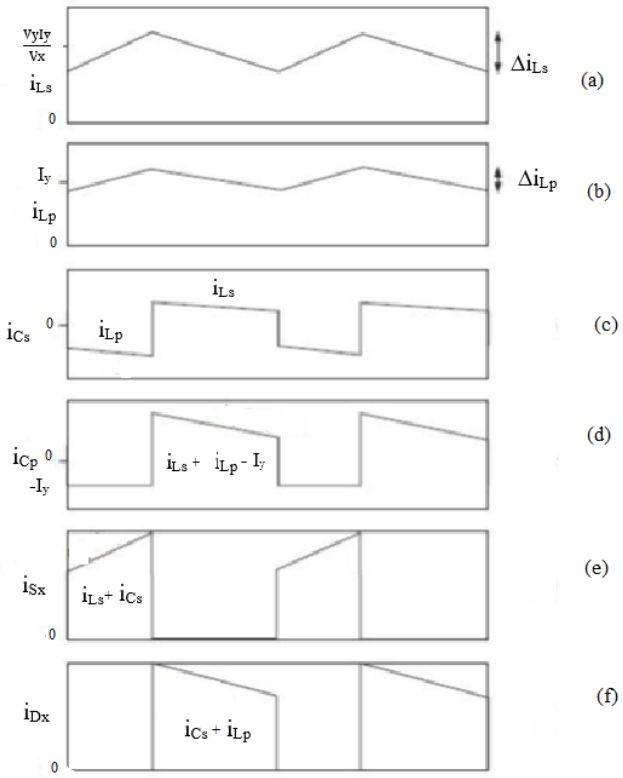

Fig.4 a. Current through Inductor Ls (iLs), b. Current through Inductor Lp (iLp), c. Current through Capacitor Cs (iCs), d. Current through Capacitor Cp (iCp), e. Current through switch Sx (iSx), f. Current through diode Dx (iDx).

III. Designing of Inductor and Capacitor Value

For continuous current in the inductors, the average current must be greater than one-half the change in current. Minimum inductor sizes for continuous current are

$$L_{smin} = L_{pmin} = \frac{(1-D)^2}{D} \cdot \frac{Ry}{2f} \qquad (3\text{-}1)$$

In this proposed work the inductance value is taken as 1.25 times of the minimum inductor value so

$$L_s = L_p = 1.25 * L_{smin} \qquad (3\text{-}2)$$

The capacitor value can be determined using the following formula by considering the minimum ripple voltage

$$C_s = C_p = \frac{D}{Ry\left(\frac{\Delta V0}{Vo}\right)f} \qquad (3\text{-}3)$$

IV. Simulation Results

Simulation is carried out in MATLAB/SIMULINK with the design parameters from table 1, the simulated results are as follows.

Table 1: Design Parameters

Parameters	Values
Input voltage, V_x	16v
Output voltage, V_y	24v
Duty ratio , D_x	60%
Resistance ,R_y	20Ω
Switching frequency , fs	25kHZ
Inductor, $L_s = L_p$	133µH
Capacitor, $C_s = C_p$	120µF

Fig. below represents the open loop simulation of the SEPIC converter

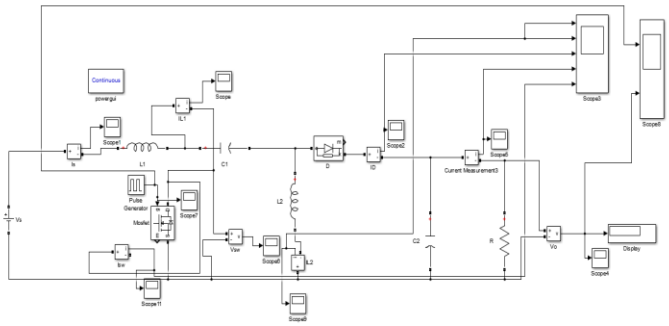

Fig.6 Simulation of open loop SEPIC converter

Fig. below represents the closed loop simulation of the SEPIC converter. In the proposed circuit, PI Controller is used to improve the output and provide stability to the system.

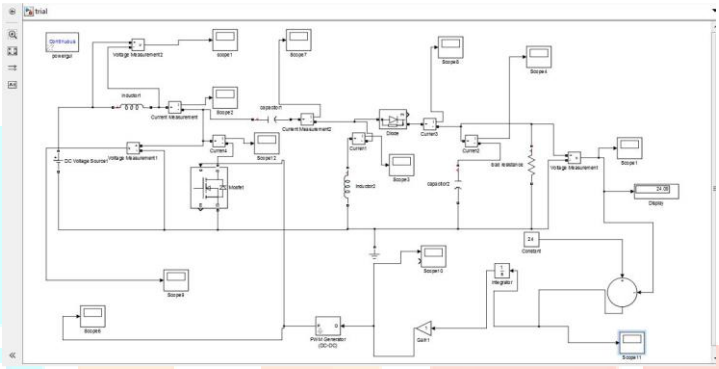

Fig.7 Simulation of closed loop SEPIC converter

Fig. shown below represents the current flowing through and the voltage across inductors, switch and diode.

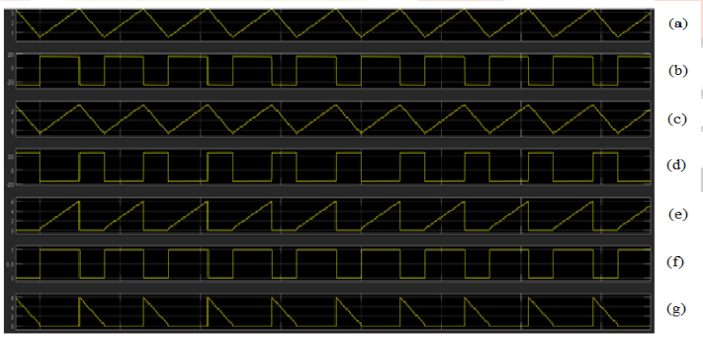

Fig.8 a. Current through Inductor Ls (iLs), b. Voltage across Inductor Ls (vLs), c. Current through Inductor Lp (iLp), d. Voltage across Inductor Lp (vLp), e. Current through switch Sx (iSx), f. Voltage across switch Sx vSx, g. Current through diode Dx (iDx).

Fig. below represents the output voltage waveform of the proposed SEPIC converter with respect to time versus output voltage.

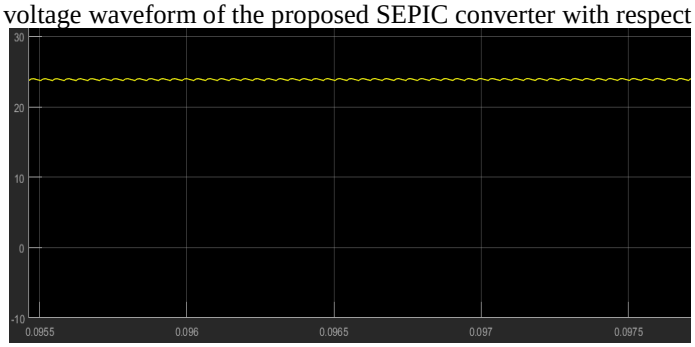

Fig.9 Output voltage

V. EXPERIMENTAL RESULTS

All the required parameter values for hardware setup are listed in table 1. Fig. below represents the hardware setup of closed loop SEPIC converter.

Fig.10 Hardware setup of SEPIC converter for closed loop system

Fig. below represents the open loop output voltage appearing across the load for the proposed SEPIC converter.

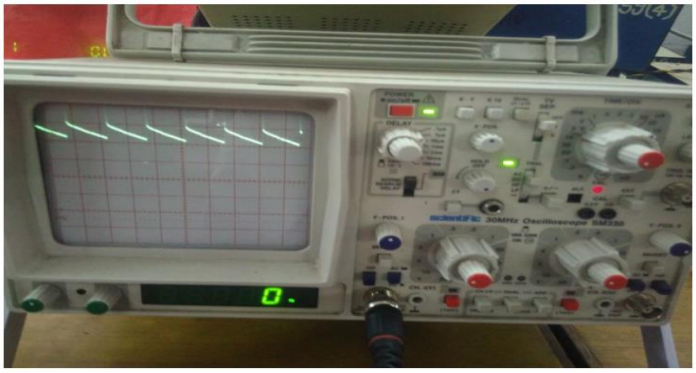

Fig.11 Open loop Output voltage vs time

Fig. below represents the closed loop output voltage appearing across the load for the proposed SEPIC converter.

Fig.12 Closed loop output voltage v/s time

VI. CONCLUSION

The open loop & closed loop analysis of SEPIC converter is presented. The advantage of this proposed converter is that the output voltage is of same polarity with respect to the input. Therefore the hardware cost of the proposed converter is lower compared with other converters for the same output. The obtained result has effectively proved that the output is invariably dependent on the duty cycle of the switch. As the duty cycle is varied buck and boost operation is performed.

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