VLSI ARCHITECTURE FOR CONTRAST ENHANCEMENT USING PIXEL BASED IMAGE FUSION

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Abstract : In the past few years, image fusion has become a very popular field in the area of image processing. Due to the fast entrance of digital imaging into the remote sensing and satellite applications, there is often a need to store large amount of image data and process it very quickly. The standard fusion methods perform well spatially but introduce spatial distortions. So to overcome this problem we focus on the most powerful tool for image processing i.e. DWT. In this paper we use an efficient DWT based image fusion by using lifting based scheme. For the processing of high resolution (HD & UHD) images requires high complexity systems and consumes larger time, to avoid such latency we use hardware processing. The VLSI architecture for contrast enhancement using pixel based image fusion is designed for the low contrast source images and is simulated using VERILOG hardware description language.

Index terms: Image Fusion, Discrete Wavelet Transform (DWT), 2-D DWT, lifting based DWT, VLSI Architecture, contrast enhancement, strip-based scanning, Gamma Correction, lifting based IDWT, 2-D IDWT.

I.INTRODUCTION

Image Fusion with multiple image sources has now a day's been very popular in many fields such as medical imaging, computer vision, paintings, remote sensing, and in many applications. The human visual system can identify various edges, colors, contrast etc. in an image, but some devices are now with limited set of colors and not pleasing to human eyes. So to get an image with sharp and crisp, image fusion technique is used in which two or more images are combined to get an image with more details from the same source images. The implementation of VLSI architecture for efficient 2-D DWT and inverse 2-DWT processor is required, that consumes less area, memory efficient and should operate with a high frequency to use in real-time applications. The implementation of lifting based scheme (DWT) requires less arithmetic complex, less memory and can be implement in parallel. Huang et al.,[7] introduced a flipping structure which provides a critical path of Tm+Ta. Now there is a requirement to improve memory efficiency. Various parallel architectures were proposed for lifting based 2-D DWT. Y.Hu et al.,[5] proposed a modified strip based scanning and parallel architecture for 2-D DWT. The on-chip memory for this is 3N+24P of image with P parallel Processing Units (PU). The architecture designed for 2-D IDWT is similar to that of 2-D DWT but the operation takes place in reverse direction.

II. DESIGN OF ARCHITECTURE

The design of the proposed architecture for the contrast enhancement of the fused image obtained by pixel based image fusion in wavelet domain is shown as below in Fig.1.
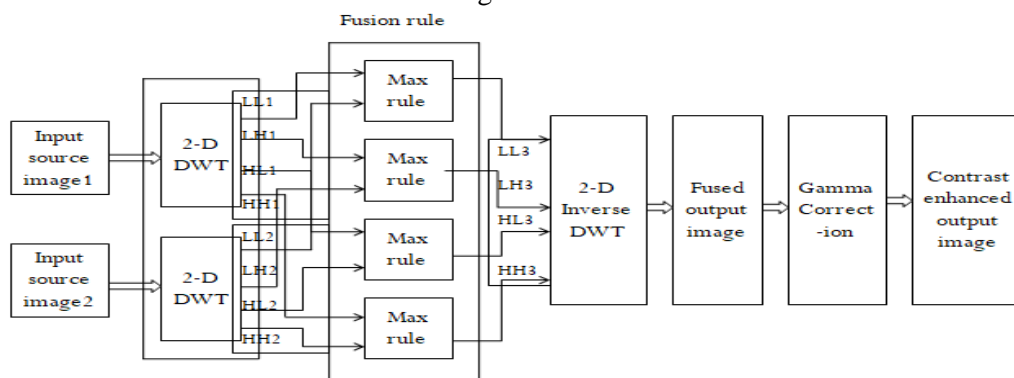

Fig.1. Block diagram for design of architecture for contrast enhancement of fused image.

2.1 Proposed architecture for 2-D DWT and 2-D inverse DWT:

2-D DWT: The architecture consists of two parallel spatial processors (2-D DWT) i.e., P=2 for which each processor takes a source image (low contrast image) of same type each. The input frames applied to the 2-D DWT modules gives the 4 sub-bands of outputs each i.e. LL1, HL1, LH1, HH1, LL2, HL2, LH2, and HH2 respectively. These results are given for maximum fusion rule module. The output results of 2-D IDWT are LL3, HL3, LH3, and HH3.

A. Architecture for spatial processor:

   The architecture of 2-D DWT is a memory efficient lifting based 2-D DWT spatial processor which consists of a row and column processors. Y.Hu et al.[5] proposed an architecture which utilizes strip-based scanning to enable the trade-off between external and internal memory. Flipping model is used for the processing element (PE). The processing unit (PU) is designed which is having five PEs. The proposed architecture performs the lifting based (9/7) 1-D DWT process by PU. The PU which is modified has a CPD to *Ta* (adder delay). The width of the strip is equal to the number of inputs to the spatial processor i.e. 2P+1. The PUs with different pipeline stages is shown in Fig.2. The proposed architecture consists of two parallel processing units (PUs) i.e. P = 2. When the internal results of the row processor are obtained then the column processor starts to process on those intermediate results.

1)   Row processor (RP): For the strip-based scanning the image is of size *N✗N* is extended to *N✗ (N+1)* by one column by symmetric extension. The strip based scanning on DWT takes place in row wise through row processor (RP) as well as column wise through the column processor (CP). In this design we consider P=2. The pixels come from *X (0, 0)* to *X (0,2P)* simultaneously for the first clock cycle.

Then it goes for the next strip i.e. pixels from *X (0,2P)* to *X (0,4P)* of the next row are taken and the same procedure continues for the whole image. From the eqn. (1) PE_alpha of PU-1 provides the output *H1[n]* along with produces partial results *X'[2n]* that is required for PE_beta. To reduce CPD the pipeline stages are increased to giving CPD as *Ta*, where the results are stored in the memories Memory_alpha, Memory_beta and Memory_gama respectively. The process of scaling is taken place for each PU and then outputs of these are fed to the transposing unit.

2) Column processor (CP): In our architecture we design the CP with two number of PUs to match with the throughput of RP. Pair of H and L is produced by transpose register in an alternative order and are fed to the CP as inputs of one PU. Four sub-bands are generated at the output of CP in an interleaved pattern. The outputs obtained from CP are given to the re-arrange unit, thus giving outputs in sub-band order i.e., *LL, LH, HL, HH* simultaneously.

The design equations of 2-D DWT are as shown below

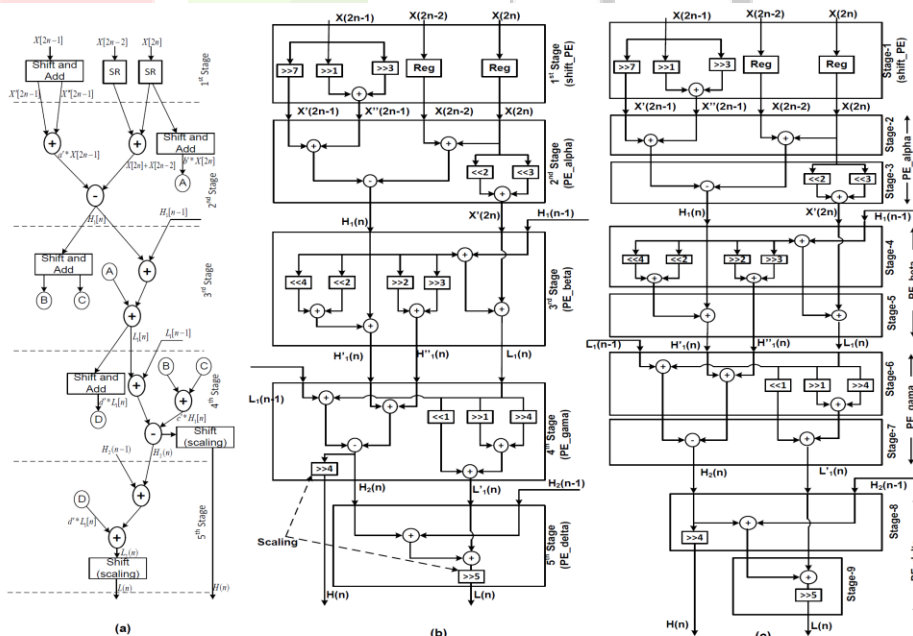$$H_1[n] \leftarrow a' * X[2n-1] + \{X[2n] + X[2n-2]\}............\text{P1} \qquad (1)$$

Fig.2. (a) Data flow graph of processing unit (b) Processing unit with five pipeline stages (c) Processing unit with nine pipeline stages.

$$L_1[n] \leftarrow b' * X[2n] + \{H_1[n] + H_1[n-1]\} \ldots\ldots\ldots\text{U1} \qquad (2)$$

$$H_2[n] \leftarrow c' * H_1[n] + \{L_1[n] + L_1[n-1]\} \ldots\ldots\ldots\text{P2} \qquad (3)$$

$$L_2[n] \leftarrow d' * L_1[n] + \{H_2[n] + H_2[n-1]\} \ldots\ldots\ldots\text{U2} \qquad (4)$$

$$H[n] \leftarrow K0 * \{H_2[n]\} \qquad\qquad\qquad\qquad (5)$$

$$L[n] \leftarrow K1 * \{L_2[n]\} \qquad\qquad\qquad\qquad (6)$$

Where $a'=1/\alpha$, $b'=1/\alpha\beta$, $c'=1/\beta\gamma$, $d'=1/\gamma\delta$, $K0=\alpha\gamma\delta\zeta$ and $K1=\alpha\beta\gamma\delta\zeta$. The lifting and the scaling coefficients are $\alpha,\beta,\gamma,\delta$ and ζ respectively. Its values are $\alpha = -1.586134342$, $\beta = -0.052980118$, $\gamma = 0.08829110762$, $\delta = 0.4435068522$, and $\zeta = 1.149604398$.

2-D Inverse DWT: The architecture designed for 2-D Inverse DWT is similar to that of 2-D DWT but the operation takes place in reverse direction. The 2-D IDWT requires an on-chip memory of 4N+86 words for a single level decomposition. The 2-D IDWT processing starts firstly column wise and then through the row wise.

A. Architecture for spatial processor (SP):

Flipping model here is used to reduce the longest path delay into shorter critical path. The PU architecture reduces the CPD to Ta (adder delay). The outputs that are obtained from the row processor are the pixels that belong to the reconstructed image. These output pixels are stored in the external memory. The 2-D IDWT utilizes pipeline structure with different stages. Huang et al. [7] Modified equations for flipping based IDWT. They are as shown below:

$$\left.\begin{aligned}\delta' L(n) &= 1.9843 L(n) \\ \delta'' L(n) &= 0.2812 L(n)\end{aligned}\right\} \quad \text{1}^{\text{st}}\text{ stage} \quad (7)$$

$$\left.\begin{aligned}L'(n) &= \big(\delta' L(n) - \delta'' L(n)\big) - \big(H(n) + H(n-1)\big) \\ \gamma' H(n) &= 0.0625 H(n) \\ \gamma'' H(n) &= 2.5 H(n)\end{aligned}\right\} \quad \text{2}^{\text{nd}}\text{ stage} \quad (8)$$

$$\left.\begin{aligned}H'(n) &= \big(\gamma' H(n) + \gamma'' H(n)\big) - \big(L'(n) + L'(n-1)\big) \\ \beta' L(n) &= 10.625 L'(n) \\ \beta'' L(n) &= 32 L'(n)\end{aligned}\right\} \quad \text{3}^{\text{rd}}\text{ stage} \quad (9)$$

$$\left.\begin{aligned}X'(2n) &= \big(\beta' L(n) - \beta'' L(n)\big) - \big(H'(n) + H'(n-1)\big) \\ \alpha H'(n) &= 12 H'(n)\end{aligned}\right\} \quad \text{4}^{\text{th}}\text{ stage} \quad (10)$$

$$\left.\begin{aligned}X(2n) &= -0.0234 X'(2n) \\ X(2n-1) &= 0.03125\big(\alpha H'(n) - (X'(2n) + X'(2n-1))\big)\end{aligned}\right\} \quad \text{5}^{\text{th}}\text{ stage} \quad (11)$$
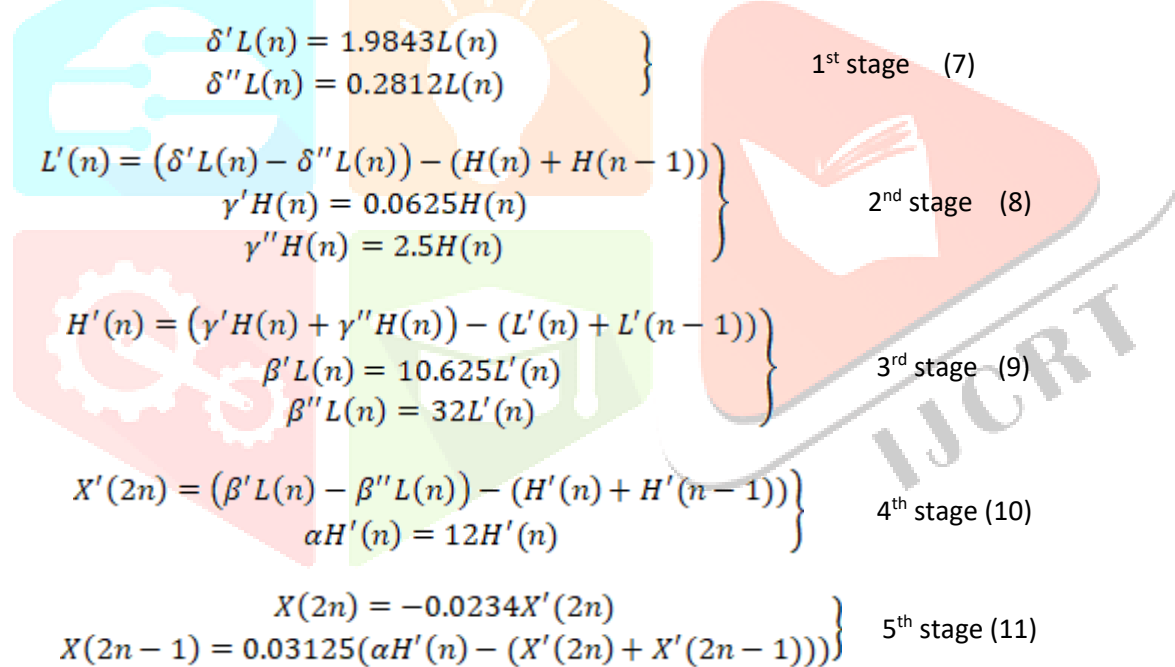
1. Column Processor: The column processor is designed with two Processing Units (PUs). It receives the 2-D DWT output coefficients (LL, LH, HL, and HH sub-bands) as inputs. It takes the inputs for the first clock cycle from LL(n,m), LH(n,m), HL(n,m), HH(n,m) simultaneously and the same procedure continues for each clock cycle until the bottom row. The PU of this consists of five pipeline stages and each pipeline stage is processed by the processing element (PE) i.e. PE_shift, PE_invdelta, PE_invgama, PE_invbeta, PE_alpha as shown in the Fig.3(a).

2. Row processor: The generalized structure for row processor is as shown in Fig.3(b). For each clock cycle the CP sends the inputs to the RP from XL(n-1,m) and XL(n,m) from low frequency sub-band and XH(n-1,m) and XH(n,m) from high frequency sub-band. The intermediate results that are obtained when input from CP XH (n-1, m) are sent i.e. (XL' (n-1, m), XH' (n-1, m), and X' (n-1, 2m)) belonging to PE_invgama, PE_invbeta, PE_invalpha of PU 1 stores in the memories i.e. Mem_delta1, Mem_invgama1, Mem_invbeta1, Mem_invdelta, Mem_invalpha1 respectively. Similarly for the other inputs of PU2 the same procedure takes place.

Image fusion: The resulting outputs of 2-D IDWT are now applied for the inverse 2-D DWT module for the reconstruction of the final fused image. For contrast enhancement the gamma correction (γ) is applied for the final fused image.
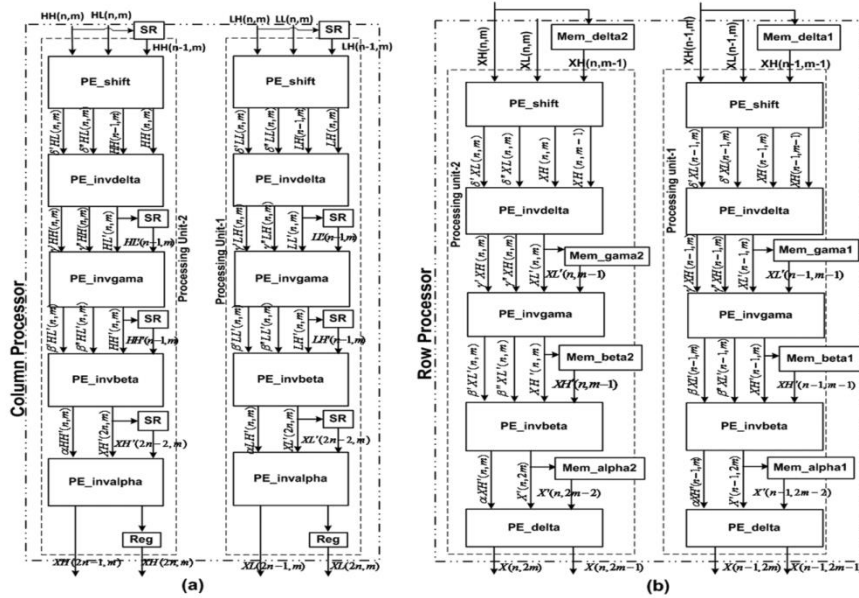
Fig.3. (a) Structure of column processor (b) structure of row processor.

III. IMPLEMENTATION RESULTS:

Two low contrast source images are taken and DWT based image fusion is applied. The contrast enhancement of the final fused image is obtained for different gamma correction values.

Table 1 VLSI architecture implementation results.

Input source image1	Input source image 2	Fused output image	Gamma(γ) corrected image
GEC Building:			
LENA:			
PLANES:			

IV. COMPARISON TABLES:

Table 2 Comparison of proposed 2-D DWT architecture with existing architectures:

Parameters	Zhang	Mohanty	Darji	Yusong	Proposed
Multipliers	10	9P	10	10P	0
Adders	16	16P	16	16P	34P
Internal memory	4N+37	15P+5.5N	4N	24P+3N	60P+3N
Critical path delay	T_m	$T_m + 2T_a$	T_m	T_m+T_a	T_a
Computation time	$N^2/2$	$N^2/2P$	$N^2/2$	$N^2/2P$	$N^2/2P$
Throughput	$2/T_m$	$2P/T_m+2T_a$	$2/T_m$	$2P/T_m+T_a$	$2P/T_a$

Table 3 Comparison of proposed 2-D inverse DWT architectures with existing architectures:

Parameters	Darji	P.K.Nath	Proposed
Memory requirement	4N+5 registers	5N	4N+86 registers
Throughput/cycle	2	2	4
Compution time	$N^2/2+N+3$	$N^2/2+2.5N+26$	$N^2/4+18$
Multipliers	10	Nil	Nil
Critical path delay	T_m	T_a	T_a
Adders	16	58	76

V. CONCLUSION:

Specialized hardware results in improvement of speed and with less complexity. Its architecture operates at 186.03 MHz frequency and it uses 734 slice LUTs for 2-D DWT and similarly 2-D inverse DWT uses 3462 slice LUTs at 209.102MHz frequency. The 2-D DWT and 2-D inverse IDWT spatial processors used in this architecture is efficient than the other existing architectures. It reduces internal memory, latency, critical path delay and complexity of the control unit.

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