TWO STAGE OPERATIONAL AMPLIFIER USING 90nm TECHNOLOGY

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Abstract— The design of high gain and power of analog components can be designed by using fully differential circuit concepts with the help of Operational Amplifiers (Op-Amps). The Op-Amp can be designed by providing the amplification of input voltages at two stages. The two stage Op-Amp features can be improved by providing the concepts like CS Amplifier , cascade etc. The Op-Amp design for high speed applications requires proper selection of biasing, logic style, and CS Amplifier as the technology is scaling down. This basic Op-Amp performance metrics can be improved by adding the CS Amplifier. The Op-Amps are designed for both with single operational amplifier and CS Amplifier with gain improvement using Cadence full custom design suite for 90nm technology.

Keywords— Single Stage Op-Amp, CS Amplifier, Mirror Pole , PMOS & NMOS of 90nm Technology.

I. INTRODUCTION

The design of high gain analog components can be designed by using fully differential circuit concepts with the help of Operational Amplifiers (Op-Amps).The Operational Amplifiers (Op amps) are one of the most widely used building blocks for analog and mixed signal systems. They are employed from dc bias applications to high speed amplifiers and filters. General purpose op amps can be used as buffers, summers, integrators, differentiators, comparators, negative impedance converters, and many other applications. While many digital circuits can be adapted to a smaller device level with a smaller power supply, most existing analog circuitry requires considerable change or even a redesign to meet the same constraints. With transistor length being scaled down to a few tens of nanometers, analog circuits are becoming increasingly more difficult to improve upon. The basic two stage Op-Amp can be designed by using MOS technology to meet the features and constraints. The basic Op-Amp features are gain, gain bandwidth, Slew rate, Common-Mode Rejection Ratio (CMRR), Power Supply, output-voltage swing, output resistance, offset etc. The open loop gain of Op-Amp for a particular technology cannot match with the bipolar based Op-Amps. This is due to small trans conductance of this devices as well as the gain reduction due to short channel effects that come into play for submicron processes. As a result, gain boosting schemes must be used to improve the gain. These gain enhancing methods often require more complicated circuit structures and higher power supply voltage, and may produce a limited output voltage swing. Hence multiple stage amplifiers may be used for higher gain analog circuit designs. But the multistage amplifiers generally are difficult to construct. However, most methods require more circuit area and more complex design than the dominant pole approach used in the classic op amp architecture. Special problems of integrated circuit amplifiers which include lack of large sized capacitors, parasitic coupling, and package parasitic and on/off chip load problems make the constructing more difficult than discrete component amplifiers. The main aim of this work is to design two stage op amp with CS Amplifier to improve the gain using 90nm technology and cadence full custom design suite. This paper is organized such that the section II gives general background and information of Op-Amp basic theory. The section III describes the design specifications, requirements and design methodology. The chapter IV gives the details of full custom design of op amp using Cadence tools and also describes the simulation results to demonstrate the functional verification and performance improvements. The conclusion is presented in section V followed by references.

II. BASIC THEORY OF OP-AMP

The Op Amp (Operational Amplifier) is a high gain, dc coupled amplifier designed to be used with negative feedback to precisely define a closed loop transfer function. The gain produced by the op amp is higher than the gain produced by normal amplifiers. Thus it is a high gain amplifier. The basic symbol of Op-Amp is shown in Figure1.The op amp symbol has two input terminals, one is positive terminal and other is negative terminal, voltage supplies to op amp as +VDD , –VSS and one output terminal.

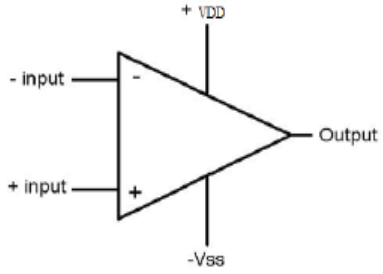


Figure 1: Symbol of Op-amp

The basic block diagram of op-amp is shown in Figure 2.

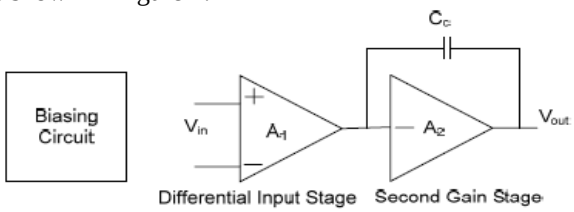


Figure 2: Block diagram of op-amp

The op-amps can be designed by using either two stage topology or folded cascade topology by modifying the stage 1.stage-2 or at any portion of the basic op-amp topology. The selection of the topology is based on the required non functional parameters and features of op-amp.

III. DESIGN OF OP-AMP

The design of two stage op-amp can be done by using the following steps .
Step-1: Selection of the transistor logic style or logic family.
Step-2: Basic structure for the op-amp from the selected
Logic family.
Step-3: Selection of transistor in 90nm technology .
Step-4: Physical verification.

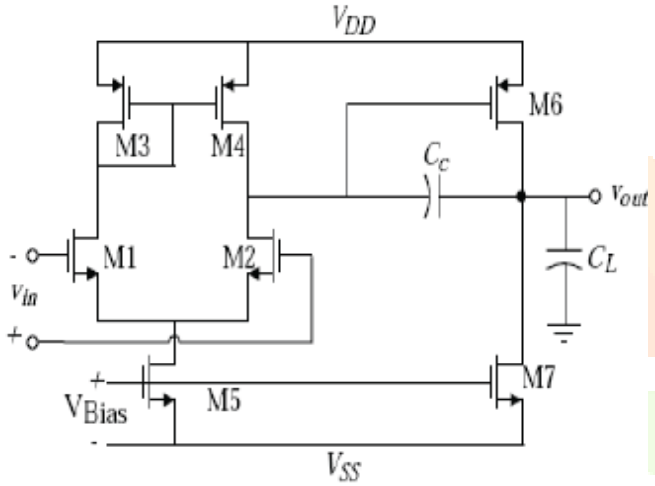


Figure-3 Two stage operational Amplifier

The input is a differential one for the current source, Transistors M5 and M7 are biasing transistors that ensure the circuit to operate always in saturation region. The $V_{out\ (max)}$ and the gain can be increased by adding extra parallel transistors to M6 transistors. The design of single stage op-amp and cs amplifier is used to improve the gain performance parameter of opamp. The M1, M2, M3 and M4 transistors provides the differential input pair circuitry and the capacitor Cc is used as first stage load capacitor. The parallel combination of M6,M7 ……Mn transistors of cs amplifier of Figure 3 is used to improve the gain performance parameter of opamp. C_L is used as load capacitor for overall circuit

IV. FULL CUSTOM DESIGN OF OP-AMP

The designed op-amp has been simulated to find the different characteristics of the designed op-amp. The total design performed in Cadence tool. Different test benches have been created and extracted design has been then simulated with the parasitic values and compared with the schematic. Later in the chapter we also have compared the obtained parameters of the device through simulation to the specifications for the device.

Table1: Cadence tool mapping for Full custom design flow

Design Action	**Tool Name**
Schematic entry	Virtuoso schematic editor
Symbol creation	Virtuoso Symbol editor
Simulation	Virtuoso Analog Design Environment tool
Layout, DRC	Assura
Layout Vs Schematic	LVS tool
Targeted Technology	90nm

Design Issues

Typical Design factors

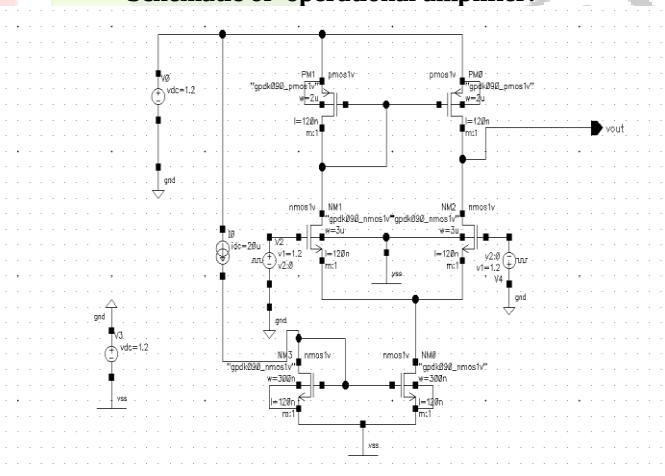
- DC Gain (Av) Frequency Response
- Unity Gain Bandwidth Phase Margin
- Power Dissipation Load Capacitance
- Slew Rate
- Output Voltage Swing
- CMRR

The design process involves the two major steps, the first is the conception of design ,and second one is optimization of design . The conception of the design has been accomplished by proposing an architecture to meet the given specifications. This step is normally done by using hand calculations in order to maintain the clear view point necessary for choices that must be made. Second step is to take the "first-cut" design and verify and optimize it. This is normally done by using Computer simulation and can include such influences as environmental or process variations. The full custom design of basic two stage op-amp using Cadence tools and 90nm is shown in Figure 4. This design is used for op-amp functional verification and the simulation result is shown in Figure 5. This design procedure assumes that the gain at dc (Av), unity gain bandwidth (GB), input common mode range (Vin(min) and Vin(max)), load capacitance (CL), slew rate (SR), settling time (Ts), output voltage swing (Vout(max) and Vout(min)) are given. Choose the smallest device length which will keep the channel modulation parameter constant and give good matching for current mirrors. Two stage OPAMP is designed for 90 nm technology for the following specifications :-

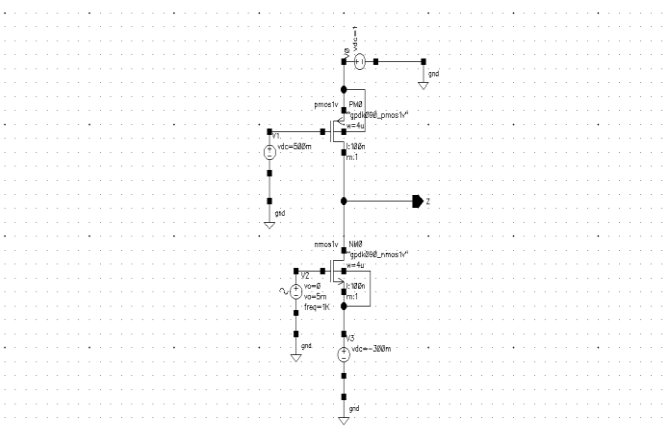
TABLE I DESIGN SPECIFICATION

Open loop Gain	100 V/V (40 dB)
Gain B/W at -3 db gain	5 MHz
Load Capacitance (CL)	10 pf
Slew Rate	10 V/Us
Maximum Power Dissipation	≤ 2mw
Phase Margin	Greater than or equal to 60^0
Channel Length	90 nm
CMRR	43db
Power Supply	2.5 Volt

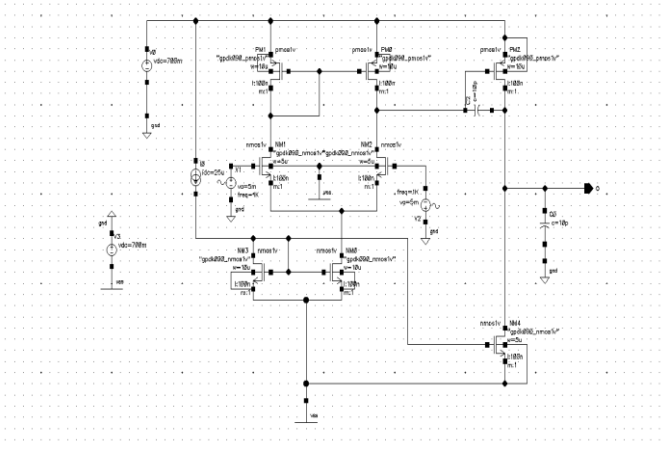
Schematic of operational amplifier:



Single Stage Operational Amplifier

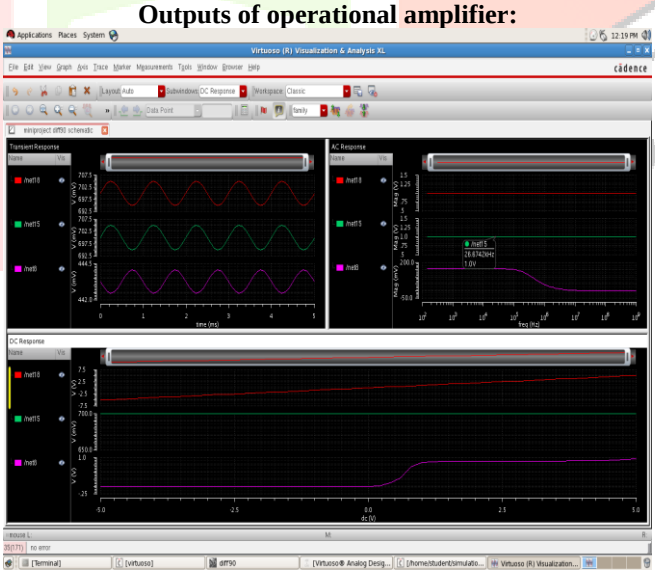


CS Amplifier

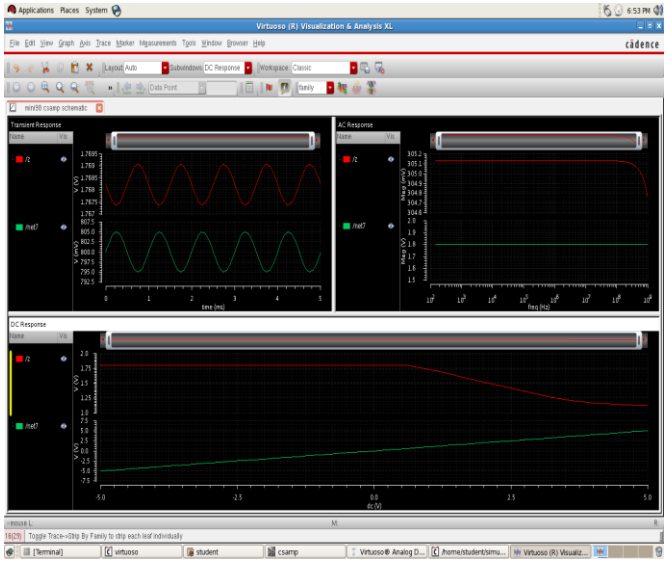


Two Stage Operational Amplifier

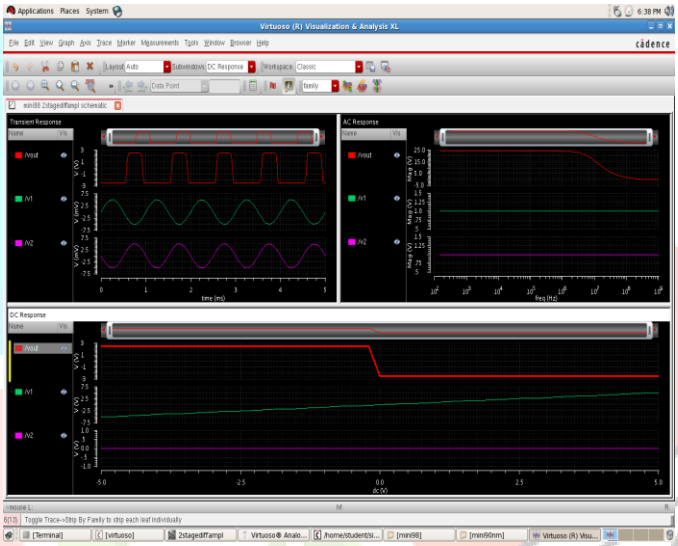
Outputs of operational amplifier:



Single Stage Operational Amplifier



Simulation results of CS Amplifier



Simulation results of two stage operational amplifier

V.CONCLUSIONS

The amplifier presented in this paper operates in saturation mode and regulates its bias current. When a signal is applied the current in the amplifier increases so that these amplifiers have very high driving current. The op-amp has low power as well as low voltage. Its slew rate is higher than reported. The unity gain bandwidth is obtained 5MHz.The two stage op amp circuit is designed for simple compensated features using 90nm technology with L=100nm and achieved a gain of 30 db. This simple op-amp design can be improved in performance by adding gain improvement circuitry.

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