# Design of Programmable Prescaler with True Single-Phase Clock Logic

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***Abstract:*** The programmable prescaler is an essential unit in Phase Locked Loop (PLL) based frequency synthesizer. The high frequency divide-by-64-79 programmable prescaler is presented with true single-phase clock (TSPC) logic which is used for low power application. The proposed programmable prescaler comprises a synchronous divide-by-4/5 dual modulus prescaler, asynchronous divide-by-16 counter and combinational circuitry to control the modulus control (MC) signal. The implementing technology is 45nm bulk CMOS technology. The simulation was performed at maximum frequency 20GHz with the supply voltage 1.1V. The design implemented in LTspice software and the simulation was performed in ng-spice simulation software. The proposed design consumes 15.76mW power for divide-by-64 operation with modulus control signal at zero logic and corresponding propagation delay is 1.5ns. The PVT analysis is done to make our design insensitive to variations in supply voltage and temperature. The comparison of performance parameters of proposed prescaler is given in terms of use of the synchronous divider, dynamic logic, maximum operating frequency, power dissipation, the supply voltage.

***Keywords—Phase Locked Loop (PLL), True Single-Phase Clock (TSPC), Programmable Prescaler, Dual Modulus Prescaler (DMP), Flip-Flop (FF), PVT (Process-Voltage-Temperature)***

## I. INTRODUCTION

The generation of a stable, low-noise, high clock source is critical to obtain which can be used in frequency translate and channel selection in wireless communication. The production of stable frequency is only possible with the help of crystal oscillator of which is very low in the range. The high frequency can be generated using a voltage controlled oscillator, but it gives unstable frequency. To convert this unstable high frequency into a stable state, we can use Phase Locked Loop (PLL). The generation of the high frequency depends on the multi-modulus prescaler which is connected in the feedback loop of the frequency synthesizer block. The frequency spacing between the output frequency of the frequency synthesizer is totally depending on the programmable prescaler.

A major requisite of many electronic systems, such as data acquisition system, data converters is the generation of a stable, high frequency, low noise clock signal. The generation of the different frequency from a single fixed frequency is accomplished by the PLL. Fig. 1 shows the basic block diagram of the PLL based frequency synthesizers.

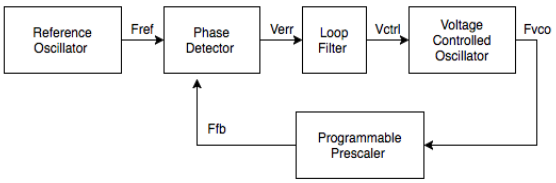


Fig. 1. Block Diagram of PLL frequency synthesizer

Several methods for different requirements of speed, power, application, and division ratio has been presented. The flip-flops (FF) are essential storage element used widely in every digital system. The true single-phase clock (TSPC) FF developed with the goals of low power, high speed, and lowering the clock signal loading [1-8]. To reduce the requirement of the supply voltage, the dynamic threshold MOSFET and forward body biasing technique are used to for threshold voltage reduction [2]. A 17GHz programmable frequency divider was presented for space application in a 130nm SiGe BiCMOS technology. Silicon-Germanium heterojunction bipolar transistors (SiGe HBTs) are of high interest for space applications. This device technology is inherently radiation-hard w.r.t gamma rays, neutrons and protons [4]. The other methods were based on the use of the synchronous dual modulus prescaler (DMP) in the first stage and followed by an asynchronous divide-by-2 counter to design DMP with higher division ratio and multi-modulus prescalers [5-8].

There are two approaches to design the prescaler. 1) Synchronous approach: In this approach, one can get any division ratio according to the combinational circuit used to select the proper division ratio. The major advantage of the synchronous approach is that it provides low jitter. In this approach, all flip-flops are operating at the high frequency so gives high loading on the clock and high-power consumption. 2) Asynchronous approach: In this approach, one can get division ration which is the power of 2. But the

advantage of this approach is loading on the clock is reduced because clock signal only drives the first stage and power consumption is also reduced because each flip-flop run at a lower frequency. The problem with this approach is that jitter is large because jitter is accumulating at each stage.

This paper is organized as follows. Sections II gives the brief introduction about the architecture of programmable prescaler. The proposed TSPC based divide-by-4/5 dual-modulus prescaler is described in Section III. The proposed programmable prescaler presented in section IV. Simulation results and performance summary are given in Section V. Section VI gives the conclusion.

## II. Architecture of Programmable Prescaler

### *A. Basic Modular Programmable Prescaler*

The simple modular multi-modulus prescaler structure comprises a chain of 2/3 divider cell connected like a ripple counter as depicted in Fig. 2. The local feedback enables simple optimization of power dissipation because the feedback lines exist in between adjacent cells.

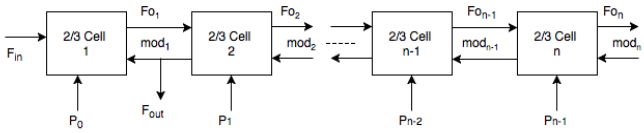


Fig. 2. Modular programmable prescaler architecture.

The advantage of this architecture is that it has the same topology for all the cells presents in the prescaler, therefore simplifying layout work. A chain of n 2/3 cells provides an output signal with a period of,

$T_{out} = 2^n.T_{in} + 2^{n-1}.T_{in}.p_{n-1} + 2^{n-2}.T_{in}.P_{n-2} + \ldots + 2.T_{in}.p_1 + T_{in}.p_0$

$$T_{out} = (2^n + 2^{n-1}.p_{n-1} + 2^{n-2}.p_{n-2} + \ldots + 2.p_1 + p_0).T_{in} \quad (1)$$

In this equation, $T_{in}$ is the time period of the input signal $F_{in}$. The signals $p_0 \ldots p_{n-1}$ are the values by which we can select the proper division ratio of the cells 1-to-n, respectively. The output ranging from 2n (if all pi=0) to 2n+1-1 (if all pi=1) can be realized.

### *B. Pre-Settable Programmable Prescaler*

Another architecture of the multi modulus prescaler is based on an asynchronous ripple counter. This asynchronous counter can be set at any given state. And this counter is basically down counter which counts down until a "zero" state is detected, which generates the reset signal. This process creates the desired division ratio of the prescaler. As the frequencies in the counter are divided by two in every stage because these counters are connected in the asynchronous manner in which every counter is operating at the different frequency, so power dissipation is low but the jitter is high as it accumulates in every stage.

### *C. Dual Modulus Prescaler Based Architecture*

This architecture comprises a dual-modulus prescaler (DMP) of division ratios P and P + 1 with two programmable counters, the "N" counter and the "A" counter as depicted in Fig. 3. These counters are "down-counters". The output of the "N" counter is connected to the "A" counter and it also generates the reload signal for itself. The output of the "A" counter is acts as the Modulus Control (MC) input of the DMP. When the MC signal is high, the prescaler acts as the divide by P + 1, and when the MC signal is low, it acts as the divide by P.

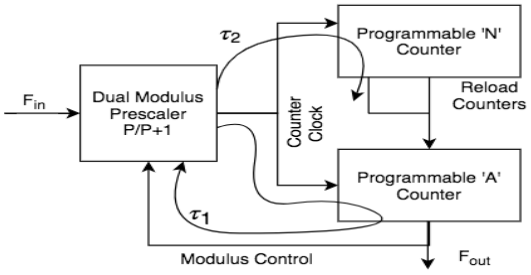


Fig. 3. Dual Modulus Prescaler based Programmable prescaler

The operation principle of the programmable prescaler is as follows. The output signal of DMP is connected to both counters. When the "N" counter counts up to "zero", it generates a reload signal for itself and for the "A" counter. The DMP divides by P + 1 until the "A" counter reaches "zero", and then divides by P. Resulting this event, there are N – A cycle of its output signal

before the "N" counter reaches "zero". So, the time period $T_{out}$ of the output signal can be stated as a function of the time period of the input signal as follows:

$$T_{out} = (A.(P + 1) + (N – A).P).T_{in}$$

$$T_{out} = (N.P + A).T_{in} \quad (2)$$

Where the last term within brackets shows the division ratio of the input signal frequency $F_{in}$.

III. Divide-by-4/5 Dual Modulus Prescaler

The architecture of D flip-flop proposed by Yuan/Svensson is shown in Fig. 4. This circuit is a true single- phase clock (TSPC) based D flip-flop, which uses only one phase of the clock signal. The TSPC based D flip-flop has only 11 transistors with three transistors stacked in each stage. Because of the single clock, this circuit does not suffer from clock skew problem. In this TSPC DFF, when the clock is high (Clk = 1) the flip flop will be in evaluation mode, the two inverters are enabled and propagate the input to output. When the clock is low (Clk = 0), both inverters are disabled, and the flip flop is in hold mode. In this mode, the output holds previous values only.

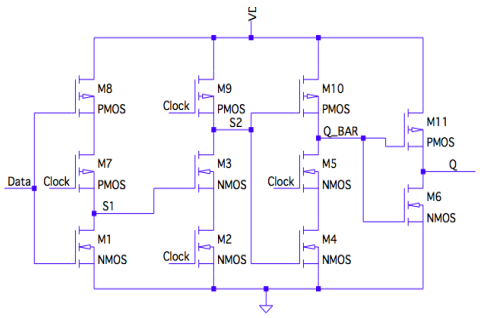


Fig. 4. TSPC based D flip flop

The simulation is done using 45nm CMOS technology with the supply voltage 1.1 using ng-spice simulation software. The simulation was performed at 27 ºC. The change in propagation delay and power dissipation with respect to frequency is shown in Fig. 5 which is as expected.

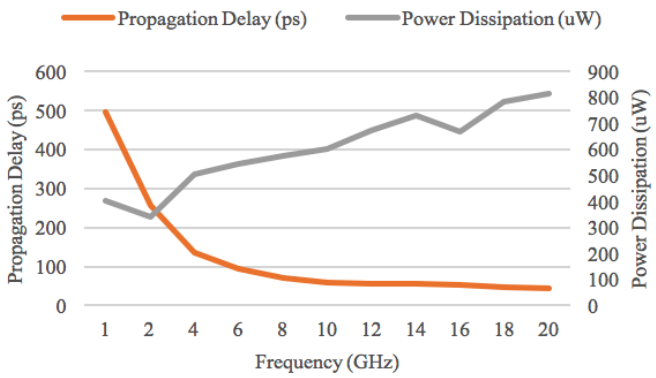


Fig. 5. Propagation delay and power dissipation of TSPC D FF Vs. frequency

The process Corner analysis of our FF design was performed across all five corners at the 20 GHz frequency with $V_{DD}$ 1.1V. These process corners are FF, FS, NN, SF, and SS in which the first and second letter is for NMOS and PMOS respectively, and F stands for Fast, S stands for Slow and NN for nominal.

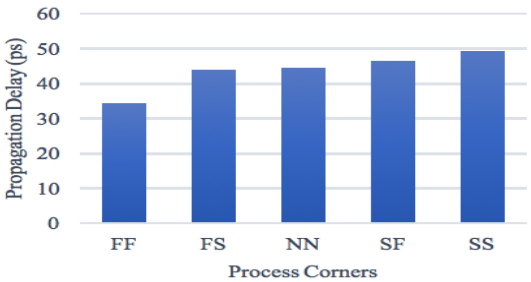


Fig. 6. The propagation delay of TSPC D FF across all corners

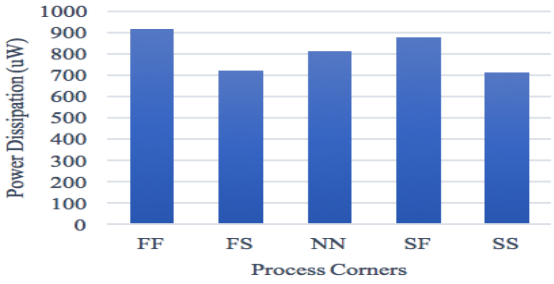


Fig. 7. Power dissipation of TSPC D FF across all corners

The propagation delay of our TSPC D FF at nominal process corner is 44.44ps. The variation in propagation delay at different corners is shown in Fig. 6. The power dissipation of the design at nominal process corner is 813.46uW. Similarly, the variation in power dissipation is also plotted in Fig. 7.

The dual modulus prescaler is used in PLL based frequency synthesizer. The depending upon the requirement of different frequency we can use dual modulus prescaler in the feedback loop of PLL frequency synthesizer to get the frequency which is multiple of the given reference frequency. The main drawback of fixed frequency divider circuit is that it gives large frequency spacing in the frequency synthesizer. So, to reduce the frequency spacing in the generating frequencies of PLL frequency synthesizer, the dual modulus prescaler is used. It can also use to design the multi-modulus or programmable prescaler.

The conventional design of divide-by-4/5 dual modulus prescaler reported in [5] has two inverters, one AND gate and one NOR gate with three DFFs. The proposed divide-by-4/5 dual modulus prescaler is illustrated in Fig. 8. This design of dual modulus prescaler contains three TSPC based DFFs and two NAND gates as in Fig. 8.

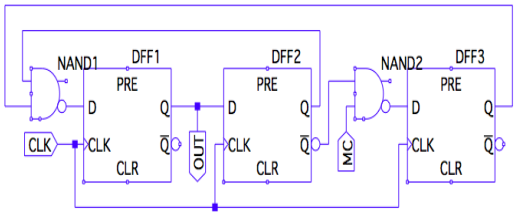


Fig. 8. A TSPC Divide-by-4/5 dual modulus prescaler

In this design, the MC input indicates the modulus control signal which can be used to control the division ratio between divide-by-4 and divide-by-5 operation. When the modulus control input is low the NAND2 gate enables the DFF3 for every clock pulse and circuit acts as mod 4 counter. When the modulus control input is high the NAND2 gate works as inverter and circuit act as mod 5 counter.

## IV. Proposed Programmable Prescaler

A 17GHz programmable prescaler using modular programmable prescaler architecture in 130nm SiGe BiCMOS technology for space application was presented in [4]. In this design, the divider is composed of a cascade of seven divide-by-2/3 circuits. Another design of multi-modulus prescaler using two divide-by-2/3 and divide-by-4/5 Dual Modulus Prescaler (DMP) using True Single-Phase Clock (TSPC) logic was presented in [6]. The multi-modulus 32/33/39/40/47/48 prescaler using Modified Extended TSPC (METSPC) was presented in [8]. The PVT analysis of proposed design was performed in [8,9].

The proposed programmable prescaler structure is based on dual modulus topology with true single-phase clocking logic. The TSPC dynamic circuit originally proposed as a high-speed topology. The TSPC structure also consumes less power and occupies less area compared to other methods. In this logic, the only single phase of the clock is used which makes this design free from a clock skew problem. Both the synchronous and an asynchronous counter are implemented using TSPC D FF.

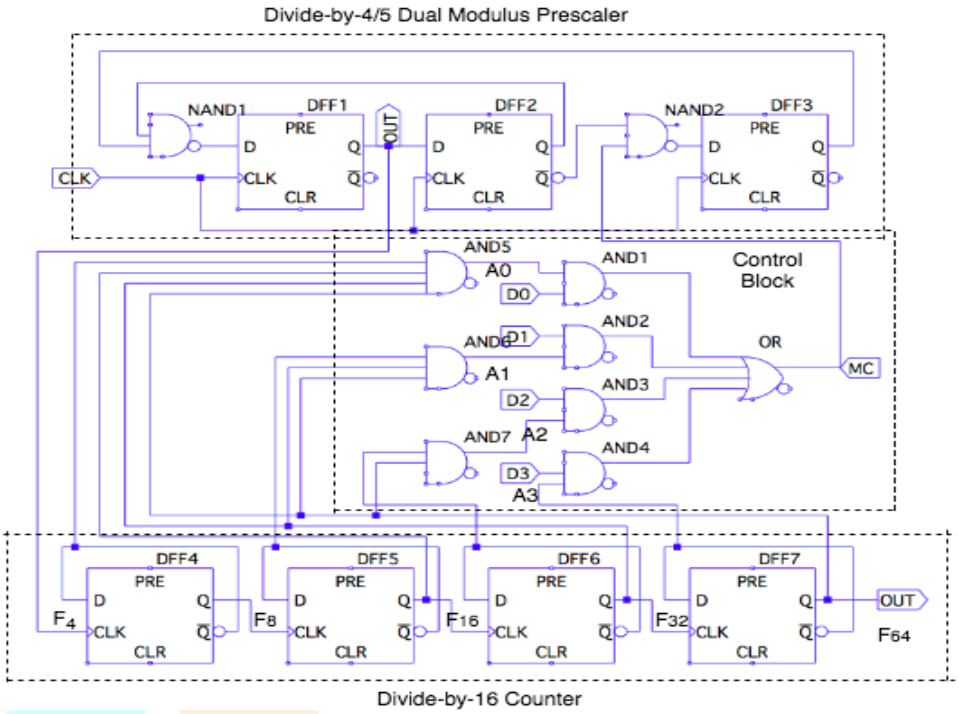


Fig. 9. Block Diagram of proposed programmable prescaler

The function of the control block is explained as follows. The MC signal changed according to the logic values of input signal $D_3$-$D_0$ as shown in Fig. 9. When the input signals $D_3$-$D_0$ are at logic zero values, the MC signal is also zero because the enable input for AND gate is logic one. So, the divide-by-4/5 dual modulus prescaler does the divide-by-4 (MC=0) operation and the programmable prescaler gives divide-by-64 frequency division. The signals $A_0$-$A_3$ are activated according to the asynchronous counter outputs $F_8$, $F_{16}$, $F_{32}$, and $F_{64}$. For signals $A_0$-$A_3$, if the input signals $D_3$-$D_0$ are at logic one then the MC signal is combined cycle of n clocks, where $n = D_3.2^3 + D_2.2^2 + D_1.2 + D_0$. The MC signal changed according to the logic values of signals $A_0$-$A_3$ and $D_3$-$D_0$. When the MC signal is at logic one value, the synchronous DMP does the divide-by-5 (MC=1) operation. Therefore, the proposed prescaler can be programmed as divide-by-64-79 using various combination of 4-bit which can be used to generate the MC signal, and the divider ratio is given as

$$P = 64 + D_3.2^3 + D_2.2^2 + D_1.2 + D_0 \quad (3)$$

Where $D_n$ is the programmable input bit.

In the proposed design, the modulus control signal controls the divide ratio of high speed divide-by-4/5 dual modulus prescaler. The output of this DMP is worked as input to the asynchronous counter. The simulation of this programmable prescaler was performed using 45nm CMOS process in ng-spice simulation software. The simulation results of this design are shown in Fig. 10. The maximum frequency of proposed programmable prescaler is 20 GHz with the supply voltage 1.1V. The simulation was performed at 27 $^0$C temperature. We have done the process corner analysis of TSPC D FF at 20GHz with the supply voltage 1.1V using 45nm CMOS process which results are shown in Fig. 6 and Fig. 7.

Since we checked the functionality of TSPC D FF for process variation (at all 5 corners), use this design of FF in the proposed programmable prescaler that will be free from process variations. To complete PVT variation, we analyzed the design across the other 2 parameters viz., the supply voltage $V_{DD}$ and temperature. The process variation analysis of Extended-TSPC D FF reported in [9]. The PVT analysis of proposed programmable prescaler described in the following section.

## V. Simulation Results and Performance Comparison

The simulation results of proposed programmable prescaler are shown in Fig. 10 using 45 nm bulk CMOS technology in ng-spice software at the 20GHz frequency and with the supply voltage 1.1V. This simulation result shows the result of the programmable prescaler when the input signals $D_3$-$D_0$ are at logic zero and modulus control input is at logic zero. So, the synchronous divide-by-4/5 dual modulus prescaler acts as a divide-by-4 counter and whole design gives divide-by-64 output. For other combination of the input signals $D_3$-$D_0$ and $A_0$-$A_3$, the modulus control signal value will be changed accordingly. When modulus control signal is at logic one, the synchronous divider acts as a divide-by-5 counter.

As shown in Fig. 10, the v(11) shows the input clock signal, v(14) shows the output of the divide-by-4/5 dual modulus prescaler, v(59) shows the output of the DFF4 ($F_8$), v(61) shows the output of the DFF5 ($F_{16}$), v(63) shows the output of the DFF6 ($F_{32}$), v(65) shows the output of the DFF7 ($F_{64}$). The simulation was performed at 27 $^o$C temperature. The proposed programmable prescaler consumes power 15.76mW with corresponding propagation delay 1.5ns for divide-by-64 operation when modulus control signal is at logic zero.

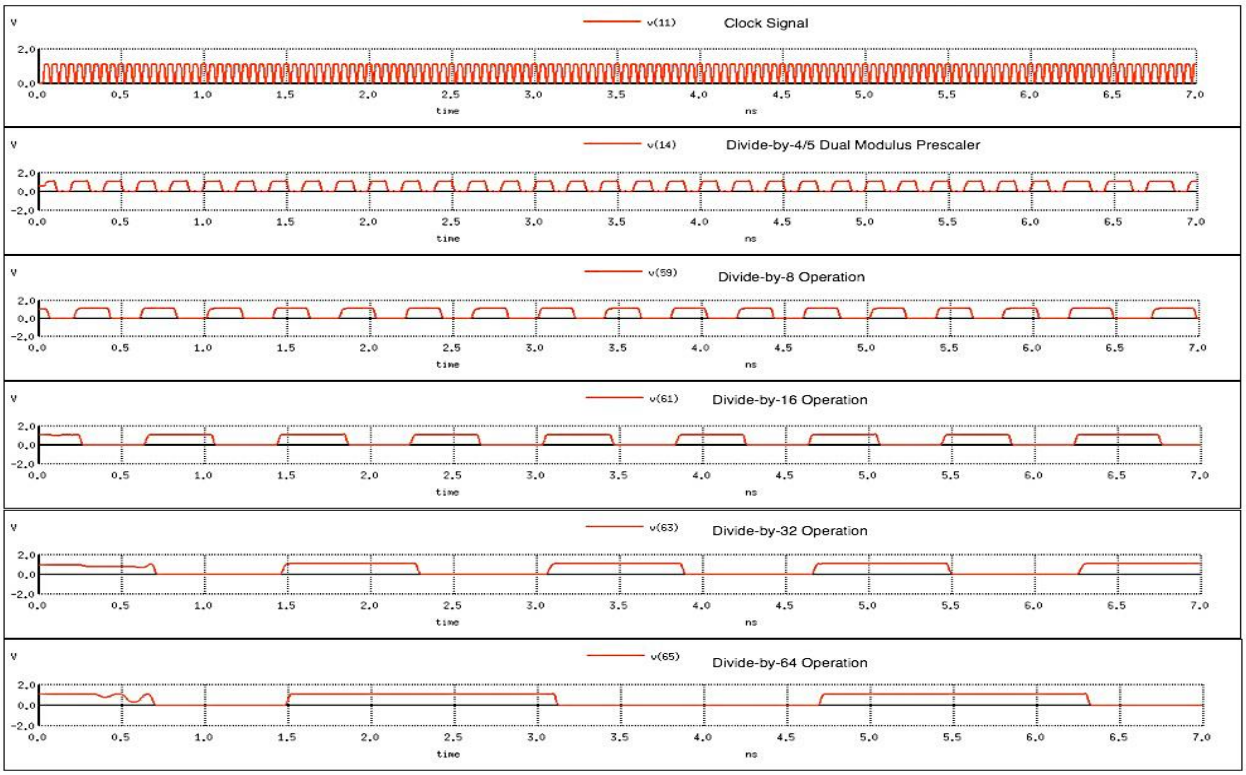


Fig. 10. Simulation waveforms of a proposed programmable prescaler using 45nm CMOS technology

The nominal supply voltage of this programmable prescaler is 1.1V. To check variations in power dissipation and propagation delay, we varied a supply voltage $V_{DD}$ from 1.04 to 1.2V. The performance parameters like propagation delay and power dissipation for $V_{DD}$ variation at 20GHz is plotted in Fig. 11.

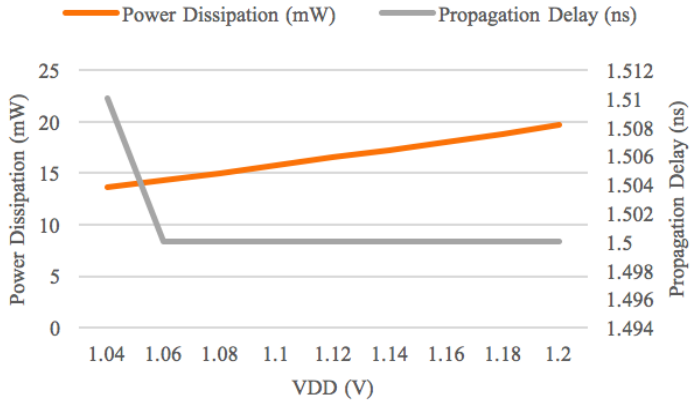


Fig. 11. The plot of power dissipation and propagation delay over a range of $V_{DD}$

The nominal temperature at which we simulated our programmable prescaler was 27 ºC. To make sure that the proposed programmable prescaler is insensitive to variation in temperature, we varied temperature from -10 to 90 ºC. The behavior of propagation delay and power dissipation for variation in temperature at 20GHz is plotted in Fig. 12.

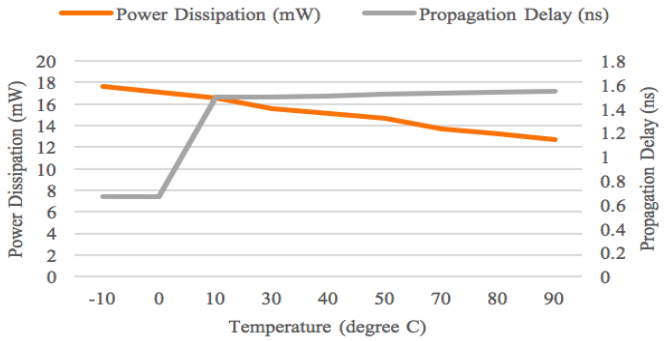


Fig. 12. The plot of propagation delay and power dissipation over a range of temperature

The programmable prescaler is the most important part of the fractional frequency synthesizer for multi-standard operation for wireless communication. This proposed programmable prescaler can divide the input operating frequency between 64-to-79 which depends on the four modulus control input signals $D_3$-$D_0$. A complete programmable prescaler consisting of a synchronous dual modulus prescaler, an asynchronous counters and modulus control block. The performance comparison our programmable prescaler with various previously reported work is shown in TABLE I.

TABLE I. PERFORMANCE SUMMARY TABLE

| Design / Parameters | [2] | [3] | [4] | [5] | [6] | [7] | Proposed Work |
|---|---|---|---|---|---|---|---|
| Publication | ICAEESE | ISCAS | BCTM | IEEE Transaction on VLSI Systems | ESSCIRC | ISCAS | - |
| Year | 2016 | 2015 | 2015 | 2014 | 2014 | 2015 | - |
| Type | MOSFET-TSPC DTMOS-FBB TSPC | TSPC | CML D Latch | TSPC | TSPC | Improved TSPC | TSPC |
| A Synchronous Divider | - | Pseudo Divide-by-4/5 | Divide-by-2/3 | Pseudo Divide-by-2/3 | Divide-by-2/3 and Divide-by-4/5 | Divide-by-4/5 | Divide-by-4/5 |
| Divide Ratio | ÷2 | 32/33 | 16-255 | 16/17 | ÷64, ÷80, ÷96, ÷100, ÷112, ÷120, ÷140 | 32/33 | 64-79 |
| Max. Fre. (GHz) | 8/2.5 | 17.9 | 17 | 0.002-5.8 | 17 | 17.9 | 20 |
| Power (mW) | 0.106/0.018 | 0.153/0.197, 0.245/0.249 | - | 2.6 | 2 | 0.245/0.249 | 15.76 |
| Supply Voltage (V) | 1.2/0.6 | 1.1 | 2.3 | 1.6 | 1 | 1.1 | 1.1 |
| Process (nm) | 130 | 40 | 130 SiGe BiCMOS | 180 | 65 | 40 | 45 |

## VI. CONCLUSION

In this article, a high-speed programmable prescaler is discussed and implemented using LT-spice and ng-spice software. The high speed and low power true single-phase clock logic based D flip flop is presented which is used to design a synchronous divide-by-4/5 dual modulus prescaler and an asynchronous divide-by-16 counter. The process corners analysis has been performed at all four corners. The simulation is done at maximum operating frequency 20GHz with the supply voltage 1.1V using 45nm CMOS technology. The behavior of the performance parameters with respect to the supply voltage and temperature were checked. This programmable prescaler can be used in fractional frequency synthesizer which is used in wireless communication.

## VII. References


[1] Jin-Fa Lin, Ming-Hwa Sheu, Member, IEEE, Yin-Tsung Hwang,Member, IEEE, Chen-Syuan Wong, and Ming-Yan Tsai, "Low-Power 19-Transistor True Single-Phase Clocking Flip-Flop Design Based on Logic Structure Reduction Schemes", IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, 2017.

[2] Tan Chen Hou, Noorfazila Kamal, Khairuddin Jaafar, Mamun Ibne Reaz, Jahariah Sampe, "Design of a low power static frequency divider", International Conference on Advances in Electrical, Electronic and System Engineering, 14-16 Nov 2016, Putrajaya, Malaysia.

[3] Song Jia, Shilin Yan, Yuan Wang, Ganggang Zhang, "A Low-Power High-Speed 32/33 Prescaler Based on Novel Divide-by-4/5 Unit with Improved True Single-Phase Clock Logic," IEEE International Symposium on Circuits and Systems (ISCAS), 2015.

[4] Frank Herzel, Johannes Borngraber, Arzu Ergintav, Maciej Kucharski, and Dietmar Kissinger, "A 17GHz Programmable Frequency Divider for Space Applications in a 130 nm SiGe BiCMOS Technology", Bipolar/BiCMOS Circuits and Technology Meeting - BCTM, 2015, IEEE.

[5] Wenrui Zhu, Haigang Yang, Tongqiang Gao, Fei Liu, Tao Yin, Dandan Zhang, and Hongfeng Zhang, "A 5.8-GHz Wideband TSPC Divide-by-16/17 Dual Modulus Prescaler", IEEE TRANSACTION ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, 2014.

[6] Manthena Vamshi Krishna, Anil Jain, Nasir Abdul Quadir, Paul D. Townsend, Peter Ossieur, "A 1V 2mW 17GHz Multi-Modulus Frequency Divider based on TSPC logic using 65nm CMOS", European Solid-State Circuits Conference (ESSCIRC), ESSCIRC 2014.

[7] Song Jia, Shilin Yan, Yuan Wang, Ganggang Zhang, "A Low-Power High-Speed 32/33 Prescaler Based on Novel Divide-by-4/5 Unit with Improved True Single-Phase Clock Logic", International Symposium on Circuits and Systems (ISCAS), 2015 IEEE.

[8] Mohammed Zackriya V, Harish M Kittur, "90nm CMOS Low Power Multimodulus 32/33/39/40/47/48 Prescaler with METSPC", International Conference on Advances in Computing and Communications, 2013.

[9] John Reuben, Mohammed Zackriya V, Dr. Harish M kittur, "Low Power, High-Speed Hybrid Clock Divider Circuit", International Conference on Circuits, Power and Computing Technologies (ICCPCT), 2013.

[10] Ching-Yuan Yang, "A high-frequency CMOS multi-moduldus divider for PLL frequency synthesizers", Analog Integrated Circuits and Signal Processing, May 2008, Volume 55, Issue 2, pp 155-162.

[11] Cicero S. Vaucher, Bram Nauta, "Architecture and circuit Design of Programmable Dividers" in Architecture for RF Frequency Synthesizers, Pages 201-227.

[12] Sung-Mo Kang, Yusuf Leblebici, "Dynamic Logic Circuit", in CMOS Digital Integrated Circuits Analysis and Design, Third ed. New York: McGraw-Hill, 1996, pp 350-396.

[13] ChristianPiguet, "Logic Circuits and Standard Cells and Low Power Very Fast Dynamic Logic Circuits" in Low Power CMOS Circuits: Technology, Logic Design and CAD Tools, First ed. CRC Press, 2005, pp. 7.1-7.7 and 8.1-8.7

[14] XiaopengLi, Mohammed Ismail, "RF CMOS Building Blocks" in Multi- Standard CMOS Wireless Receivers Analysis and Design, Kluwer Academic Publishers, pp. 45-57.