Design of Vedic multiplier based on VHDL

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***Abstract*— Design of vedic multiplier based on fault coverage is proposed. The multiplier is design for 64 bit. The multiplier is design using Urdhava Tiryakbhyam method. In these proposed design fault detection is proposed. The circuit behaviour is check by designing build in self test circuit. The circuit covers all 64 bit fault coverage, which means the circuit shows the status of a multiplier whether it provides correct or incorrect output. The circuit is tested on various input combinations. Those combinations are provided by LFSR. The proposed Vedic multiplier design is tested. The circuit is ready very efficient which can be tested for various multiplier. The ALU is the heart of any processor or the any complex system. To increase the speed of any system, it is required to increase the speed of ALU, but with low power consumption and for that portable life is required .Vedic multiplier gives faster processing speed in terms of array multiplier. VLSI designing techniques are the source to reengineering any digital electronics circuitry. In this paper a low power 64 bit ALU is designed in VHDL.**

***Keywords*— Vedic multiplier,Urdhva Tiryakbhyam method, Vedic Mathematics ,64 bit multiplier ,Vedic Mathematics.**

I. INTRODUCTION

Multipliers are widely utilized as a part of Microchips, DSP and Correspondence applications. For higher arrange Duplications, countless are to be utilized to play out the incomplete item expansion. The need of low power and fast Multiplier is expanding as the need of fast processors are expanding. The Vedic duplication system is in view of 16 Vedic sutras or maxims, which are as a matter of fact word formulae portraying regular methods for understanding an entire scope of numerical issues [1] The scientific activities utilizing, Vedic Technique are quick and requires less equipment, this can be used to enhance the computational speed of processors. This paper depicts the outline and usage of 4x4 piece Vedic multiplier in light of Urdhva-Tiryakbhyam sutra (Vertically and Transversely strategy) of Vedic Arithmetic utilizing EDA (Electronic Outline Mechanization) apparatus. The utilization of Vedic science lies in the way that it decreases the average counts in traditional arithmetic to exceptionally basic ones. This is so in light of the fact that the Vedic formulae are asserted to be founded on the normal standards on which the human personality works. Vedic Science is a procedure of number-crunching rules that permit more productive speed usage. It additionally gives some viable calculations which can be connected to different branches of designing such as registering.

III. Vedic Multiplier:

Vedic multipliers depend on Vedic Sutras. In Sanskrit word 'Veda' remains for 'information'. Vedic science is accepted to be reproduced from Vedas by Sri Bharti Krishna Tirathaji between the years 1911 to 1918. The Vedic arithmetic has been separated into sixteen distinct Sutras which can be connected to any branch of science like polynomial math, trigonometry, geometry and so on. Its techniques diminish the intricate figurings into more straightforward ones since they depend on strategies like working of human personality accordingly making them less demanding. It has been seen that being rational and symmetrical, they devour lesser power and procure bring down chip region Vedic Mathematics manages Sixteen Sutras .These sutras are given underneath one after another in order with their concise significance. Every one of these sutras have tremendous examination. Discussion of all of them is beyond the scope of this paper. Only one Sutra number 14 "**Urdhva Tiryakbhyam**" has been discussed.

1. Anurupye Shunyamanyat– If one is in ratio, the other is zero
2. Chalana-Kalanabyham– Differences and Similarities
3. Ekadhikina Purvena– By one more than the previous one
4. Ekanyunena Purvena– By one less than the previous one
5. Gunakasamuchyah– The factors of the sum is equal to the sum of the factors
6. Gunitasamuchyah– The product of the sum is equal to the sum of the product
7. Nikhilam Navatashcaramam Dashatah– All from 9 and the last from 10
8. Paraavartya Yojayet– Transpose and adjust
9. Puranapuranabyham– By the completion or non completion.
10. Sankalana-vyavakalanabhyam– By addition and by subtraction
11. Shesanyankena Charamena– The remainders by the last digit
12. Shunyam Saamyasamuccaye– When the sum is the same that sum is zero
13. Sopaantyadvayamantyam– The ultimate and twice the penultimate
14. Urdhva Tiryakbyham– Vertically and crosswise.
15. Vyashtisamanstih– Part and Whole
16. Yaavadunam– Whatever the extent to fits deficiency

III. URDHVA TRIYAKBYHAM SUTRA:

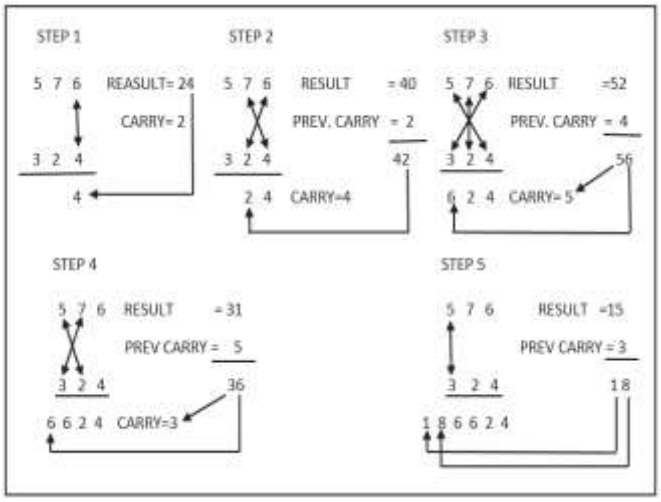

Figure1 : VEDIC MULTIPLIER STEPS 3X3

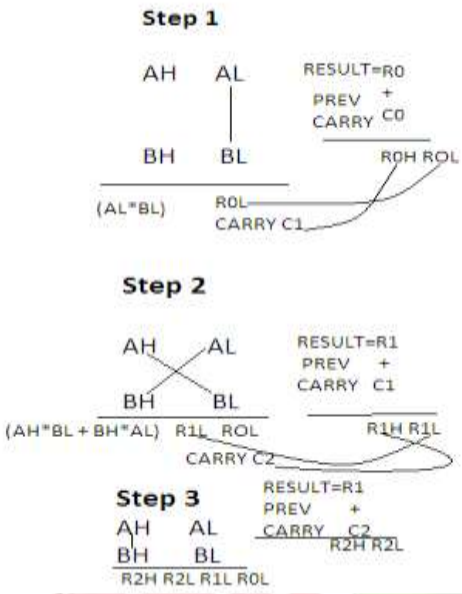

FIG.2 : VEDIC MULTIPLIER STEPS 2X2

The sutras in Vedic mathematics helps to do almost all types of numeric calculations in easy and fast manner. This sutra is typically used for the multiplication purpose, applicable to all types of multiplication. Any bit binary number can be multiplied quickly by using this sutra. The meaning of this sutra is vertically and crosswise. Given below summarize the general process of the working of the Urdhva triykbyham sutra. For that we have consider here two number A and B having digits AH and AL for A number and BH and BL for number. The result is in the form R0,R1,R2 and each time carry is added in to each product i.e.C0,C1,C2. So there will no carry propagation occur in the result due to which delay will be minimized. By using this sutra the carry will not propagated up to the higher level each time it will added to the product term, so time required to propagate carry up to higher level will be minimized. By designing this 2bit multiplier we have to design the 64 bit multiplier. Following block diagram shows the diagram for 64bit Vedic multiplier in the following fig shows the block diagram, RTL view and technology schematic and output waveform of 64bit Vedic multiplier.

IV: Proposed Design

The Vedic multiplier with built in self test is design which cover all the output. Fig.2

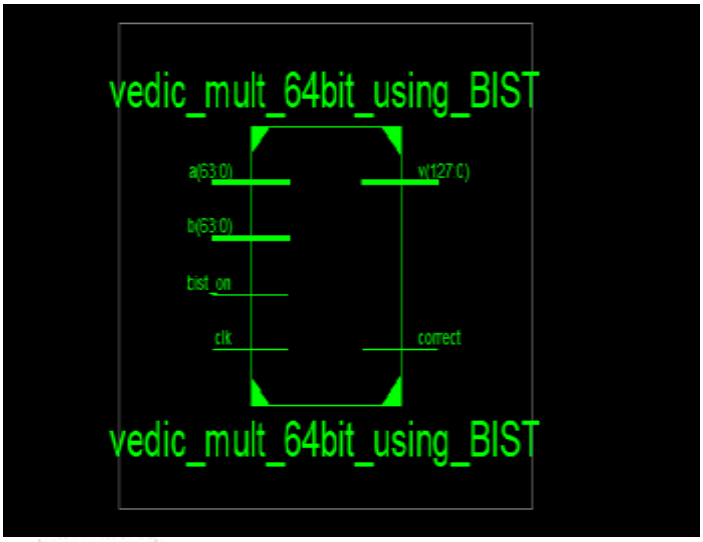

Figure.2 Top Level Entity of 64 bit Vedic with BIST

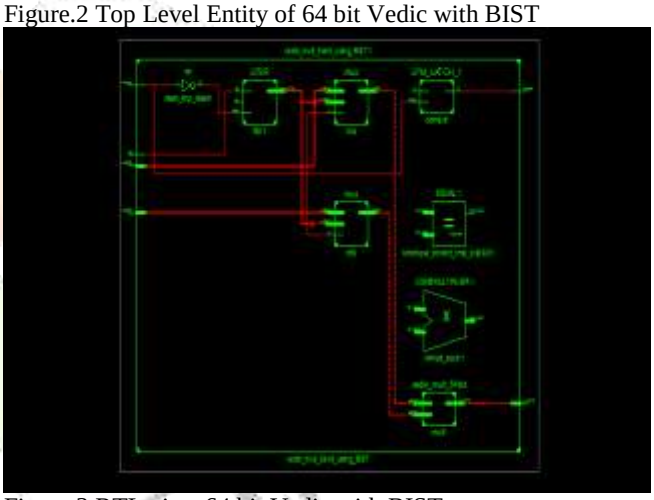

Figure.3 RTL view 64 bit Vedic with BIST

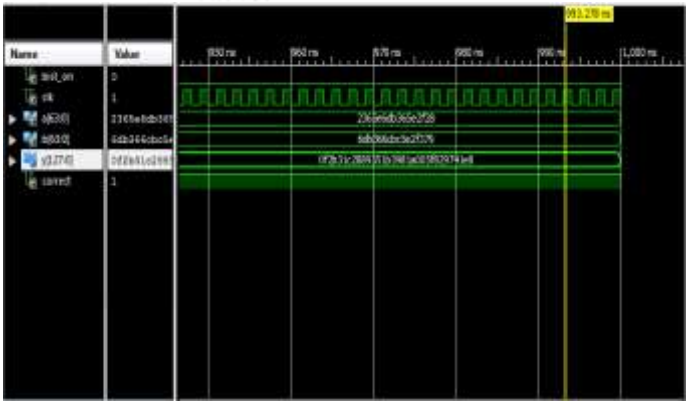

Figure.4 Waveform of 64 bit Vedic with BIST

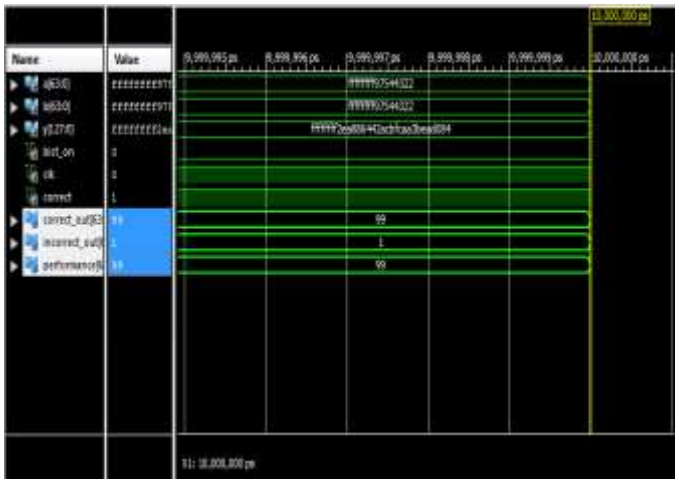

Figure.5 : Waveform for 64 bit Vedic Multiplier with 99% fault coverage

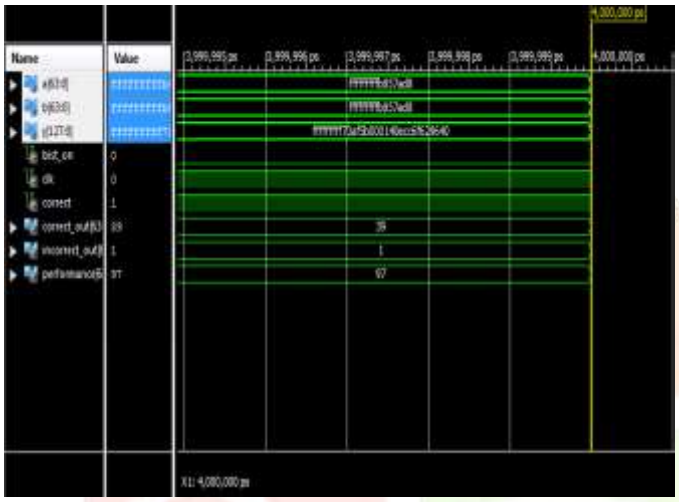

Figure.6: Waveform for 64 bit Vedic Multiplier with 97% fault coverage

Table 1: Comparison Analysis of various multiplier with fault test circuit.

Multiplier Type	Name Of Operation		
	Number Of LUT Used	Number Of Bonded IOBS	Maximum Combinational Path Delay(ns)
64-BIT Vedic Multiplier Using BIST	17495/2400	259/102	27.598ns
32-BIT Vedic Multiplier Using BIST	2875/2400	131/102	25.293ns
16-BIT Vedic Multiplier Using BIST	706/2400	67/102	21.854ns

V. CONCLUSION:

The design of 64 bit Vedic multiplier with fault detection capability is studied and design. The circuit is tested for various combinations. The delay is calculated as 27.598ns.The Circuit is efficiently work and tested for manual combination. The future work of these project is to design for fault detection and coverage for higher bits.

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