IP CORE FPGA DESIGN USING VHDL FOR DIGITAL FILTER IN STRESS SPEECH IDENTIFICATION

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Abstract: Today the lifestyle of human are changing tremendously, every person wants to lives a luxurious life but doing all these things Stress is a burden which is acting on individual's body in form of various diseases. Everybody agrees to avoid the stress but when the actual time comes no one can escape from it. Every speech processing system must be judged on two basic factors which govern its usability- Accuracy and speed. Unfortunately, one of them almost invariably comes at the cost of the other. A higher accuracy rate implies a wider training sequence and higher number of iterations in the learning algorithm, all of which would necessarily take a far greater number of iterations in the learning algorithm, all of would necessarily take a far greater number of clock cycles in a standard processor setting. This paper presents the solution on Adaptive Empirical Mode Decomposition (AEMD) Algorithm applied to voice for benchmark as well as real time database in collaboration with VHSIC Hardware Description Language (VHDL) to introduce a high degree of parallelism methodology thereby reducing the number of clock cycles required for its implementation. This is possible when we port the digital filter part of the MATLAB algorithm onto an A Field Programmable Gate Array (FPGA).

***Index Terms*-MATLAB, AEMD, VHDL, FPGA**

I. INTRODUCTION

Today's world is filled with fast and growing technology. Day to day the working environment is having ease of comfort with this technology. Due to this there has been less physical movements and has induced mental stress levels which introduced new field of research as analysis of speech. In the study of Speech Identification by machine is a critical core technology for the Information age. An Empirical Mode Decomposition (EMD) was developed using MATLAB to detect micro-tremor in the speech to detect stress [1], [2], [3], stress recognition was considered in speech signal as normal or stressed. Again stress speech will be further considered as high level stress or low level stress depending on its amplitude level [4],[5],[6], in this paper a part of AEMD from MATLAB has been taken as input and given to VHDL to increase the speed and accuracy through Digital filter design in VHDL.

II. FLOWCHART ON DIGITAL FILTER FPGA DESIGN

In the implementation of the designing a Digital filter which is Band-pass Filter [7] we used a Verilog and test-bench file. We got two things from Matlab which are given as input to the Verilog, they are as follows.

1. Expected input to be applied to the filter design in Verilog.
2. What is expected output coming from Verilog filter design.

The VHDL and verilog hardware description languages (HDLs) allow you to embed constraints in the design code at the highest level of abstraction. In designing the Band-pass filter we need the above two things. In the following flowchart HDL coding is done in Model-Sim Software and Xilinx Plan Ahead Software. To this design Gate Simulation is performed and verified for making a VHDL Test Bench. In the Logic Synthesis a User Constraints File (ucf) is used during the implementation process, you can enter timming, placement, and pinout constraints in the ucf file. The output is obtained, by doing Physical design and to configure it. We get the Band-pass filter with high speed and accuracy in FPGA. The design works in Verilog & from Verilog we can convert on FPGA.

III. IMPEMENTATION

An IP (Intellectual Property) core is a block of data or logic that is used in making VHDL to describe digital and mixed signal system such as speech signal in a field programmable gate array specially used for designing of digital filter. In this work stressed speech identification is implemented in VHDL [8]. In the Verification scheme functional simulation is done using Xilinx ISIM Simulator. ISIM software has significant enhancements to the graphical user interface, and project flows, which offer a more comprehensive design flow for Logic designer[9],[10]. Test-bench is developed for top level design for Band-pass Filter. Stimulus is configured for testing top level IP core. Performance is observed using simulation results and Timing diagram. The Band-pass Filter

which we designed needs only 36µs to execute its working at high speed. Following Timing Diagrams will be able to understand the design.

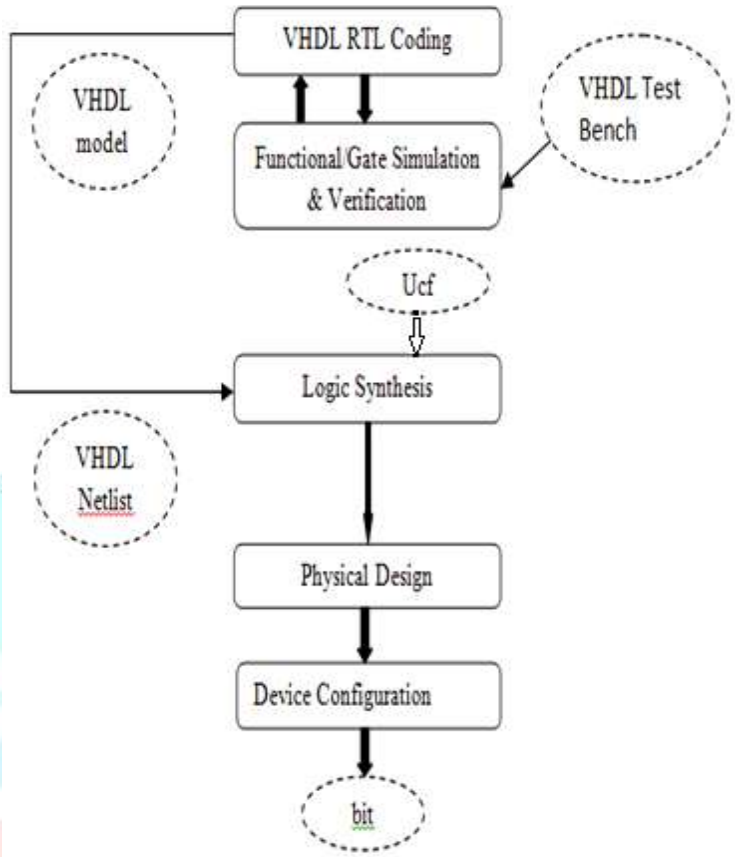

Figure1 Flowchart for FPGA design methodology.

IV. RESULTS

The following figure determines the test has passed completely, which means that the AEMD Algorithm working in Matlab software level [1] is matching the expected output through Verilog in hardware on FPGA. The design was compiled and then simulated with self checking mechanism to get expected output which will run the band-pass filter with high speed.

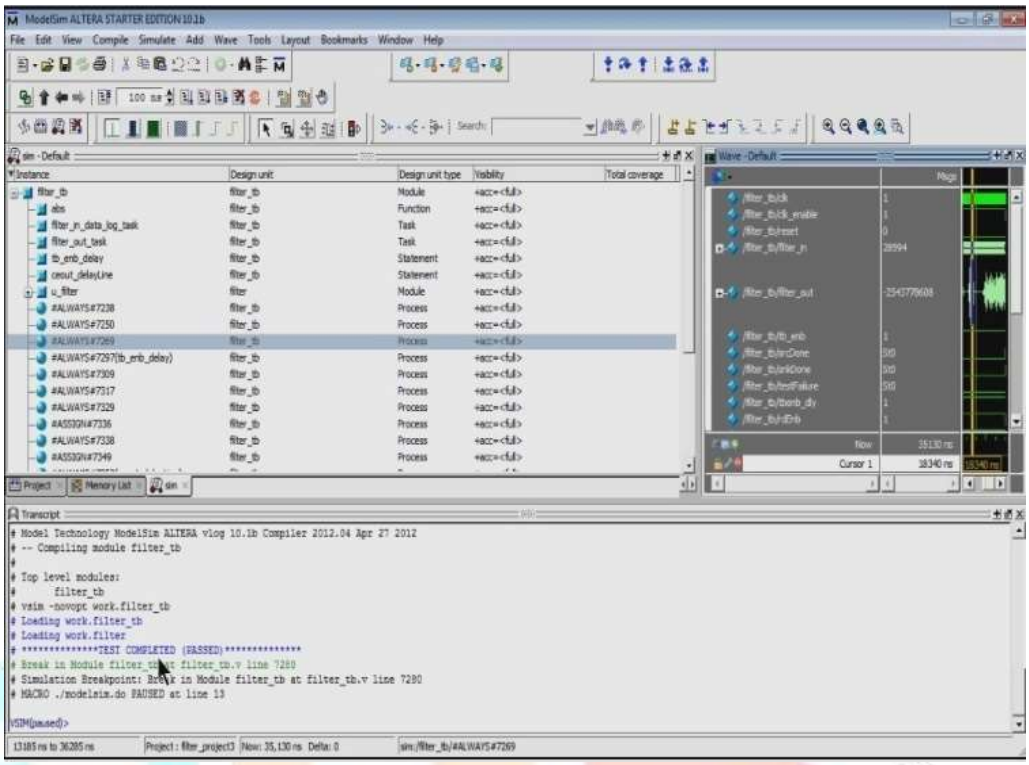

Figure 2 self checking test-benches.

The following figures consist of hexadecimal values as input to the filter.

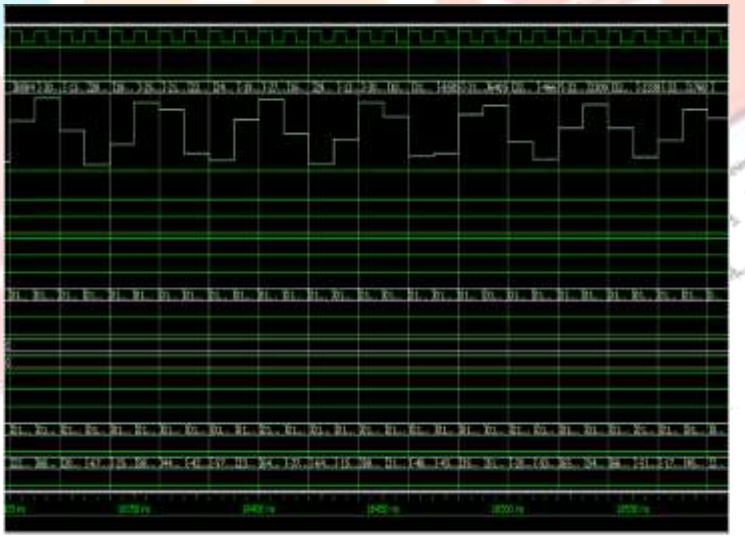

Figure 3 Zoomed filter input as hex values.

The Input or Output of filter is in time. Hence in all waveform the “X” and “Y” axis is in time. The figure 4 shows the filter output which is a staircase waveform

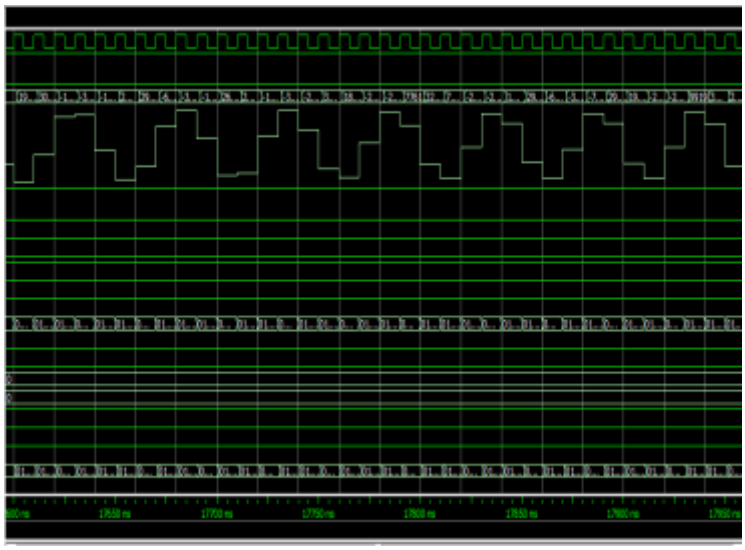

Figure 4 Zoomed filter output.

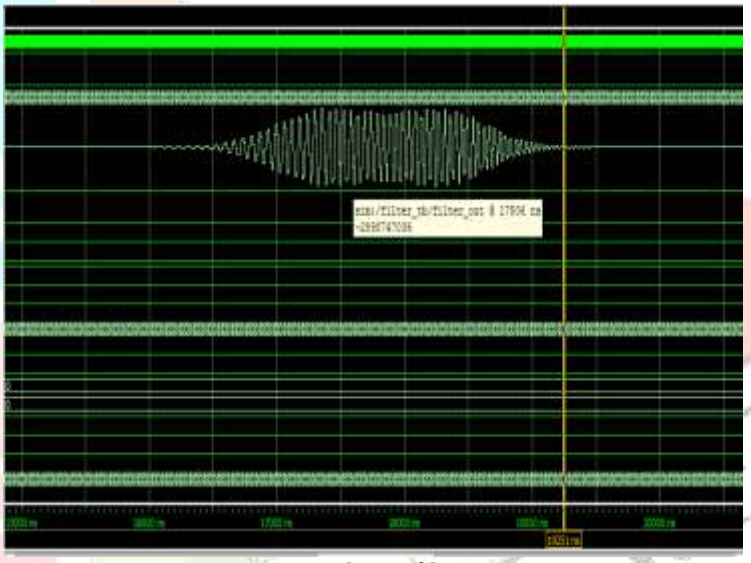

Figure 5 Band-pass filter output

The complete band-pass filter is design and shown in above shown figure.

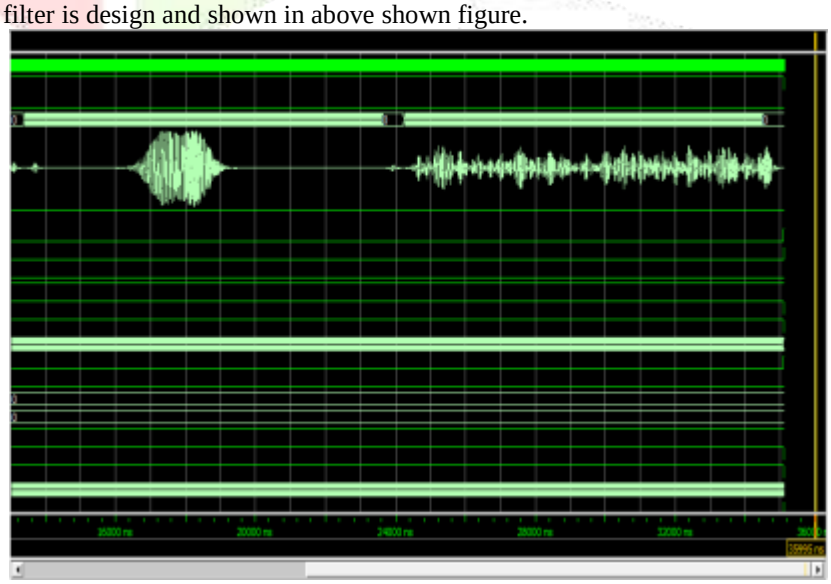

Figure 6 Complete Waveform for designing digital filter

Figure 6, explains and helps us to understand that the design of Band-pass filter to execute needs only 36 µs to work. This is very high speed for any filter to filter out stress speech which will improve the Identification of the stress in speech.

V. CONCLUSIONS

This paper designs a digital filter which is a Band-pass Filter to filter out the Stress speech in Verilog. The time to execute the filter needs only 36µs which is at very high speed at software level when final checking happened. The output coming from Matlab is matching with the output as Verilog. This is the advantage of Converting one part of Matlab for software algorithm into hardware on FPGA in Microseconds. This time is very low for software to run. This is the reason to choose a digital filter design in Verilog for Stress Speech Identification.

VI. FUTURE SCOPE

After the designing of Band-pass Filter the rest Algorithm will be implemented in Matlab Software, to capitalize on its signal processing capabilities.

REFERENCES

[1] Mrs. N.P. Dhole , Dr. S.N. Kale. 2017. Adaptive Empirical Mode Decomposition of Speech Signal, International Journal of Emerging Trends & Technology in Computer Science (IJETTCS). Volume 6, Issue 3, ISSN 2278-6856, PP. 422-425.

[2] Laxmi Narayana M, Sunil Kumar Kopparapu. 2009. On the use of Stress Information in Speech for Speaker Recognition, IEEE TENCON Conference, pp.1-4.

[3] James Z. Zhang, Nyaga Mbitiru, Peter C. Tay, Robert D Adams. 2009. Analysis of Stress in Speech Using Adaptive Empirical Mode Decomposition, IEEE, 43rd ASILOMAR conference on signals, systems & computers, pp. 361-365.

[4] Sahar E. Bou-Ghazale, and John H. L. Hansen. 2000. A Comparative Study of Traditional and Newly Proposed Features for Recognition of Speech under Stress, IEEE TRANS on Speech and Audio Processing, Vol.8, Pp.429-442

[5] Bozo Tomas and Darko Zelenika. 2000. Determination of Spectral Parameters of Speech Signal by Goertzel Algorithm, IEEE TRANS on Speech and Audio Processing, Vol. 8, pp. 978-982

[6] Milan Sigmund, Spectral Analysis of Speech under Stress. 2007. IJCSNS International Journal of Computer Science and Network Security, Vol.7, pp. 170-172

[7] Marchetto, E., Avanzini, F., Flego. 2009. An automatic speaker recognition system for intelligence applications. Proceedings of the European Signal Processing, Glasgow, pp. 1612–1616

[8] Selvan, K., Joseph, A., Anish Babu, K.K. 2013. Speaker Recognition System for security applications. In: IEEE Recent Advances in Intelligent Computational Systems (RAICS), pp. 26–30

[9] YANG Shou-jian,SHEN Yi-bo, YANG Zhong, LI Hong (Faculty of Information Science and Engineering, Ningbo University, Ningbo 315211,China). 2011. The Design of Real-time Spectrum Analysis Based on FPGA and C8051F020 [J]; Computer Knowledge and Technology.

[10] U. Zong-fu,CAI Ming-shan, CHENRi-xin(College of Electrical and Information Engineering, Hunan University of Arts and Science, Changde, 415000,China). 2011. Research and Realization of Abnormal Noise Recognition System Based on Short-term Treatment [J]; Chinese Agricultural Mechanization.