DESIGN AND DEVELOPMENT OF VHDL LOGIC FOR INTERFACE CONTROLLER UNIT

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Abstract: The objective of this project is to Design and Developing the VHDL Logic for "Interface Controller Unit". Interface Controller Unit is a part of ESM Receiver applications. Two important interfaces provided by Interface Controller Unit to any ESM Receiver are Gyro Interface and Radar's Interface. These interfaces are very essentially required by any ESM system as part of its functionality.

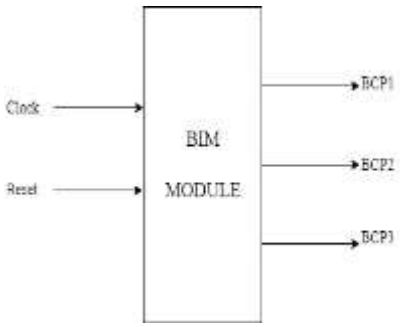
The VHDL Logic required for Gyro and Radar Interfaces will be designed & developed in two modules, Gyro interface Module (GIM) and Blanking Interface module (BIM) respectively as under:
The functionality of receiving the Gyro inputs from platform and measuring & providing the corrected Gyro output data to ESM System will be implemented in Gyro Interface module (GIM).
As part of Radar Interface, the Interface Controller receives the trigger information from onboard radars and generates the ESM Receiver control pulses with respect to the band of interest. This functionality is implemented in the Blanking Interface module (BIM).
The project is broadly segregated into two phases. In phase 1, the above said two modules will be designed and developed individually in standalone mode and integration of both the modules will be carried out during phase II. The VHDL Logic developed during phase I & II will be tested for its complete functionality in the simulated environment using Xilinx ISE Software tool.

Keywords: Xilinx platform studio ISE (14.7) Foundation software

I. INTRODUCTION

The objective of this project is to design, developing and implementing the Digital Glue Logic (DGL) in VHDL for interface controller sub-system. The interface controller sub-system is a part of ESM receiver applications. Two important interfaces provided by the interface controller to any ESM Receiver are Gyro Interface and radar's Interface.The Digital Glue Logic for both the above modules is to be designed, developed and implemented individually in standalone mode and integration of both the modules using XILINX evaluation platform. Electronic Warfare sub-system is used to protect military resources from enemy threats. EW is defined as a military action involving the use of electromagnetic energy to determine, exploit, reduce or prevent hostile use of the EM spectrum and action which retains friendly use of the EM spectrum.In Electronic Warfare receiver system the electronic support (ES), Electronic Attack (EA) and Electronic protect (EP) are the three techniques that will determine certain operation to be taken for a target detected.The ES will detect & measure the parameters of a target and it does not take any military action.The EA will take certain action depending upon the ES information acquired.The EP system will protect our own electromagnetic signals from the enemy's detection.Interface controller sub-system is part of an ESM receiver. It receives inputs from the On-Board Radars (OBR) and on-board GYRO system. The main purpose of the Digital glue logic is to generate the band wise Composite Blanking Cover Pulses as an input from on-board radars and performing the necessary corrections on Gyro data received from on-board Gyro system.The Blanking cover pulse is a TTL pulse which is to shutoff the ESM Receiver during the on-board radar transmissions, in order to protect the ESM Receiver from high power signals emitted by the on-board radars

II. BIM Module:

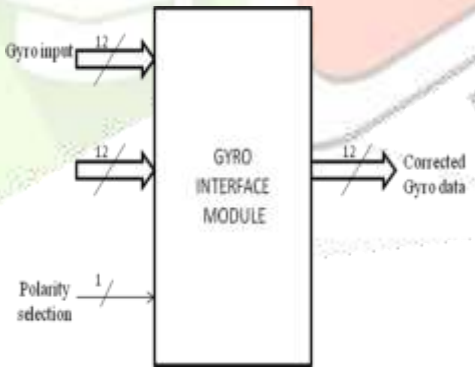


Clock and reset which are external inputs to the module are show in the figure a. The BIM module thus generates the blanking cover pulses. The radar has its own parameters in system itself the parameters such as pulse width(PW),pulse repetitive interval(PRI),advance delay, delta delay, pulse width of main pulse transmission (MTP),delay of MTP. The internal logic has to generated to get the BCP's. The internal top module has two components and is shown in the figure

- MTP module
- BCP module

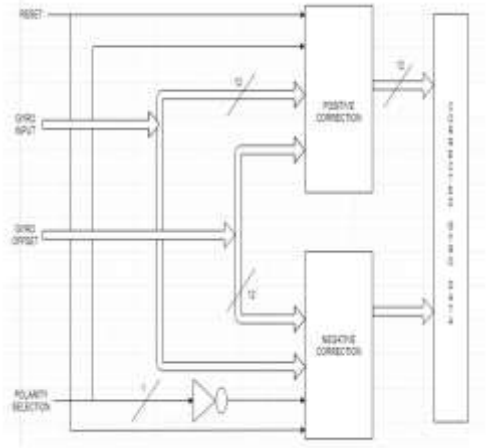
The clock and reset pins are used for free running clock generator. The inputs for simulator for BIM are clock and reset and the outputs are pre-trigger (PT) and Main Transmission pulse (MTP) is shown in figure below.The parameters such as pulse width (PW), pulse repetitive interval (PRI) of PT pulse and PW and delay of MTP pulse are fixed. The parameters are PW of PT, DELAY and PW of MTP is 4 bits.The PT is generated with clock, reset and enable signals and with fixed parameters. The PT is generated with fixed parameters such as PW and PRI. The PW period is HIGH and PRI period is LOW.The MTP PULSE is generated with taking reference with the PT pulse. The trailing edge of PT is detected then after a certain period a MTP pulse width is transmitted. A delay period is kept LOW after trailing edge is detected. And PW period has some information is kept HIGH. The continuous pulse is repeated with delay and pw of MTP after trailing edge of PT. It also uses the clock generator circuit.The internal block of MTP module for the BIM has clock generator, PT generator block and MTP generator block as shown in the figure.

III. GIM Module:



In GIM module, the Gyro input data is corrected with a gyro offset data. The types of corrections are positive or negative correction. The polarity pin is an input that decides the type of correction to be done. The inputs are gyro input and gyro offset are 12 bits, polarity selection and reset pin. When polarity pin is high a negative correction is done and is indicated by the marker and corrected value is indicated on corrected gyro data output pin which is also a 12 bit value. When polarity pin is low a positive correction is done and is indicated by the marker. When corrected is within the range of specified value then a valid bit is generated which is indicated high on output pin.

INTERNAL BLOCK DIAGRAM GIM:



The inputs are 12 bit data of gyro input and gyro offset. Both inputs are applied to positive correction and negative correction block along with polarity selection pin. The reset is also applied to both blocks.The positive or negative correction of both the gyro inputs will depend upon the polarity selection pin. The positive correction block adds the both the gyro inputs and making required corrections, the corrected gyro data must be within 0 to 360° range.The negative correction block subtracts both the gyro inputs and making required corrections, the corrected gyro data must be within 0 to 360° range. The valid bit is enabled whenever the corrected gyro data is within the 0 to 360° range. The gyro rotates the mind the 360°.

The number of 12 bit combinations are 2^12=4096.

Hence the resolution = 360/4096 =0.087890625.

Each LSB bit position is 0.087890625.

For example: If we add 5° with 358° then we get output as 363° but it should be corrected and the output range should get in within 360°. 3° degree equivalent value in hexadecimal is X"020"

Conversion of angle to 12 bit binary number:

358:

Range value = (358/0.087890625)-1

= 4072

12 bit value of angle = X"FE8"

= 111111101000

5:

Range value = (5/0.087890625)-1

= 56

12 bit value of angle = X"038"

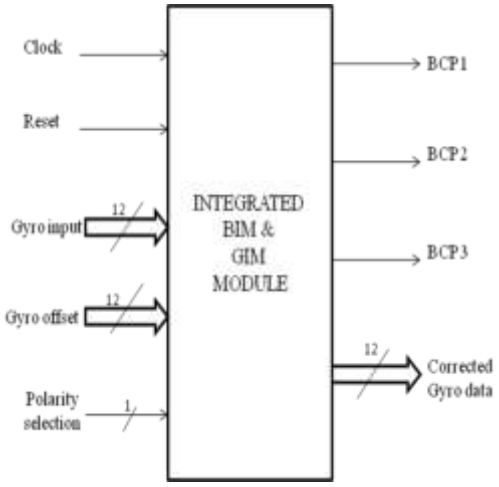
= 000000111000

Adding above two 12 bit numbers we get X"1020" but it exceeds 12 bits i.e., X"FFF" hence X"1020" subtracts X"1000". "Therefore the required result is X"020".

X"020" is the 12 bit value which corresponds to 3°.

The 12 bit value X"020" is also obtained practically.

IV. INTEGRATED BIM &GIM MODULE.



BIM and GIM modules can be integrated using structural design model. The inputs are same for each module as used previously. The outputs of the integrated module are independent The inputs for the integrated module are the same as the ones used in the earlier case. They are Clock, Enable, Reset, Gyro Offset, Gyro Input, Polarity Selection. The outputs BCP 1, BCP 2, BCP 3 and Corrected Gyro data are independent. The integrated module of BIM and GIM can be combined using structural model. The inputs are same for each module as used previously. The clock and reset which generates free running clock.The outputs of integrated module are not related and are independent. Thus the figure indicates the BIM module outputs such as BCP'S generation and GIM module outputs such as corrected gyro and valid bit. In figure, the markers indicate the GIM and BIM outputs.

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