Reducing leakage in a Solar power System

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Abstract: **The main focus of this project is to design and construct leakage reducer which is one of the main parts in solar energy system. The system is comprised in a solar panel, with a lithium battery and a control unit. A lithium battery has an extremely long life with an appropriate charging method, which improves the reliability and stability of the system. It adapts a Maximum Power Point Tracking (MPPT) circuit to take a full advantage of solar energy. In existing system the harvested energy is used twice for processing before it reaches the load circuit. But in proposed system, the usage of solar energy power is monitored and controlled using DC-DC converter. The usage of power to home appliances and remaining power will be displayed in the system. The voltage is continuously monitored by using OFDMA transmitter and receiver. The above technique is simulated and performance is evaluated for different power input using Xilinx ISE.**

IndexTerms **- DC-DC Converter, MPPT, OFDMA transmitter, VHDL**

INTRODUCTION

Solar energy harvesting is an attractive way to improve the power supply system by MPPT (Maximum Power Point Tracking) algorithm. This algorithm is well suited for nano-scale solar energy harvesting system [1]. The available energy at that moment is not sufficient for supplying the power all the time. The DC-DC convertor is used to present optimal impedance for transferring the maximum power. The LDO is used to divide the power required to operate the devices and to reduce the noise and to increase the efficiency [2].Rapid development in computing, communication and integration has resulted in the emergence of ultra-low power system. such designed systems are made to run for several years without the need of battery replacement, because it is inferable to replace the battery again and again. It may also cost high while replacing the battery. As a result, it is necessary to provide the efficient method to store the power for long life, maintenance free operator [3].

To harvest the power continuously, a battery cannot be supported at all time. Therefore, an circuit was designed between the load and the source in order to maintain and regulate power [4]. The basic architecture to reduce the power loss consists of two stages. In first stage DC-DC converter is used boost up the harvested energy is transforming the input level to the maximum level whereas is second stage is used to split up the boosted energy as per the requirement of the load[5]. Harvesting the energy by means of piezoelectric method can improve the efficiency on the usage of the power. The switch only rectifiers reduce the power in every half of the cycle. Maximized by means of MPPT hold block system it consists of a prerogative conditioner to border the PV output to the load [6]. The system consists of high efficiency.

The system old solar PV cell the enter and HBLED as the output which conserves the power inclusive system has been considered and simulated in multi sim which resulted efficiency [7]. The conventional boost convertor the cable of the advantageous for step-up application that make not demand self-same high level voltage gain, mostly directly to the resulting low condition design simplicity. Theoretically the boost convertor static grow tends to be an endless after task series in addition tends unity. However in hands on terms such get is inadequate R passing away in the boost inductor appropriate to its intrinsic resistance most important to the necessary of precise and highcost[8]. The memory chip energy management architecture for solar energy harvesting system is offered which unitizes particular present dc to dc convertor as soon as nearby sufficient ambient energy for maintain convection holder equally key in and load. Linear controller and utilizes plain arrangement pump perception in regulation to keep up regulation [9].

11. **Proposed System**

The proposed architecture comprises of a solar panel in which solar energy is used a source. The harvested solar energy is processed to reduce the power leakage by two blocks. They are converter block, selection block. In converter block, DC-DC converter is used. The input energy which is harvested is boosted up by the DC-DC converter. In selection block, LDO is used to regulator the amount of power needed to the load.

Proposed Architecture

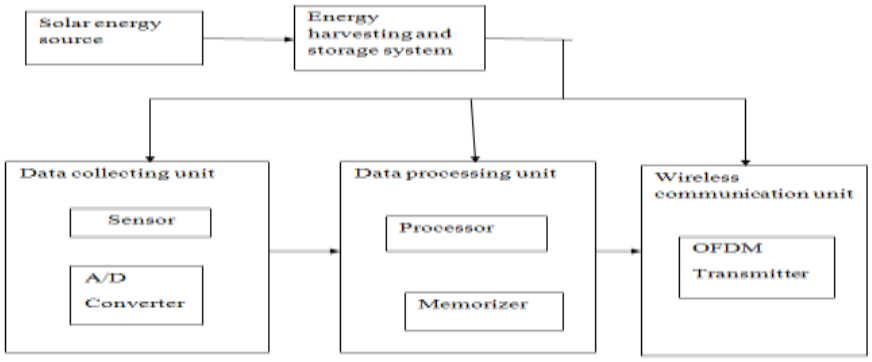


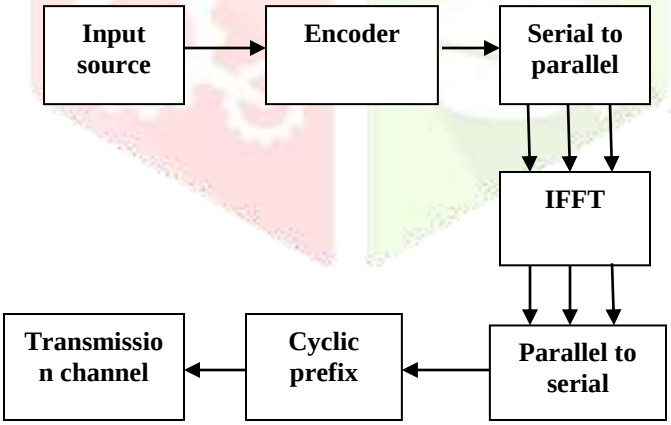
Fig: 1 proposed architecture

The solar energy is the source which is divided into three parts to reduce the power leakage. In data collecting unit, the harvested energy is sensed by the sensor and the incoming analog signal is converted to digital signal by A/D converter. In data processing unit, the signal is processed and is stored in the memorizer. The OFDMA transmitter is used in the wireless communication unit to monitor the usage of the voltage. To transmit the data from DC-DC converter to OFDMA transmitter the following process is done. The data is send to serial to parallel converter which can be used to convert the serial bit of data to the parallel streams. The output of converter is send to IFFT which multiplexed to parallel stream. The data is sent to the cyclic prefix which removes the inter-symbol interference(ISI).The data is send to channel for transmitting and receiving the data. OFDM system such as BPSK modulator and demodulator is designed on XILINX ISE design

Existing system:

The existing system is power management architecture and comprised a switched capacitor boost convertor to bring the output voltage several time higher than the input voltage, current starved voltage control oscillator (CS-VCO) to generate switching frequency for boost convertor. A control unit to regulate the load voltage, a buffer stage to stored the excess energy for future reference and an application delivery the load. Two types of modes storage mode and DC-DC convertor mode. Over All efficient on chip switched capacitor based architecture.

Block Diagram



It deals with function of hardware units in a communication link. The aim is to transmit information from analog source to a analog wireless propagation channel to the link.

Encoder

Encoder the data with code rate 1/3 converts into parallel stream i.e. multiplex into single stream.

Serial to parallel

Serial to parallel conversion. Parallel data can be taken from a register by reading the Q output of each flip-flop. Serial data can be applied to a shift register by applying one bit at time to the MSB input for a shift right register.

IFFT

IFFT 8 point is used to generate TDM symbols IFFT converts the frequency domain into time domain signals. Convert input to number of parallel stream.

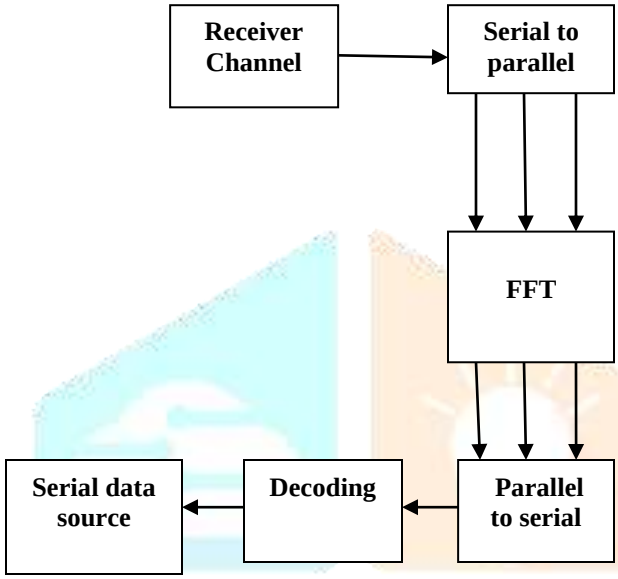
Parallel to serial

A conversion process in which the stream of data elements received all at once is converted and sent as a stream of data at one bit at a time.

Cyclic prefix

It is used to removing the Inter-symbol Interference (ISI) and avoids overlapping signals.

Receiver section



Serial to parallel

Serial to parallel conversion. Parallel data can be taken from a register by reading the Q output of each flip-flop. Serial data can be applied to a shift register by applying one bit at time to the MSB input for a shift right register.

is the inverse of IFFT. FFT converts the time domain signals into frequency domain signals. FFT is used in receiver side to handle this process of signal conversion.

Inverse cyclic prefix

It is the inverse process of cyclic prefix it is a block in receiver side which removes the prefixing of symbols done in the cyclic prefix.

Parallel to serial

A conversion process in which the stream of data elements received all at once is converted and sent as a stream of data at one bit at a time.

Decoder unit

A decoder is a circuit that changes a code into a set of signals. It does the reverse of encoding process.

Circuit implementation

A DC-DC BOOST converter with high voltage gain is employed to step up the output DC voltage from the PV module to a high voltage level without losing the overall efficiency of the system. It is provides high efficiency and increasing the reliability.

DC-DC converter

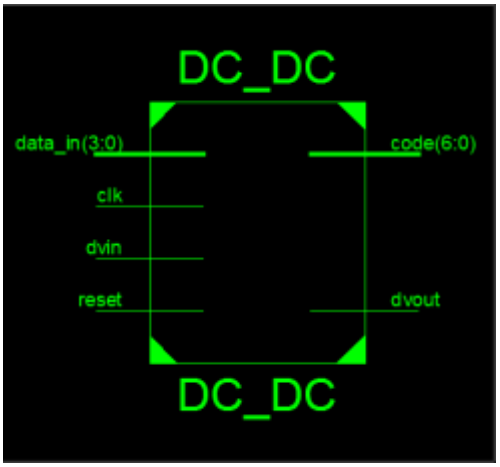


Fig: 4 DC-DC Circuits

DC-DC converter is used to boost up the voltage level. Four input and seven outputs is used in this converter. Show the figure.

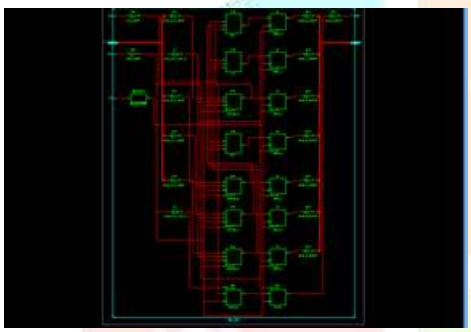


Fig: 5 Circuit implementation

The flip-flop is asynchronously cleared, output low when a power is applied For FPGA devices power on condition are simulated when a global set/reset (GSR)is active GSR default to active- high but can be inverted by adding an inverter in front of the GSR input of the appropriated start up_ architecture symbol.

DC-DC output

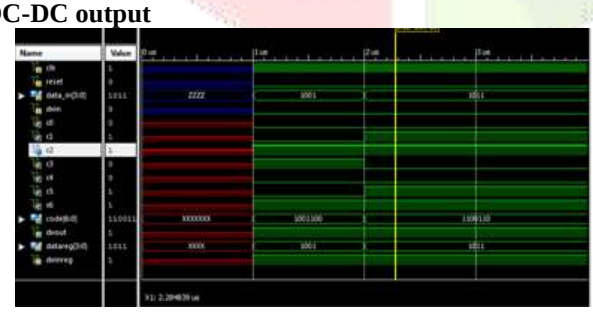


Fig: 6 DC-DC Simulation output

BPSK:

Binary phase shift keying is digital modulation scheme that convey data by changing (or) modulation.

OFDMA Transmitter

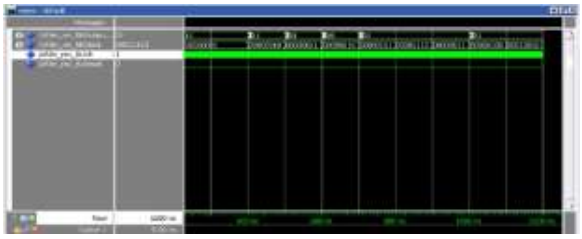


Fig: 7 OFDMA Transmitter output
Data- in=1, reset =0, enable=1, clk=1.

OFDM Receiver

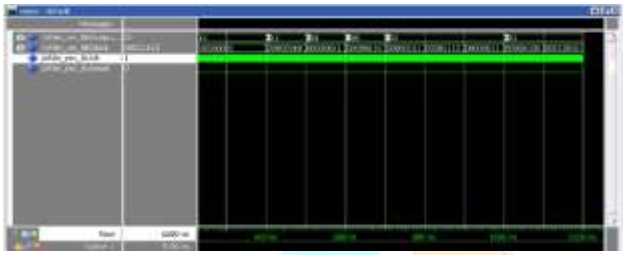


Fig: 8 OFDM Receiver output

Data in =1, reset=0, clock = 0, enable=1.

Output

Name	Power (W)	Used	Total Available	Utilization (%)
Clocks	0.045	2	--	--
Logic	0.000	539	20480	2.6
Signals	0.000	7294	--	--
IOs	0.000	12	320	3.8
DCMs	0.000	0	4	0.0
Total Quiescent Power	0.394			
Total Dynamic Power	0.045			
Total Power	0.439			

Fig: 9 Total output power

Simulation result

Xilinx integrated software ISE is used for modeling and synthesizing design for simulation wave form is obtained for FFT and IFFT using OFDM transmitter and receiver form output by varying the input value.

Conclusion

In this paper a solar energy harvesting system designed using MPPT algorithm is discussed. Leakage reduction by using DC-DC converter is simulated and its performance is discussed. For continuous monitoring and control OFDMA technique simulation is performed in Xilinx ISE and its results show high performance in terms of power leakage reduction. In future actual hardware can be implemented for efficient real time leakage reduction.

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