Automatic Design and Analysis of CMOS D Flip Flop

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Abstract : D flip-flops are simulated using TSPICE in 125nm process technology with BSIM4 MOS transistor model. Latch is an electronic device that can be used to store one bit of information. The D latch is used to capture, or 'latch' the logic level which is present on the Data line when the clock input is high. If the data on the D line changes state while the clock pulse is high, then the output, Q, follows the input, D. When the CLK input falls to logic 0, the last state of the D input is trapped and held in the latch.

IndexTerms - **TSPICE, CMOS, D Flip Flop.**

I. INTRODUCTION

A) Transmission Gate

A transmission gate, or analog switch, is defined as an electronic element that will selectively block or pass a signal level from the input to the output. The solid-state switch is comprised of a p MOS transistor and n MOS transistor. The control gates are biased in a complementary manner so that both transistors are either on or off. In principle, a transmission gate made up of two field-effect transistors, in which – in contrast to traditional discrete field-effect transistors – the substrate terminal (bulk) is not connected internally to the source terminal.

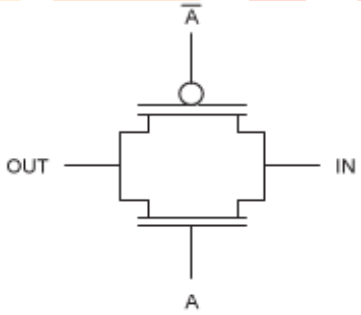

Fig.1 A Simple Transmission Gate

B) B. Pass Transistor

In electronics, pass transistor logic (PTL) describes several logic families used in the design of integrated circuits. It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. Transistors are used as switches to pass logic levels between nodes of a circuit, instead of as switches connected directly to supply voltages. This reduces the number of active devices, but has the disadvantage that the difference of the voltage between high and low logic levels decreases at each stage. Each transistor in series is less saturated at its output than at its input.

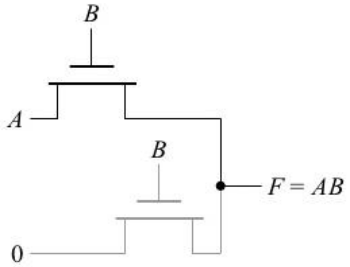

Fig. 2 A Simple Pass Transistor

C) Power Gating

Power gating is a low power technique in deep sub micron technologies. Power gating is performed by shuting down the power for a portion of the design in order to reduce the static(leakage) power in design. Power switch(ps) cell is basic element which is used in power gating technique to shutting down the power for the portion of the design. The ps cell is also known as power management cell. Power gating is used to save the leakage power when the system is not in operation. This is accomplished by adding a switch either to VDD or VSS supply. When the design is power gated it literally means the block is powered OFF. Powering OFF a design block is the most beneficial technique of all the low power techniques because you dissipate near zero power. Near zero because the switching circuit used for implementing power gating still dissipate leakage power even in power gating mode. The control to the power gating switching circuit is generated by the Power gating control block.

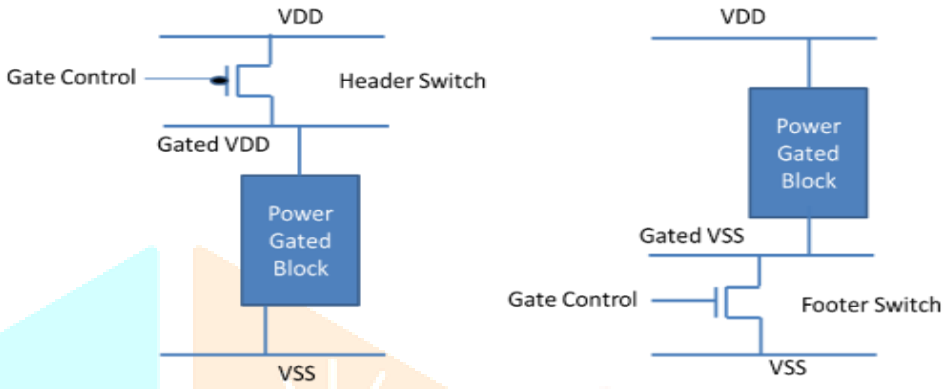

Fig. 3 A Simple Power Gating Circuitry

II. EXISTING SYSTEM

Power consumption and delay are the two major issues in the design of today‘s VLSI based battery operated portable electronic devices. Memory units in these devices are made of flip flops and each flip flop will consume more power in both active and idle conditions. Through this paper we try to explore alternate techniques to implement D flip-flop with the aim of reducing leakage power, delay and to increase the speed. All the different configurations of D flip-flops are simulated using HSPICE in 90nm process technology with BSIM4 MOS transistor models.

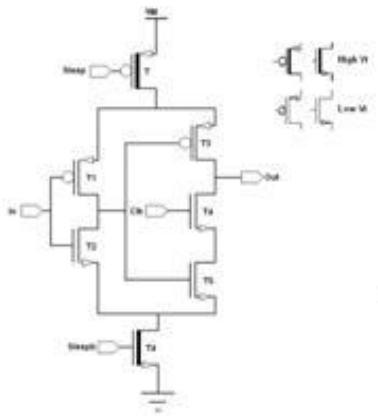

Fig. 4 D FF using MTCMOS

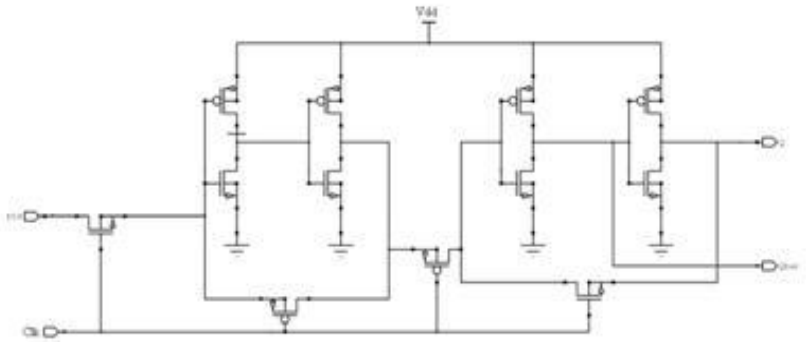

Fig. 5 D FF using pass transistor

CMOS D flip flop implementation

D flip flop is widely used in the design of sequential circuits and memory storage devices. Design of high speed and low power memory elements is desirable for the today’s battery operated portable devices. Three different design of D flip flops are outlined in this section. Design 1 uses MTCMOS technique that uses high Vt PMOS and NMOS devices to minimize leakage current in the silent mode. The circuit is implemented by adding sleep transistors in the pull up and pull down network of the 5T latch circuit is as shown in the fig. 1. When input and CLK is high the transistors T1 and T5 are OFF and a transistor T2, T3 and T5 are ON and causes the output to follow input.

In this circuit high threshold transistors are used for sleep transistors. In the active mode, the high Vt transistors are turned ON to keep the low Vt transistors to operate with low switching power dissipation and minimum delay. In the idle mode high Vt transistors are turned OFF to cut off the conduction path such that any leakage currents arise from internal circuitry can be controlled. Design 2 uses master slave latch configuration to built flip flop using inverters and pass transistors as shown in the fig.2. When CLK is low PMOS loop transistor in the two series connected inverters are ON and other two series inverters are OFF.

The state of the flip flop is changed during falling edge of the clock. Design 3 describes stack based D flip flop using pass transistor shown in the fig 3. By taking width of stacked transistor equal to half of the width of the single transistor the leakage across stacked transistor is lowered compared to the single transistor. The lower transistor in the stacked configuration induces a reverse bias to the below transistor thus increases the threshold voltage which in turn controls the leakage current.

III. PROPOSED SYSTEM

The two transistors, an n-channel MOSFET and a p-channel MOSFET, are connected in parallel with this, however, only the drain and source terminals of the two transistors are connected together. Their gate terminals are connected to each other by a NOT gate (inverter), to form the control terminal. The values at n-gate and p-gate are expected to be opposite to each other. If p-gate is 0 while n-gate is 1, then the value found at source is transmitted to drain. If p-gate is 1 while p-gate is 0, then the connection is broken, so the value at drain is left floating. In all other cases, drain receives an error output unless source is floating, in which case drain is floating as well. The circuits are implemented using the transmission gates and pass transistor logic.

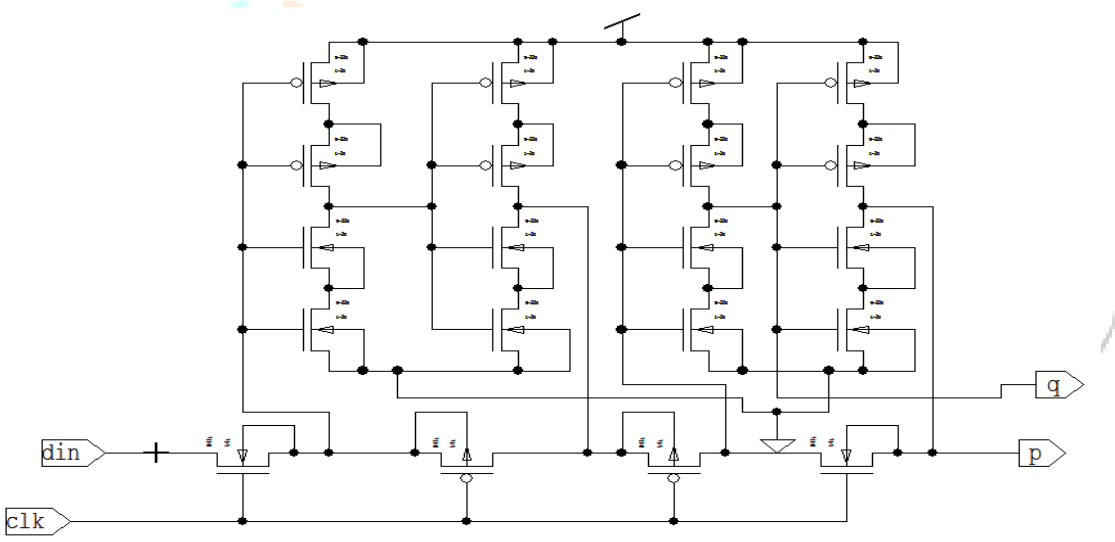

Fig .6 CMOS D latch using pass transistor logic.

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V. RESULT AND OUTPUT

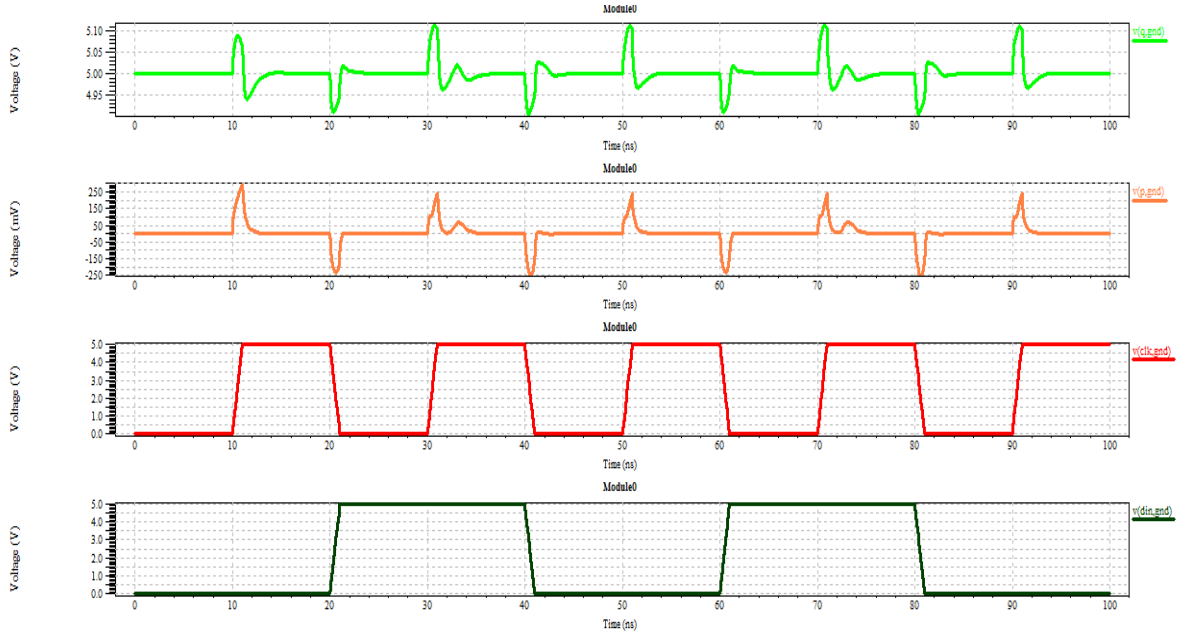

Fig. 6 Waveform for CMOS D latch using pass transistor logic

VI. POWER ANALYSIS

Systems	Max power	Min power	Average power
Proposed system	1.34	2.14	>2.49
Existing system	2.00	2.73	>3.0

VII. CONCLUSION

Thus the CMOS D latch is done using model file ML125 and its output waveform is taken. and its power analysis for pass transistor logic is taken.

Further enhancement can be done by using various low power logic and design in the lower nm technology. The further reduction of the CMOS technology, the transistor behavior is changed and it can be used to analyze various parameters.

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