IMPLEMENTATION OF DRAM USING SELF VOLTAGE LEVEL CONTROLLABLE TEHNIQUE

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Abstract : Today the important is to reduce the power consumption as increasing of the voltage. The more voltage consumption gives the low performance and reliability so that for the high density, reducing cost and chip size area is the main important phenomena in the circuit design in VLSI technology. In CMOS technology DRAM is dynamic random access memory which is high dense memory with high storage data capability. In DRAM the major limitation is lost data due to the discharge of a capacitor and current leakage across the transistors. So that the extra external circuitry provide to continuous refresh to the circuit to hold the data stored in the circuit and increase power consumption. To reduce leakage current in the circuit implementing of DRAM using self-controllable voltage techniques.

Index Terms **- SCVL, Leakage current, DRAM, low power consumption.**

I. INTRODUCTION

The random-access memory is one in which the time required for storing (writing) information and for retrieving (reading) information is independent of the physical location (within the memory) in which the information stored. The bulk of memory chip consists of the cells in which the bits are stored. The DRAM cell stores the bit of information as charge on the cell capacitance[1].

When a cell is storing a,one, the capacitor is charged.

When a cell is stored a 0, the capacitor is discharged to a zero voltage.

Because of leakage effects, the capacitor charge will leak off, and hence the cell must be refreshed periodically. During refresh the cell content is read and the data bit is rewritten, thus restoring the capacitor voltage to its proper value. The refresh operation must be performed every few milliseconds. Dynamic RAM is volatile that is they require the continuous presence of a power supply. The memory access time is the time between the initiation of a read operation and the appearance of the output data. Memory operation is usually taken to include both read and write.

Basically, RAM are two basic types SRAM and DRAM. The term SRAM stands for Static Random Access Memory and DRAM stands for Dynamic Random Access Memory.

SRAM is made up of a transistor and DRAM is made up of a capacitor. Therefore an SRAM store the binary bit inform of voltage; 5v represent one and 0v represents zero.

DRAM stores binary bit in form of charge; presence of charge represents 1 and absence of charge (discharge) represent zero.

The charge on the capacitor naturally leaks in few milliseconds. Therefore, a DRAM needs to be recharged (called refreshing a DRAM) periodically generally every 2 milliseconds. For this, a DRAM needs a special refreshing circuit. DRAMs are cheaper than SRAMs and have high packing density. A DRAM consumes less power than a SRAM. They have lower speed than SRAMs. Cheaper DRAM is used in main memory while SRAM is commonly used in cache memory.

I. II. RELATED WORK

II. (A) LOW POWER REDUCING TECHNIQUES

A) Supply Voltage Scaling To reduce the power consumption, the scaling power supply voltage is most effective method [2]. Reducing the supply voltage can significantly reduce the power dissipation that is a quadratic function of the operating voltage.

B) Reducing Effective Capacitance in the circuit When, we are applying the lowering supply voltage the throughput gives loss in the performance which is not acceptable. The low power consumption in CMOS circuits also can effectively the reducing capacitance.

(B) THE SOURCES OF LEAKAGE CURRENT

There are three main sources of leakage current that the designer must minimize. There are the sources/drain junction leakage current, the gate tunnelling leakage and the sub-threshold leakage current through the channel of an OFF transistor. The source/drain junction leakage current from the drain and the source to the substrate is due to the fact that the junction acts like a reversed biased diode when the transistor is off. So that the magnitude of this current depends on the size of the diffusion area of the transistor which depends on the process technology. The gate tunnelling current flows through the gate oxide into the substrate and which is increases exponentially when the gate oxide becomes thinner. It also increases with the increase of supply voltage. If the low power device is in sleep mode then, it is important to control the high-K gate dielectric leakage current. The sub-threshold leakage current is a leakage current from drain to source. It is a diffusion current that is built up by minority carriers in the channel of the MOS device[3].

2.1 DESIGNS OF DRAM CELL

A. **2.1.1 1st TRANSISTOR DRAM CELL**

DRAM is basically design on the basis of the transistor present in the circuit. A DRAM memory cell[18] uses a single transistor [T1] and capacitor [C2] to store a bit of data thus reducing the chip size. Additionally, management input signals like word line (WL), data I/O and bit line (BL) are used. Random access means that the processor will access any part of the memory at random instead of having to proceed sequentially. In figure (a) shows 1T DRAM cell circuit.

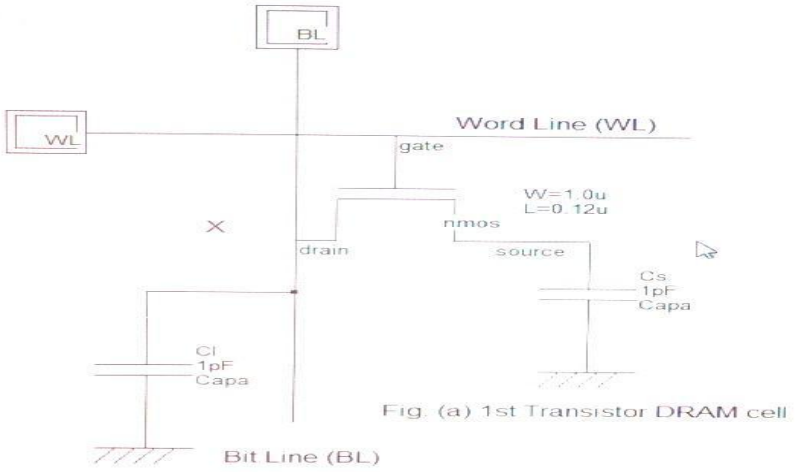

Fig. (a) 1st Transistor DRAM cell

2.1.1.1 1T DRAM WORKING

Fig. (a) Show schematic of 1T DRAM in which the read and write operation is performed. The steady-state voltage: Vc= VDD –VT

Read operations:

(i) First we making the Cl=Vdd/2 because DRAMs, a voltage of +VCC/2 across the capacitor is required to store a logic one; and a voltage of -VCC/2 across the capacitor is required to store a logic zero.

(ii) For read operation we are providing the word line WL=1 then the transistor M1 becomes ON .

(iii) Cs is precharged capacitor then it will share its voltage to the node X .

(iv) If we don't know the capacitor Cs is consuming voltage, it means depending on whether a "1" or "zero" is stored in the cell.
So that, if Cs=1 then it will share its voltage to node X the collectively voltage V>>Vdd/2 & this is the voltage of BL so the output is sending to sense amplifier we will get as output =1
if Cs=0 then collectively voltage becomes V<<Vdd/2 then the output getting sense amplifier after sense BL i.e. output=0

(v) after doing this ,it will refreshing the cell.

Write operations:

(i) BL is act as the input line so that we are providing 0 or 1 as input in DL.
(ii) WL=1 then transistor M1 is ON and also to access the capacitor Cs we provide WL=1
(iii) If BL=1 , Cs=Vdd (charging)
If BL=0 then Cs=0 (discharging)
(iv) Hence the capacitor has tendency to discharge so that the refreshing the cell to maintain the bits.

B. 2.1.2 2nd TRANSISRTOR DRAM CELL

C. The 2T DRAM cell consist of two transistors (as shown in Fig. b, one transistor controls write operation and another transistor controls read operation. It is a simplified version of 3T DRAM cell in which charge is stored in

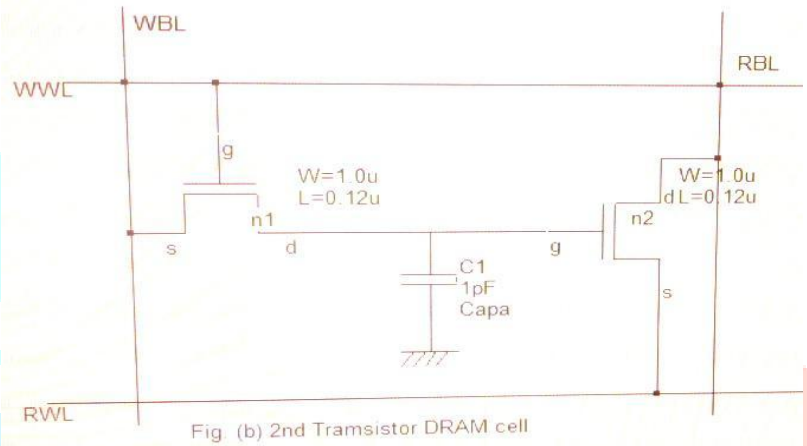

Fig. (b) 2nd Tramsistor DRAM cell

parasitic capacitor. The charge storage node have capacitance equal to sum of parasitic capacitance of drain of T1 and parasitic capacitance of gate of T2. During the write operation write bit line (WBL) is enabled and write word line is set to logic high state so that first transistor turns on and charge is stored into the parasitic capacitor. During the read operation the read word line (RWL) is pulled to lower voltage so that second (read) transistor turns on. When 1 is stored in the memory than a very high current drawn from RBL to RWL. The retention time of 2T dram cell is very less because of the high leakage current. The leakage current between the gate and the source or drain, the leakage current between the gate and the substrate.

The advantages of 2T DRAM cell is that it consumes less area and also the read operation is non-destructive[5] and also the stability issues.

2.1.3 3rd TRANSISTOR DRAM CELL

The circuit diagram of a typical three-transistor dynamic RAM cell consist of column pull-up (precharge) transistors and the column read/write circuitry. Here, the binary information is stored in the form of charge in the parasitic node capacitance C1. The charge stored in the capacitance C1 which depends on the transistor M2 for turned on or off . The pass transistors Ml and M3 act as access switches for data read and write operations.[5] The DRAM cell shows in the fig.(c)

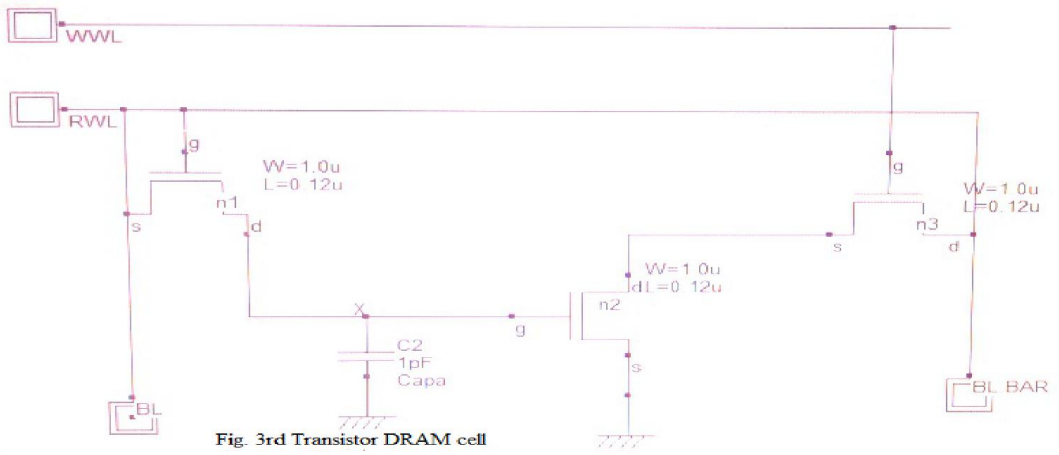

Fig. 3rd Transistor DRAM cell

The cell has two separate bit lines for "data read" and,"data write," and two separate word lines to control the access transistors. The three-transistor DRAM cell operation and its peripheral circuitry is based on a two-phase non-overlapping clock scheme. Here also, the read operation is non-destructive and relatively fast.3T DRAM cell consumes less area as compare to 4T DRAM cell. The 3T DRAM cell has highest retention time as compare to other DRAM circuits so it is widely used in on chip memory system. [9].

D. **2.1.4 4th TRANSISTOR DRAM CELL**

E. This DRAM cell design consists of four transistors. One transistor is used as a write transistor, the other as a read transistor. Data in DRAM is stored in the form of charge at the capacitance attached with the transistor structure. There is no current path to the storage node for restoring the data; hence data is lost due to leakage with the period of time. Read operation for the 4T DRAM cell is non-destructive, as the voltage at the storage node is maintained. The basic DRAM cell shows in fig. d. 4T DRAM cell has least read access time as compare to 3T DRAM and 2T DRAM cell. 4T DRAM cell consumes less time to read the stored data.[10]

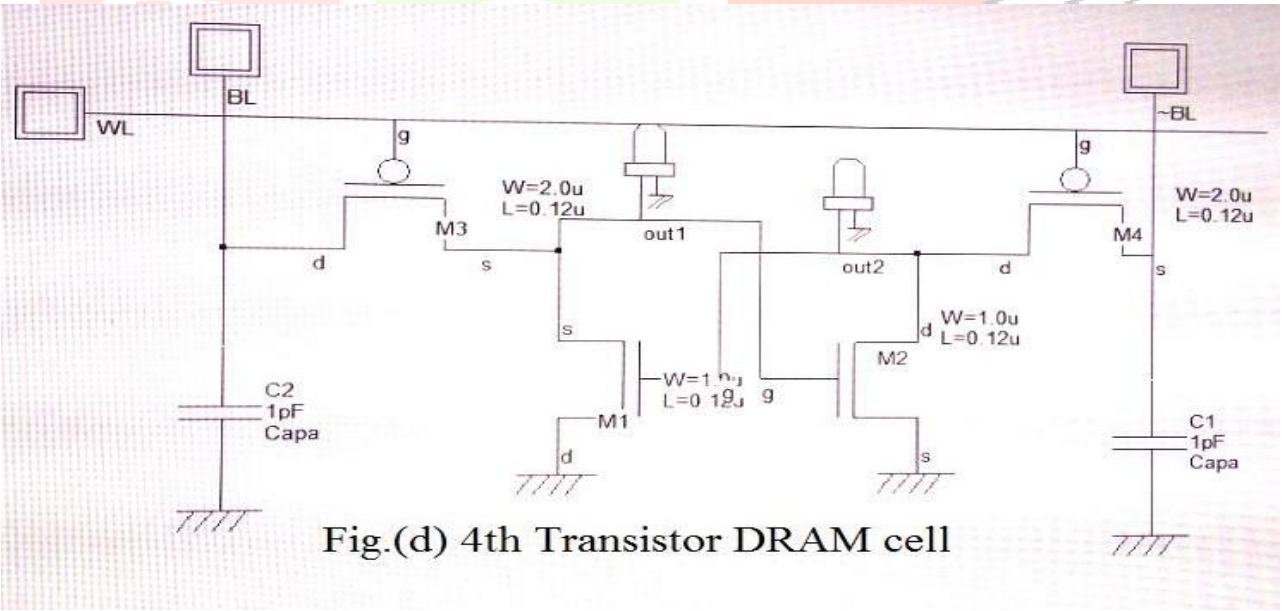

Fig.(d) 4th Transistor DRAM cell

III. PROPOSED WORK

3.1 SELF-VOLTAGE LEVEL CONTROLLABLE TECHNIQUE

The DRAM array is designed using a pair of inverter at the VCC and GND terminals. Such an arrangement is called as self controlled voltage technique. It is implemented such that it reduces the amount of power consumption by allowing the transistors to swing between safe voltage values to prevent excess power consumption. SCVL is an effective technique to reduce the leakage current by controlling the voltage supplied to the DRAM array. As the leakage current reduces, the power dissipation across the transistors is also reduced significantly.[7]

By using the self-controllable voltage level reduce the leakage current in the DRAM.In the Self-controllable voltage level technique used an NMOS and PMOS that is connected in the bit line and output and controlling by using a world line.

After that controlling the leakage current in the circuit the SVL circuit is connected in upper and lower side. The correlation of the circuit is obtained by row and column matrix using cells and also the layout & circuit diagram design by micro wind & DSCH. The layout of any circuit to be manufactured by Using a particular process must confirm to a set of geometric rules which are generally called a layout design rules. These rules usually specify the minimum allowable line width for physical objects on a chip such as metal, and poly silicon interconnects or diffusion area, minimum feature dimension and minimum allowable separation between two such features. The layout modifications are usually concentrated on the width to length ratio of the transistors (transistorizing). The transistor size is change, and the leakage current is affected. The Implementation of the DRAM with self-controllable voltage level reduce the leakage current by varying the voltage.

IV. CONCLUSION

In this paper we have to discuss about implementation of DRAM by using different designs and the how to reduce the leakage current and the leakage current sources which is helpful in reducing the leakage current in the circuit. The leakage of current is occurring due to the dynamic in nature because the capacitor is responsible to store the data. So need to refreshing the cell periodically that's why DRAM is used as cache memory & over it small size, less complex circuit is the bright side to design. By controlling voltage level we can reduce the leakage current as possible as low.

V. ACKNOWLEDGMENT

I would like to thank my Prof. K. S. Solanki sir, for the guidance, fully supporting encouragement throughout the project.

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