LOW AREA LFSR-BASED TEST PATTERN GENERATOR FOR BIST ARCHITECTURE

[1]B.JAMUNA, [2]B.NIREESHA
[1]Assistant Professor, Dept of E.C.E, Teegala Krishna Reddy Engineering College, Telangana, India.
[2]Assistant Professor, Dept of E.C.E, Teegala Krishna Reddy Engineering College, Telangana, India.

Abstract:Basically, to reduce the power consumption in devices, long life batteries are used in battery operated devices. As we know that during testing when the device's normal functioning mode is off then the dissipation of power is approximately 200% more than that of normal functioning mode. So to minimize the concerned power at testing mode a new design is proposed. In this paper we discuss about the design of "Test Pattern generator" for testing the circuits. In this test pattern generator we use gray code generator with modified clock scheme. This circuit generates exhaustive set of test patterns with hamming distance between two consecutive sets. So from this we can observe that the dynamic power consumption is minimized because of increase in switching activity of the transistors at gate level. At last compared to existed system, the proposed system minimizes more power consumption.

***Index Terms*-Dynamic power, Test Pattern Generator, Linear-feedback shift register (LFSR)-based test generation, multi cycle tests, test compaction, test data compression.**

I. INTRODUCTION

Between the scan-in and scan-out operations of a test, a single cycle test has a single functional clock cycle, while a multi cycle test has one or more functional clock cycles. Their effectiveness for test compaction was demonstrated and results from the following observations. During a functional clock cycle of a test, the combinational logic of the circuit receives an input pattern that can be used for detecting faults. A larger number of functional clock cycles allows more faults to be detected. As a result, a multi cycle test may detect more faults than a single-cycle test. With more detected faults for every test, the number of tests is reduced. This reduces the number of scan operations that a test set requires. With fewer scan operations, the test data volume and test application time are reduced.

The fact that each test consists of more functional clock cycles has a negligible effect on the test Application time when the number of functional clock cycles is bounded. The test data volume is independent of the number of functional clock cycles if the primary input vector is kept constant during a test. This is a common requirement to address tester limitations that prevent the primary input vector from being changed during a test.

The generation of multi cycle tests for test compaction becomes more complex when test data compression is used. In one of the commonly used test data compression methods, a test is compressed into a seed for a linear-feedback shift register (LFSR). The on-chip decompression logic uses the LFSR to apply the test to the circuit. A seed is typically computed based on an incompletely specified test cube by solving a set of linear equations that relate the bits of the seed with the specified values of the test cube. With this process, optimizing a multi cycle test <*pi, vi, li*>to increase the number of faults it detects requires a seed to be recomputed after every step that modifies the test, and some modifications of the test cannot be accepted because a seed does not exist for the modified test.

Motivated by these observations, the goal of this paper is to develop a procedure for computing seeds for LFSR-based generation of multi cycle tests that are effective for test compaction. To avoid sequential test generation, the procedure uses a single-cycle test set similar to and optimizes the multi cycle tests to increase the numbers of faults they detect. In contrast to the procedure optimizes the compressed multi cycle tests in order to avoid producing tests for which seeds do not exist.

A compressed multicycle test is represented as *ti*= <*si, vi, li*>, where *si*is a seed that produces the scan-in state *pi* of *ti*. For simplicity, and since the number of primary inputs is typically significantly smaller than the number of state variables, a seed is computed for the scan-in state *pi*. The primary input vector *vi*is stored separately. This is consistent with the approach. The number of functional clock cycles *li* does not need to be stored for every testif tests with equal numbers of functional clock cycles are stored and applied consecutively.

To achieve the goal of producing compressed multi cycle tests that are effective for test compaction, the procedure described in this paper optimizes the seed *si*, the primary input vector *vi*, and the number of functional clock cycles *li* together to increase the number of faults that the test detects. By considering the seed *si*directly, the procedure optimizes the scan-in state *pi*, and avoids modifications of *pi* for which a seed does not exist. Moreover, the single-cycle test set that the procedure uses as guidance does not need to be compressed. To accommodate this case, the procedure initializes the seed *si*randomly, and not based on the scan-in state *qi* of a single-cycle test. It is thus possible to use a compact single-cycle test set that is not constrained by the LFSR.

The possibility of optimizing a seed *si*was used to modify seeds that produce fault detection tests into seeds that produce diagnostic tests. The modification of a seed *si*is implemented in by complementing bits of *si*one by one, and re-computing the test *ti* that the LFSR produces. A bit complementation is accepted when *ti*satisfies certain objectives. In the procedure described in thispaper, bits of *si*and *vi*, as well as thevalue of *li*, are modified together in order to produce an effective multicycle test. The target faults in this paper are single stuck-at faults. The procedure is developed assuming that an LFSR is given. In this paper we describe about the modified binary search process to select an LFSR out for a given set of available LFSRs.

II. EXISTED SYSTEM

This section describes the computation of a compressed multi cycle test set based on a single-cycle test set *W*1. The test set *W*1 is not producible by an LFSR with a limited number of bits. With a bound *L*MAX on the number of functional clock cycles in a test, the multi cycle test set is denoted by T_{LMAX}.

The procedure initially assigns *TL*MAX = ∅, and includes in a set *F*all the target faults that are detected by *W*1. The procedure constructs *TL*MAX by performing *L*MAX iterations over the tests of *W*1. The iterations differ in the initial target *L* for the number of functional clock cycles in a test. The procedure considers *L* = *L*MAX, *L*MAX − 1, . . . ,1 in order to achieve the following goals. By considering higher values of *L* earlier, the procedure gives a precedence to the computation of multi cycle tests with larger numbers of clock cycles. Such tests allow more target faults to be detected, thus contributing to test compaction. By considering all the values of *L* down to 1, the procedure ensures that single-cycle tests will be included in *TL*MAX if this is necessary for detecting some of the faults.After considering all the values of *L*, the procedure performs forward-looking reverse order fault simulation in order to remove unnecessary tests from *TL*MAX.

Several features of the procedure are illustrated by the following example. The example uses a 24-bit primitive LFSR for ITC-99 benchmark *b*07. The test set *W*1 consists of 52 tests, and it achieves a 99.92% single stuck-at fault coverage (the remaining faults are undetectable). The procedure is applied with *L*MAX = 8. The multi cycle tests that the procedure constructs with*L* = 8, 7, 6, and 5. The procedure terminates after considering *L* = 5 since all the target faults are detected.A higher fault coverage implies that fewer faults remain to be detected. The procedure does not compute a multi cycle test based on every single-cycle test. So, a new system is proposed which is discussed in below section.

III. PROPOSED SYSTEM

The proposed design comprised of a gray code generator and modified clock. The gray code generator takes care of generation of all sets of pattern i.e. given n bit input the number of patterns will be 2n, where n corresponds to number of bits involved. The modified clock will minimize the use of clock. Since the pattern generator used is one of the sequential circuits designed so far, each flip flop is clocked sequentially. A normal clock remains active throughout the process but a modified clock will be active only for that flip flop of the design where any event is taking place i.e. either logic 0 is changed to logic 1 or vice versa. From below figure (1) & (2) we can observe that schematic diagram of gray code generator and modified clock scheme module.

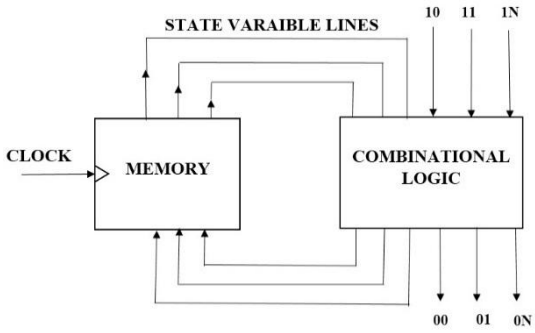

Fig. 1. Gray code generator

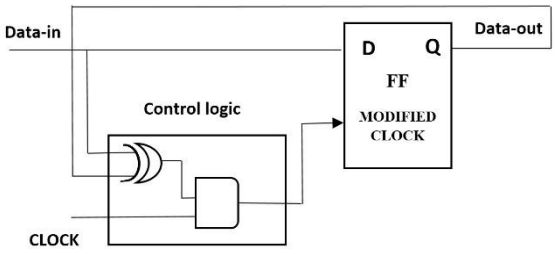

Fig. 2. Modified block scheme model

This modified clock is used with each of the flip flop being involved. The result and discussion section will show both test pattern generator without modified clock scheme as well as test pattern generator with clock scheme. So from below figure (3) we can observe the Standard LFSR with modified clock scheme.

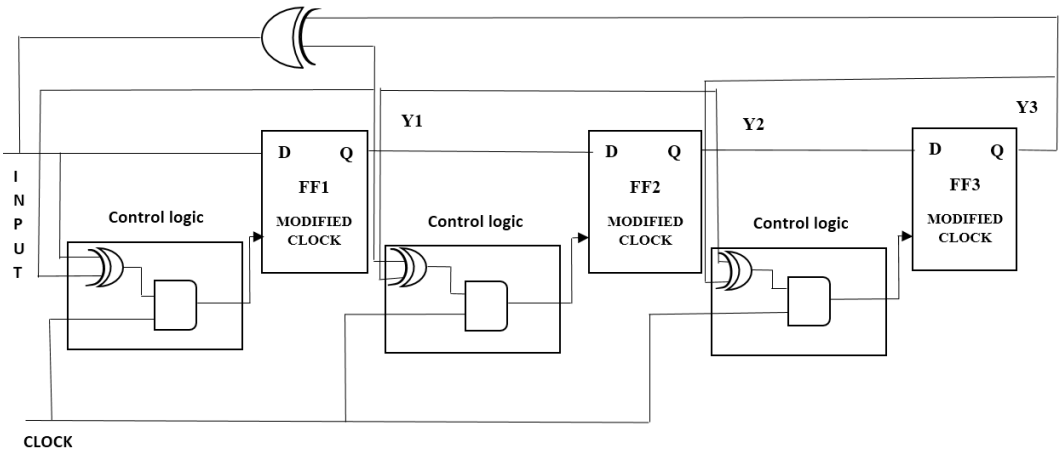

Fig. 3. Standard LFSR with modified clock

IV. RESULTS

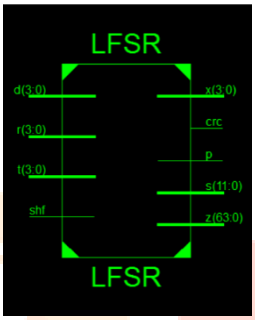

Fig. 4. RTL schematic

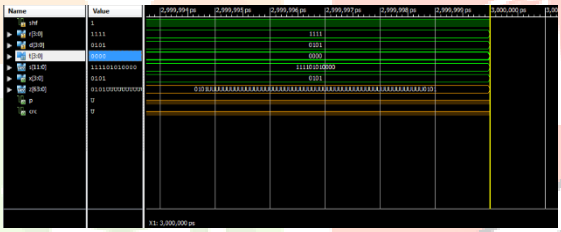

Fig. 5. Output waveform

V. CONCLUSION

From proposed system it can be said that the dynamic power as well as the total power dissipated has reduced to a great extent with the use of the modified clock module. This test set does not have to be applicable using an LFSR with a limited number of bits. The result may vary with the increase or decrease in the number of inputs. The proposed system will adjusts an initially random seed, the primary input vector, and the number of functional clock cycles of each multi cycle test to detect the largest possible number of faults. At last it consumes less power compared to exist one.

REFERENCES

[1] M. Pallavi, "Low Power Testing Using Re-Configurable Johnson Counter And Scalable SIC Counter", IEEE ICCSP conference 2015.

[2] R.C. Ravishankar Reddy and V.Sumalatha,, " Implementation Of Area And Power Efficient Built In Self-test Pattern Generator", IEEE WISPNET conference 2016.

[3] B. Michael L. and A. Vishwani D., Essentials of Electronic Testing for digital, Memory and Mixed Signal VLSI Circuits, Kluwer Academic Publishers (2000).

[4] N. Lubna and C. Tarana A., "Design of Low Transition Pseudo-Random Pattern Generator for BIST Applications", International Journals of Computer Applications, Volume 87, number 15, February 2014.

[5] K. Arun," Design of Low Power Test Pattern Generator For Built In Self- Test (BIST) Circuits", International Journal of Technical Research and Applications, Volume 4, PP.210-214, June 2016.

[6] S. Abdallaitf, Abu-Issa, T. Iyad K. and G. Wasel T., " SR-TPG: A Low Transition Test Pattern Generator for Test-per-Clock and Test-per-Scan BIST", IEEE 10th International Design & Test Symposium, 2015.

[7] M. Puezko, V.N. Yarmolik, "Two-pattern test generation with low power consumption based on LFSR", Information processing and security systems, Springer-Verlag, 2005, pp. 159-166.

[8]K.Jayasheeli and S.Maria Antony, "Low Power Test Pattern Generation of Logic Built in Self-Test", International Journal of Latest Trends in Engineering and Technology, Volume 6, November 2015

B.JAMUNA present working as Assistant professor in Teegala Krishna Reddy Engineering College. Completed M.Tech degree in VLSI System Design from TRR Engineering College, patancheru, JNTU, Hyderabad in 2010 and received B.Tech degree in Electronics and Communication Engineering from SVITS, mahabubnagar JNTU, Hyderabad, in 2007. Research interests include Digital, wireless communication, VLSI and signal processing.

B.NIREESHA present working as Assistant professor in Teegala Krishna Reddy Engineering College. Completed M.Tech degree in VLSI System Design from ATRI, uppal, JNTU, Hyderabad, in 2014 and Received B.Tech degree in Electronics and Communication Engineering from SVECW, Bheemavaram, JNTU, Kakinada in 2010. Research interests include Digital, wireless communication, VLSI and signal processing.