Single Phase Multilevel Inverter By Using Sinusoidal Pulse Width Modulation Technique

MURALI DASARI  
Associate Professor  
Department of Electrical & Electronics Engineering,  
Geetanjali Institute of Science & Technology,  
Gangavaram;Nellore,Nellore(Dt); A.P,India

MALLI SUMAN  
PG Scholar  
Department of Electrical & Electronics Engineering,  
Geetanjali Institute of Science & Technology,  
Gangavaram;Nellore,Nellore(Dt); A.P,India

Abstract: In this project, a novel multilevel inverter is proposed. The proposed multilevel inverter generates seven levels AC output voltage with the appropriate gate signals design. Also, the low pass filter is used to reduce the total harmonic distortion of the sinusoidal output voltage. The switching losses and the voltage stress of power devices can be reduced in the proposed multi-level inverter. The operating principles of the proposed inverter and the voltage balancing method of input capacitors are discussed. By using resonant switching capacitor converter, the voltage balance of input capacitors is achieved. Sinusoidal pulse width modulation is used to control the multilevel inverter.

IndexTerms – Multilevel inverter, Sinusoidal Pulse Width Modulation,

I. INTRODUCTION
Now a days many industrial applications have begun to require high power. Some appliances in the industries however require medium or low power for their operation. Using a high power source for all industrial loads may prove beneficial to some motors requiring high power, while it may damage the other loads. Some medium voltage motor drives and utility applications require medium voltage. The multilevel inverter has been introduced since 1975 as alternative in high power and medium voltage situations. The multilevel inverter is like an inverter and it is used for industrial applications as alternative in high power and medium voltage situations.

The need of multilevel converter is to give a high output power from medium voltage source. Sources like batteries, super capacitors, solar panel are medium voltage sources. The multi level inverter consists of several switches. In the multi level inverter the arrangement switches angles are very important. Problems can be reduced in multilevel inverter are increases no of voltage level which leads to better voltage waveforms. Reduces switching stresses on the device due to the reduction of step voltage between the levels.

In this project, a novel multilevel inverter is proposed. The proposed multilevel inverter generates seven levels AC output voltage with the appropriate gate signals design. Also, the low pass filter is used to reduce the total harmonic distortion of the sinusoidal output voltage. The switching losses and the voltage stress of power devices can be reduced in the proposed multi-level inverter. The operating principles of the proposed inverter and the voltage balancing method of input capacitors are discussed. By using resonant switching capacitor converter, the voltage balance of input capacitors is achieved. Sinusoidal pulse width modulation is used to control the multilevel inverter.

1.1 EXISTING SYSTEM
In the applications of inverters, the inverters with five level inverter topology can produce output not as the high step-up output voltage and with high number of switches Pulse-width modulation (PWM), is a technique used to encode a message into a pulsing signal. It is a type of modulation. Although this modulation technique can be used to encode information for transmission, its main use is to allow the control of the power supplied to electrical devices, especially to inertial loads such as motors.

1.2 PROPOSED SYSTEM
In this project, multilevel DC-AC inverter is introduced. The proposed multilevel inverter generates seven levels AC output voltage with appropriate gate signal design. Also, the low pass filter is used to reduce total harmonic distortion of sinusoidal output voltage. The switching losses and the voltage stress of power devices can be reduced in proposed multi-level inverter. The operating principles of proposed inverter and voltage balancing method of input capacitors are presented. This multilevel inverter is controlled with sinusoidal pulse-width modulation (SPWM).

The proposed multilevel inverter generates seven levels AC output voltage with the appropriate gate signals design. The low pass filter is used to reduce the input current harmonics. Multi-level inverter concepts and voltage balancing concepts on the input capacitors are proposed. The switching losses and the voltage stress of power devices can be reduced in the proposed multi-level inverter. By combining output voltages in multilevel form, it has advantages of low dv/dt, low input current distortion, and lower switching frequency. The quality of electric power is higher than before. Because of the...
advancement of semiconductor, the specification of power device and power conversion technique is promoted.

2. SEVEN LEVEL INVERTER TOPOLOGY

2.1 OPERATION OF PROPOSED TOPOLOGY

![Fig.2.1 Proposed seven level inverter topology](Image)

The introduced novel topology used in the seven-level inverter. An input voltage divider is composed of three series capacitors C1, C2, and C3. The divided voltage is transmitted to H-bridge by four MOSFET, and four diodes. The voltage is send to output terminal by H-bridge which is formed by four MOSFET. The proposed multilevel inverter generates seven levels AC output voltage with the appropriate gate signals design.

### TABLE-1 Switching Combinations

<table>
<thead>
<tr>
<th>Output Voltage Vdc</th>
<th>S1</th>
<th>S2</th>
<th>S3</th>
<th>S4</th>
<th>S5</th>
<th>S6</th>
<th>S7</th>
</tr>
</thead>
<tbody>
<tr>
<td>1/3Vdc</td>
<td>On</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
<td>On</td>
<td>Off</td>
<td>Off</td>
</tr>
<tr>
<td>2/3Vdc</td>
<td>On</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
<td>On</td>
<td>Off</td>
<td>Off</td>
</tr>
<tr>
<td>Vdc</td>
<td>On</td>
<td>On</td>
<td>Off</td>
<td>Off</td>
<td>On</td>
<td>Off</td>
<td>Off</td>
</tr>
<tr>
<td>-1/3Vdc</td>
<td>Off</td>
<td>On</td>
<td>Off</td>
<td>Off</td>
<td>On</td>
<td>Off</td>
<td>Off</td>
</tr>
<tr>
<td>-2/3Vdc</td>
<td>Off</td>
<td>On</td>
<td>On</td>
<td>Off</td>
<td>On</td>
<td>Off</td>
<td>Off</td>
</tr>
<tr>
<td>-Vdc</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
<td>On</td>
<td>On</td>
<td>On</td>
</tr>
<tr>
<td>0</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
</tr>
</tbody>
</table>

2.2 OPERATION MODES

The required seven voltage output levels (±1/3Vdc, ±2/3Vdc, ±Vdc, 0) are generated as follows:

1) To generate a voltage level \( V_o = 1/3V_{dc} \), \( S_1 \) is turned on at the positive half cycle. Energy is provided by the capacitor \( C_1 \) and the voltage across H-bridge is \( 1/3V_{dc} \). \( S_2 \) and \( S_3 \) is turned on and the voltage applied to the load terminals is \( 1/3V_{dc} \). Fig.2.2.1 shows the current path at this mode. turned on and the voltage applied to the load terminals is \( 1/3V_{dc} \). Fig.4.2.1 shows the current path at this mode.

2) To generate a voltage level \( V_o = 2/3V_{dc} \), \( S_1 \) and \( S_4 \) are turned on. Energy is provided by the capacitor \( C_1 \) and \( C_2 \). The voltage across H-bridge is \( 2/3V_{dc} \). \( S_3 \) and \( S_4 \) is turned on and the voltage applied to the load terminals is \( 2/3V_{dc} \). Fig.2.2.2 shows the current path at this mode.

3) To generate a voltage level \( V_o = -1/3V_{dc} \), \( S_2 \) is turned on at the negative half cycle. Energy is provided by the capacitor \( C_3 \) and the voltage across H-bridge is \( 1/3V_{dc} \). \( S_5 \) and \( S_6 \) is turned on and the voltage applied to the load terminals is \( -1/3V_{dc} \). Fig.2.2.4 shows the current path at this mode.

4) To generate a voltage level \( V_o = -2/3V_{dc} \), \( S_2 \) and \( S_3 \) are turned on. Energy is provided by the capacitor \( C_2 \) and \( C_3 \). The voltage across H-bridge is \( 2/3V_{dc} \). \( S_5 \) and \( S_6 \) is turned on, the voltage applied to the load terminals is \( -2/3V_{dc} \). Fig.2.2.5 shows the current path at this mode.

5) To generate a voltage level \( V_o = -V_{dc} \), \( S_1 \) and \( S_2 \) are turned on. Energy is provided by the capacitor \( C_1 \), \( C_2 \), and \( C_3 \), the voltage across H-bridge is \( V_{dc} \). \( S_5 \) and \( S_6 \) is turned on, the voltage applied to the load terminals is \( -V_{dc} \). Fig.2.2.6 shows the current path at this mode.
6) To generate a voltage level $V_c = 0$, $S_5$ and $S_7$ are turned on. The voltage applied to the load terminals is zero. Fig. 2.2.7 shows the current path at this mode.

Since the voltage deviation causes larger harmonics distortion in the output voltage, voltage balancing circuits are indispensable for the capacitors in the multilevel inverters. By using resonant switching capacitor converter, the voltage balance of input capacitors is achieved. Fig. 5.1 shows the circuit configuration of a unit of the RSCC. The duty cycle of every switch is equal to 50%. The voltage of $C_1$ is higher than the voltage of $C_2$. Since the average current of $C_1$ is higher than that of $C_2$ at one switching cycle, most of the charges flow from $C_1$ to $C_2$. After few switching cycles, the voltage of $C_1$ and $C_2$ are equal. Fig. 5.1 shows the waveforms of the RSCC.

TABLE II: Components Comparison between four different seven-level inverters

<table>
<thead>
<tr>
<th>Input sources</th>
<th>Proposed</th>
<th>Diode-clamped</th>
<th>Capacitor-clamped</th>
<th>Cascaded multilevel</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input capacitors</td>
<td>3</td>
<td>6</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>Clamped capacitors</td>
<td>0</td>
<td>0</td>
<td>5</td>
<td>0</td>
</tr>
<tr>
<td>Power switches</td>
<td>8</td>
<td>12</td>
<td>12</td>
<td>12</td>
</tr>
<tr>
<td>Diodes</td>
<td>4</td>
<td>10</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

TABLE III: Voltage Stress Comparison between four different seven-level inverters

<table>
<thead>
<tr>
<th>Input sources</th>
<th>Proposed</th>
<th>Diode-clamped</th>
<th>Capacitor-clamped</th>
<th>Cascaded multilevel</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input capacitors</td>
<td>$V_o$</td>
<td>$2V_o$</td>
<td>$2V_o$</td>
<td>$V_o$/3</td>
</tr>
<tr>
<td>Power switches</td>
<td>$V_o$</td>
<td>$V_o$</td>
<td>$V_o$/3</td>
<td>$V_o$/3</td>
</tr>
<tr>
<td>Diodes</td>
<td>$2V_o$/3</td>
<td>$3V_o$/2</td>
<td>N/A</td>
<td>N/A</td>
</tr>
</tbody>
</table>

3. VOLTAGE BALANCING CIRCUIT BASED ON RSCC

Conventional switched capacitor converters have an inherent drawback that their efficiency is much decreased as the output current is increased. This inherent drawback is due to a periodical forced charging and discharging operation in the internal switched capacitors accompanied by a large capacitor current, so that their efficiency cannot be increased by decreasing its internal resistance. As a result, conventional switched capacitor converters have been limited to be used with a very small output current. This paper presents some novel switched capacitor converter topologies that use a resonant operation instead of the forced charging and discharging operation. Their advantage over conventional switched capacitor converters is a high efficiency even in a high output current region.
Fig.3.2 shows the configuration of proposed seven-level inverter with RSCC. To apply RSCC at seven-level configuration, two switches $S_{b5}$ and $S_{b6}$, resonant inductor $L_r$, and resonant capacitor $C_r$ are added. In this application, switches $S_{b1}$, $S_{b3}$, and $S_{b5}$ are turned on at the same time; $S_{b2}$, $S_{b4}$, and $S_{b6}$ are turned on at the same time. The duty of each switch is equal to 50%.

compared against the fundamental component of the voltage or current wave:

$$\text{THD} = \frac{\sqrt{V_2^2 + V_4^2 + V_6^2 + \cdots}}{V_1} \times 100\%$$

4.2.2 SPWM

In many industrial applications, Sinusoidal Pulse Width Modulation (SPWM), also called Sine coded Pulse Width Modulation, is used to control the inverter output voltage. SPWM maintains good performance of the drive in the entire range of operation between zero and 78 percent of the value that would be reached by square-wave operation. If the modulation index exceeds this value, linear relationship between modulation index and output voltage is not maintained and the over-modulation methods are required.

Sinusoidal PWM is a type of carrier-based pulse width modulation. Carrier based PWM uses pre-defined modulation signals to determine output voltages. In sinusoidal PWM, the modulation signal is sinusoidal, with the peak of the modulating signal always less than the peak of the carrier signal.

Instead of maintaining the width of the pulses same as in the case of multiple pulse width modulation, the width of each pulses is varied in proportion to amplitude of a sine wave. The gating signals are generated by comparing sinusoidal reference signal with a carrier triangular wave. The frequency of the reference signal $f_r$ determines the inverter output frequency $f_o$, and its peak amplitude $A_r$ controls the modulation index $M$. The number of pulses per half cycle depends on the carrier frequency. This sinusoidal pulse width modulation is commonly used in industrial application.

5. SIMULATION RESULTS

PROPOSED CIRCUIT

Fig.4.1 (a) Ideal sine wave   (b) Distorted waveform

Harmonics have frequencies that are integer multiples of the waveform’s fundamental frequency. For example, given a 60Hz fundamental waveform, the 2nd, 3rd, 4th and 5th harmonic components will be at 120Hz, 180Hz, 240Hz and 300Hz respectively. Thus, harmonic distortion is the degree to which a waveform deviates from its pure sinusoidal values as a result of the summation of all these harmonic elements. The ideal sine wave has zero harmonic components. In that case, there is nothing to distort this perfect wave.

Total harmonic distortion, or THD, is the summation of all harmonic components of the voltage or current waveform.
be extended to any number of levels. The schematic of the cascaded H-bridge seven level inverter and proposed new seven level topology built in MATLAB SIMULINK as shown in fig.5.1.

Fig.5.2 Subsystem from main circuit

Fig.5.4 7-Level output Waveforms

Fig.5.5 Solar Panel output Voltage and Current

Fig.5.3 Triggering Pulses for MOSFET

Problems can be reduced in multilevel inverter

I/p current: Multilevel inverter can draw input current with low distortion.
Switching frequency: Multilevel inverter can operate at fundamental frequency and high switching frequency.

Conclusion

A Seven level inverter with reduced number of power devices is designed.

The reduction of power device is proved by comparing with the traditional structures.
References