Design Of 0.6V Low Power High Gain Single Ended Two Stage CMOS Operational Amplifier

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Abstract : This paper presents the design of high gain, single ended two stage CMOS operational amplifier, For designing the specifications like Gain (Av), Phase Margin (PM),Technology & Optimal dimensions (Channel length & widths), Unity gain frequency (UGF), Operating Voltage, Power consumption (Pc) are plays major role as the design variables. The proposed operational amplifier operates at ±600mV power supply designed using 180nm CMOS technology. The OPAMP designed has two-stages and a single ended output. The gain of the op-amp is 78.396dB with a 60^0 phase margin, UGF of 650 KHz, CMRR 83.092dB and has power dissipation 696nW. Design and Simulation has been carried out in Cadence Virtuoso Spectre simulator.

IndexTerms **- CMOS, NMOS differential pair Op-Amp, Op-amp, Single - Ended, Two stage Op-amp,**

I. INTRODUCTION

Data Converters are the basic block of the CMOS mixed circuits, Recent trends in CMOS Mixed IC design the designer look forward towards low power, since reduced supply voltage decreases battery size and power consumption which results to longer battery life time, low-power CMOS mixed circuits are also advantageous to reduce thermal dissipation. To achieve the low power decreasing the supply voltage is one method, but there exist problems with transistors such as difficult operate them in saturation region. Another concern that draws from supply voltage scaling is the threshold of the transistor. A decrease in supply voltage without a similar decrease in threshold voltage leads to biasing issues [2]. Maintaining all the transistors in sub threshold region with achieving desired specifications is a challenging task to the designer. The unique behavior of the MOS transistors when they are in sub threshold region not only allows a designer to work at low input bias current but also at low voltage [2].

In general mainly three op-amp topologies are used in the design of data convertors they are
(i)Two stage CMOS Op-amp
(ii) Folded Cascode Op-amp
(iii) Telescopic Op-amp.

Table 1 Comparison of Op-Amp Topologies

Topology	Speed	Gain	Power Consumption	Noise	Output Swing
Two-Stage	Medium	High	Medium	Low	Highest
Folded-Cascode	High	Medium	Medium	Medium	Medium
Telescopic	Highest	Medium	Low	Low	Medium

In this paper we considered the conventional two stage CMOS operational amplifier. With design variables as Gain (Av), Phase Margin (PM), Technology & Optimal dimensions (Channel length & widths), Unity gain frequency (UGF), Operating Voltage, Power consumption (Pc). A decrease in supply voltage without a similar decrease in threshold voltage leads to biasing issues [2]. Maintaining all the transistors in sub threshold region with achieving desired specifications is a challenging task to the designer. The unique behavior of the MOS transistors when they are in sub threshold region not only allows a designer to work at low input bias current but also at low voltage. In order to achieve good tradeoff between supply voltage, power consumption, gain and UGF the conventional two stage CMOS operational amplifier with NMOS differential pair is considered and also to maintain good degree of stability.[1]

The organization of this paper is done as Section-I will give Introduction to Op-Amp and different topologies, Section-II describes the design of two stage op-amp, Section-III gives the simulation results and comparison with previously published results, Section-IV concludes the paper.

II. TWO STAGE CMOS OPERATIONAL AMPLIFIER DESIGN

The main objective of this work is to implement the full custom design of high gain single ended low voltage and low power operational amplifier. The design has been made through the scaling of device parameters with the theoretical calculations of optimal dimensions, by maintaining the scaling factor to a minimum value reduced the bias current, and by reducing the supply voltage power consumption is minimized. In this presentation Miller Compensation technique is implemented to maintain the stability, it is the simplest frequency compensation technique which employs the Miller effect by connecting a compensation capacitor C_c across the high-gain stage. And the transistor level schematic of the considered topology is shown in the below Fig.

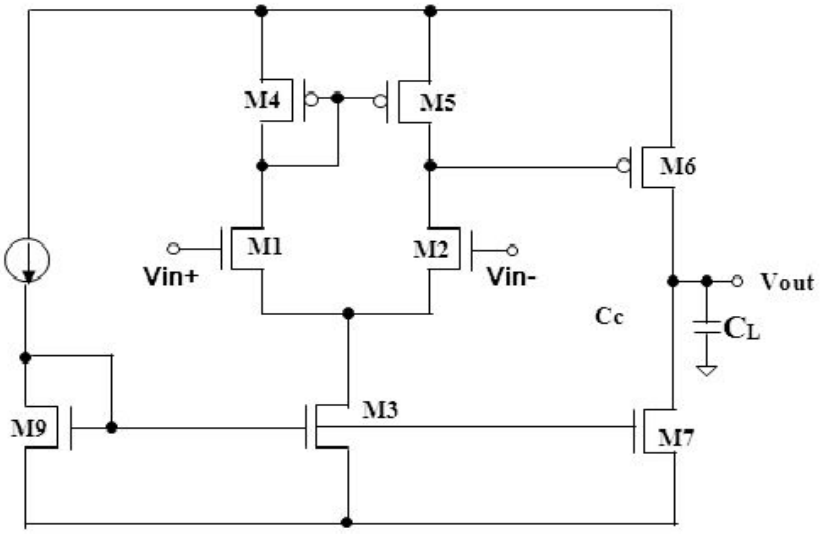

Figure.1: Schematic of Two stage CMOS Op- Amp

In the above transistor level schematic M1, M2 transistor pair forms the NMOS differential pair which is a differential trans conductance stage of the operational amplifier. The M1 & M2 Transistor lengths and widths should be equal and also the dimensions of these two transistors decides the gain of the first stage as,

$$A_{V1} = \frac{g_{m1}}{g_{ds2} + g_{ds4}} \qquad (1)$$

they are also responsible for Gain band width product as

$$GainBandWidth = \frac{g_{m1}}{C_c} \qquad (2)$$

The transistor M6 will decides the gain of second stage such as and the M6 transistor forms the Common source configuration.

$$A_{V2} = \frac{g_{m6}}{g_{ds7} + g_{ds6}} \qquad (3)$$

The overall gain is the product of Av1 and Av2. M3 & M9 forms the current mirror which acts like a biasing circuit of the operational amplifier, M4 & M5 forms the current load. Cc is the millar capacitor for compensation circuitry. the input can be applied at inverting or non inverting terminal of the op-amp.and output is observed at Vout.

The Schematic connected in cadence is shown as

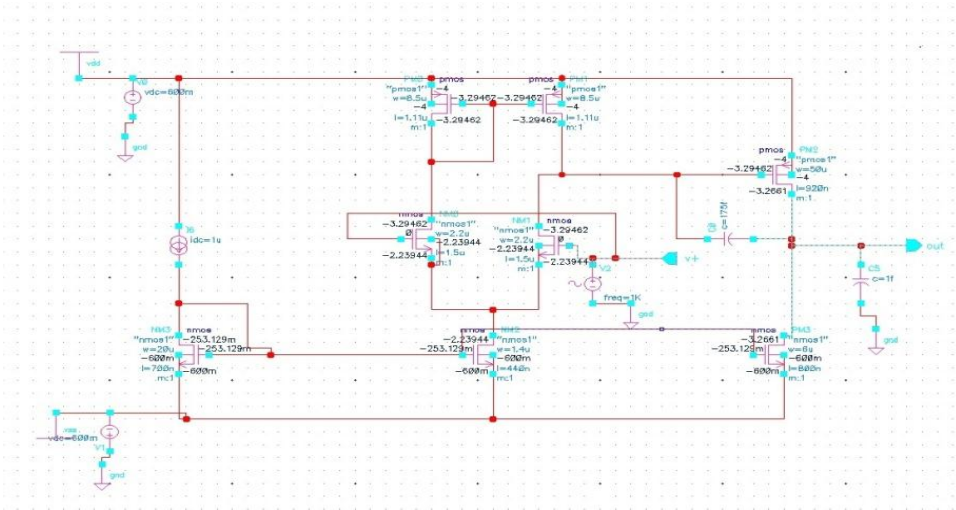

Figure.2: Designed two stage CMOS Op- Amp

III. SIMULATION RESULTS & COMPARISON

The proposed Op-Amp is operated at supply voltages Vdd = +600mV and Vss = - 600mV, Applied input at inverting terminal and observed ouput at Vout. The proposed Op-amp exhibits the Gain(Av) of 78.396dB,with Phase Margin of 60^0, UGF of 650KHz, AC magnitude in common mode is 8.416KV,AC magnitude in differential mode is 589.5mV and the CMRR is 83.092dB with C_c = 175fF & C_L = 1fF the power consumption is 696nW.

Table 2: Comparison of results

S.No.	Parameter	PAPER [2]	PAPER [3]	PAPER [4]	THIS WORK
1	Technology	180nM	180nM	180nM	180nM
2	Power supply	±1.8V	±600mV	±2.5V	±600mV
3	Gain	70dB	23.5dB	52.80dB	78.396dB
4	Power Consumption	19.5µW	1.39µW	0.775mW	696nW
5	UGF	8MHz	379.7 kHz	9.20MHz	650KHz
6	Phase Margin	75degrees	93.8º	-	60^0

IV. CONCLUSION

This paper presented the full custom design of a single ended two stage CMOS Op-Amp. Design technique for this Op-Amp, its calculations and computer-aided simulation results are presented. In the Design of a two-stage Op-Amp the tradeoff (one parameter can lead to degradation of other) of six design specifications are considered. The present work is carried out in Cadence Spectre Simulator with 0.18µm CMOS process at ±600mV supply. The result shows improvement in some key electrical parameter such as Gain, PM, Power Consumption and CMRR and a good tradeoff is observed between the considered six design aspects.

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