COMPARITIVE ANALYSIS OF SRAM CELL TOPOLOGIES USING 65nm TECHNOLOGY

[1]Manish Verma

[1]Assistant Professor
[1]Electrical Engineering,
[1]Kalinga University, Raipur,India

Abstract :The Aim of the Thesis is to obtain low power, low leakage 7T SRAM single ended input and output cell with speed up to good level and minimum area penalty. This paper analyses standard 6T, new 7T SRAM and 8T SRAM (static random access memory) cell in light of power consumption, leakage current and time delay to verify their functionality and robustness at 65nm Technology. The 7T SRAM cell consumes 50%-70% less power during write operation and 30%-60% less power consumption during the read operation. It shows 80% improvement in static noise margin (SNM), 85% improvement in read static noise margin (RSNM) and 45% improvement in write static noise margin (WSNM). Leakage current reduction is 10%-20%. Therefore a single ended input output 7 transistor SRAM cell using 65nm Technology is suitable for low voltage regime.

Index Term **-7T SRAM, leakage current, noise margin, SNM, RSNM, WSNM.**

I. INTRODUCTION

The usage of SRAM is continuously increasing in system-on-chip (SoC) design. Process technology scaling has contributed remarkably in improving the performance and area density of SoC. In order to achieve high density, the SRAM Cell typically utilizes minimum sized transistor. With the result SRAM Scaling has become extremely difficult in the advance technology node (e.g. 65nm, 40nm, 32nm LP CMOS technology). The lowest operational VDD (VDDmin) for embedded memories (SRAM) is limited either by SNMread (Cell stability) or write ability [write margin (WM)]. The random threshold variation in sub-nanometer technologies have resulted in serious yield issues for realizing low VDD READ/WRITE operation with a 6T SRAM Cell. The area of the SRAM Cell is very important because the cell area contributes significantly to the silicon area. The minimum sized 6T SRAM Cell in 65nm technology occupies $0.4um^2$ (Utsumiet al.2005), in 40nm $0.33um^2$ (Yabuuchi et al.2007), and in 32nm $0.124um^2$ (Chang et al.2005).

II. OBJECTIVE

The objective of the thesis is to optimize the power consumption and the leakage current during the read and write operation with minimum penalty in the increase in the area of the new single ended input output 7T SRAM Cell at 65nm Technology and comparative analysis with the existing standard 6T and 8T SRAM Cell. The conventional 6T SRAM Cell has two bit lines and one word line to perform read and write operation. 45% of the power is consumed in the data path and the memory. This means almost half the power is dissipated in this section. If we can reduce the data line or area of the memory then we can save more power.

Following are the objectives accomplished:

i. The new design of the 7T SRAM is taken into consideration in the 65nm Technology in which the cell operates on single bit line instead on the traditional two bit lines in case of 6T SRAM and 8T SRAM Cell, where in case of 8T SRAM Cell a read word line (RDWL) and read bit line (RDBL) is used for each cell so the power dissipation is more here as compared to 6T and 7T SRAM Cell.

ii. Despite of the area penalty in the 7T SRAM Cell the time delay is maintained at the good level.

iii. In compare with the 6T and 8T SRAM the leakage current in the 7T SRAM is reduced considerably despite of the area penalty (because of the extra transistor which is also known as the access transistor).

Abbreviations and Acronyms

SRAM = Static Random Access Memory, DRAM = Dynamic Random Access Memory, CPU = Central Processing Unit, CMOS= Complementary Metal Oxide Semiconductor, LP= Low Power, T= Transistor, nm= nanometer, SNM= Static Noise Margin, RSNM= Read Static Noise Margin, WSNM= Write Static Noise Margin, um= micrometer.

III. SRAM CELL

3.1 WORKING PRINCIPLE

An SRAM (Static Random Access Memory) is designed to fill the two basic needs: to provide direct interface with the CPU at speed not attained by the DRAMs, and to replace in systems that require very low power consumption. In the first role, the SRAM provides cache memory, interfacing between DRAMs and CPU. An SRAM can be accessed in as little as a few nanoseconds (ns) versus 50ns to 80ns for a DRAM. The second application – low power – is found in most equipment where the DRAM refresh current is several orders of magnitude more than the low power SRAM standby current. In low power parts, the access time is comparable to a DRAM.

The SRAM consists of a bi-stable flip flop (back to back connected inverters) connected to two access transistor. The data is latched into the flip flop.

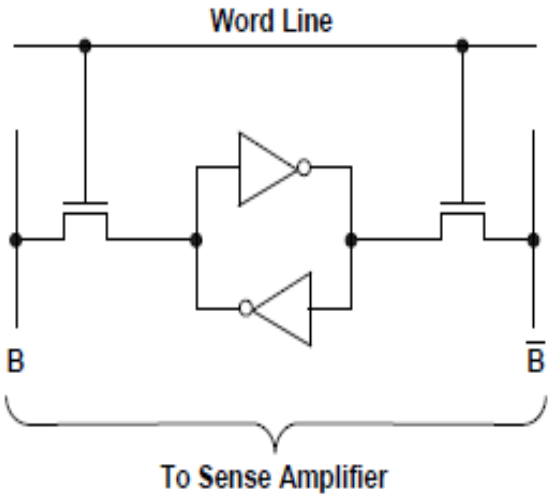

Fig 3.1The SRAM Cell

The SRAM consists of a bi-stable flip flop (back to back connected inverters) connected to two access transistor. The data is latched into the flip flop. The data in SRAM is volatile i.e. the data is lost when the power is removed. However the data does not "leak away" like in a DRAM, so SRAM does not require a refresh cycle.

3.2 THE 7T SRAM CELL

The major disadvantage of 6T SRAM Cell was that most of the power was consumed in the data lines and the loss due to the sub threshold leakage. One of the most important solutions of this problem is the stacking of the MOS. The new 7T SRAM is designed on this basis. An extra access transistor is used in the 7T SRAM cell and only one bit line is used in place of conventional 2 bit lines. In this way total 34% power is saved of the total power consumed in the data lines. This comes with the 11% area penalty in 7T SRAM Cell.

One of the most powerful techniques to reduce the power consumption in the memory design is the low power supply to the memory cell. But the traditional memory cell like 6T SRAM fails to operate at ultra-low voltage supply. Therefore new SRAM cell is designed using 7 transistors which is single ended input/output type.

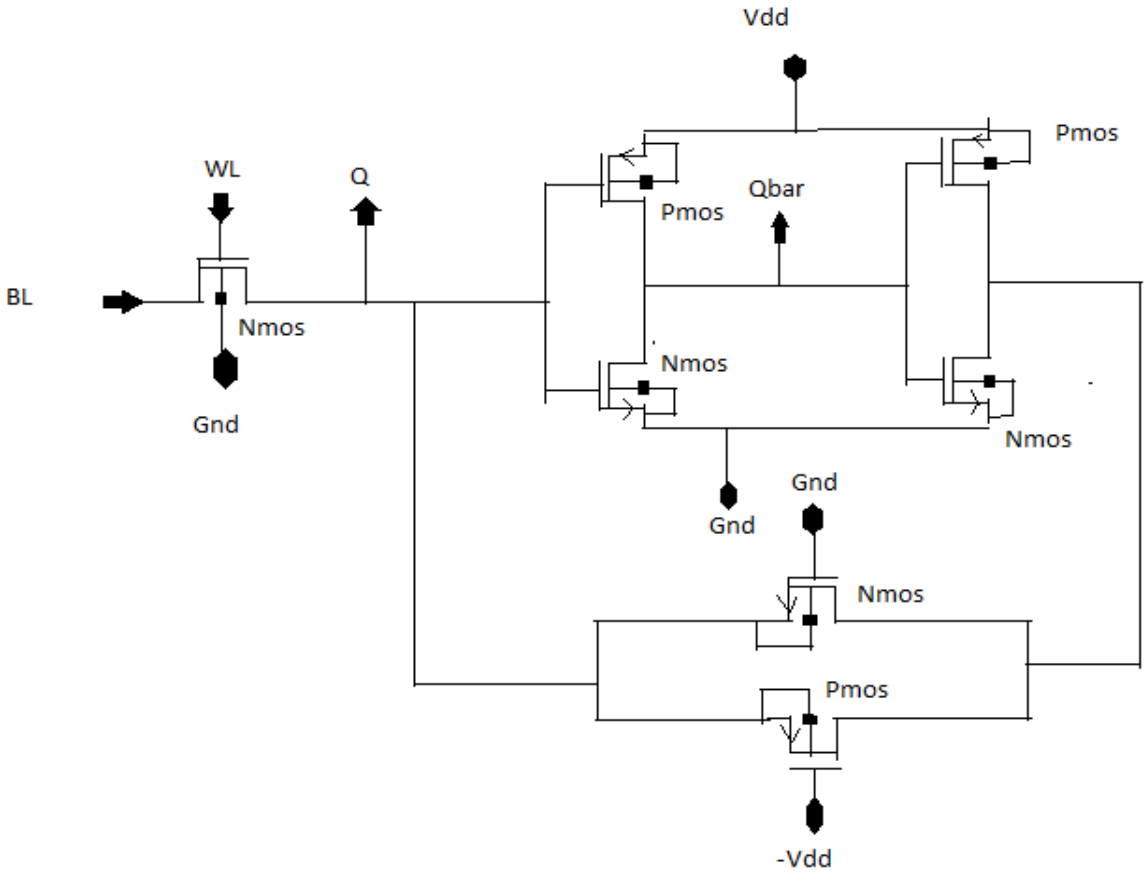

Fig 3.2 single ended input/output 7T SRAM cell

This structure is suitable for ultra-low power applications. This technique reduces power consumption as well as leakage current and improves Signal to noise margin (SNM). This design also reduces the problem of poor write ability of 6T SRAM cell, increased design sensitivity and process variation. This design motivates to design new Nano scale CMOS circuits which can operate at ultra-low voltage regime.

This new cell has only one bit line instead of two bit line as in case of 6T SRAM cell and other old design and has one word line, which can perform both read and write operation. It has one extra read and write access transistors, two inverters connected back to back in the close loop fashion in order to store 1 bit of information and has one transmission gate to provide feedback to the circuit. The word lines are asserted prior to the every read and write operation. In the hold mode operation, the word line is low and a strong feedback is provided to the cross coupled inverter with the help of transmission gate.

Equations:

CR is called cell ratio (CR) or β ratio defined as:

$$CR = (W/L)_1 \ / (W/L)_2$$

Leakage current:

$$I = Io\ Exp\ ((Vgs - Vth)/2\alpha\eta Vt) * \ (1- Exp(-Vgs/2\ \alpha Vt\ )$$

The threshold voltage Vth is calculated as:

$$V_{th} = V_{fb} + 2\Phi_p + \lambda_b / C_{ox}\ (2qN\varepsilon s\ (2\Phi_p + V_{sb})^{1/2} - \lambda_d\ V_{ds})$$

Saturation Region Equation:

$$I_{DSS} = ½\ \mu n\ Cox\ W/L\ (Vgs - Vt)^2\ (1+ \lambda\ Vds)$$

$$\alpha\ + \beta\ = \chi.$$

3.3 Write operation of 7T SRAM Cell

In earlier developed SRAM cells accurate performance of the circuit at ultra-low regime or reduced Vdd, was not possible because of the NMOS access transistor and PMOS pull-up transistor. To solve this problem several write assist circuit and weakening cross coupled inverter circuits has been proposed. In all of that single ended input/output 7T SRAM is very reliable. The write operation of the circuit starts with asserting the bit line to the high logic. This indeed disconnects the feedback connection of the circuit. This operation is performed by the transmission gate with proper write control signal. This makes the charging and discharging operation at the node Q very easy to an equivalent "0/1" level.

The write operation becomes similar to that of the 6T SRAM cell. When we have to store logic high "1" in the memory, the bit line is also raised to high level. This charges the node Q at the high logic level and NMOS of the first inverter and PMOS of the second inverter becomes off. At the Qbar the complement of the Q is stored. The data is present in the memory until the memory is refreshed or the new data is written.

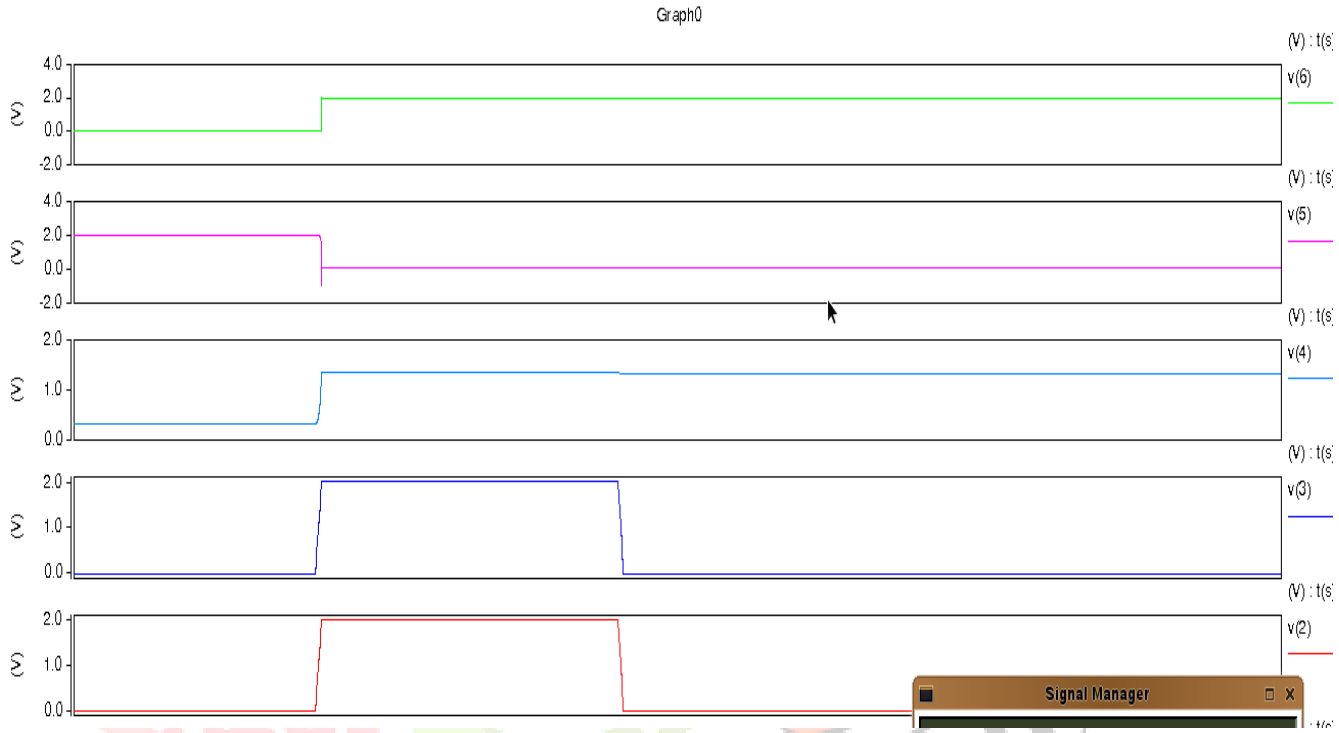

Fig 3.3 Write operation in the 7T SRAM Cell, storing "1" in the memory

In the obtained CSCOPE graph, the word line is asserted high at node V(3). When the data is present at the bit line node v(2), it charge the node Q i.e. node V(4) to the level of the bit line logic level. The feedback path is disconnected and the first inverter gives the complement of node v(4) at node V(5) which is Qbar. In this way the data is stored in the memory. The data will remain in the memory until the memory is refreshed or the new data is written in the memory.

3.4 Read operation in 7T SRAM Cell

For the read operation, pre-charging of the bit line is necessary. For which a pre-charge circuitry is used. Just like the 6T SRAM cell, where the two pull-up transistors were used, one for the bit line (BL) and another one for the bit line bar (BLB) here also a PMOS pull-up transistor is used to pre-charge the single bit line (BL). The worst case situation of SNM or static noise margin is under "read-disturb" condition. The pre-charge circuitry is shown in the figure below:

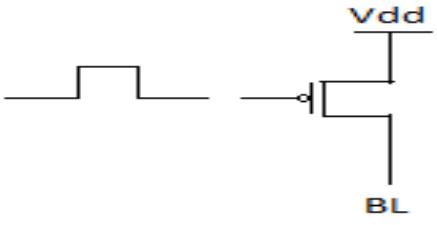

Fig.3.4 pre-charge circuitry

In the pre-charge circuit, a short duration pulse is given input to the PMOS gate input to pre-charge the bit line. The drain of the pre-charge circuit is connected to the bit line (BL) of 7T SRAM Cell. After pre-charging of the bit line the word line is asserted to high logic level “1”. This makes the access transistor to provide path to the storage node Q. The feedback path is connected to the inverter input. The stored value in the node Q is discharged in the bit line. If the data “0” is present in the memory then bit line is discharged from 1 to logic level “0”. If the data “1” is present in the memory then bit line is charged to the high logic level “1”.

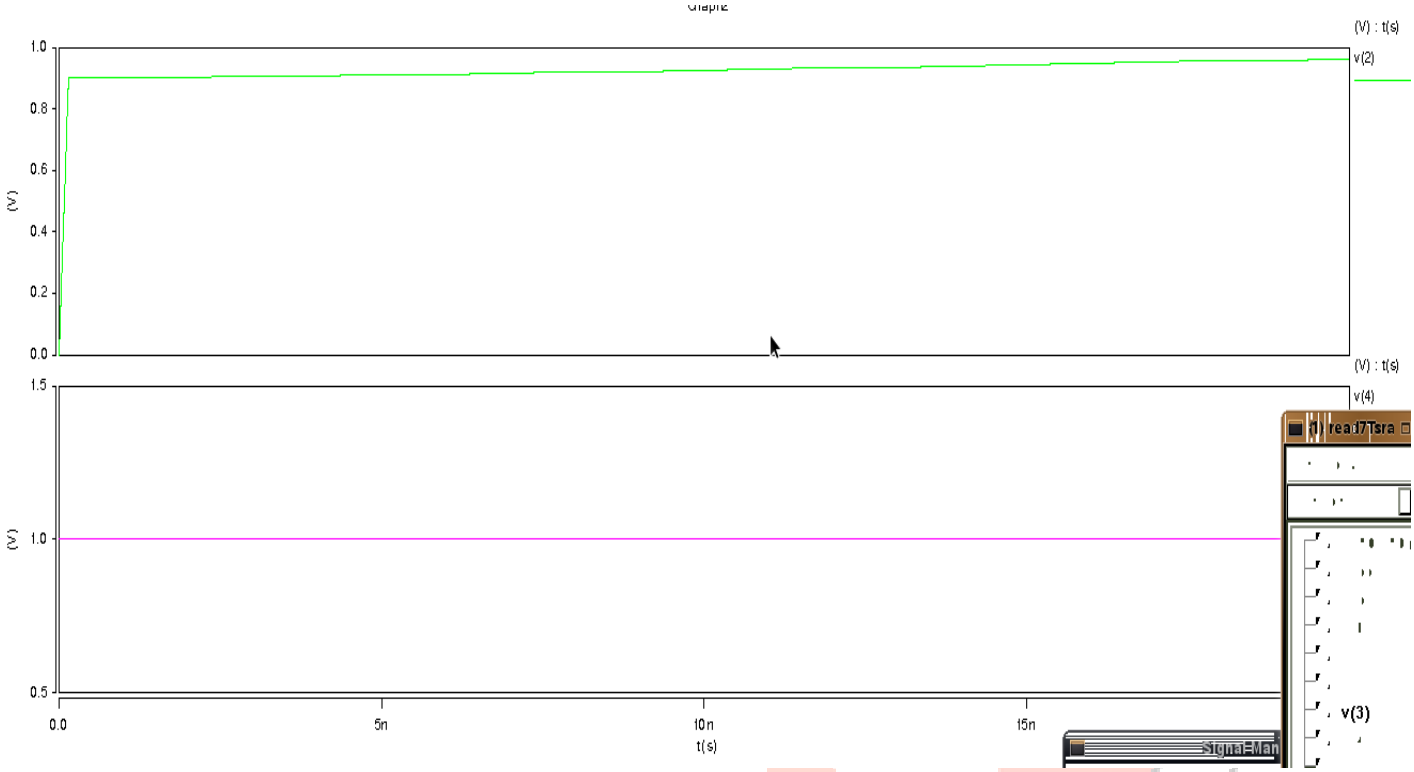

Fig 3.5 Read operation in the 7T SRAM, reading “1” from the memory.

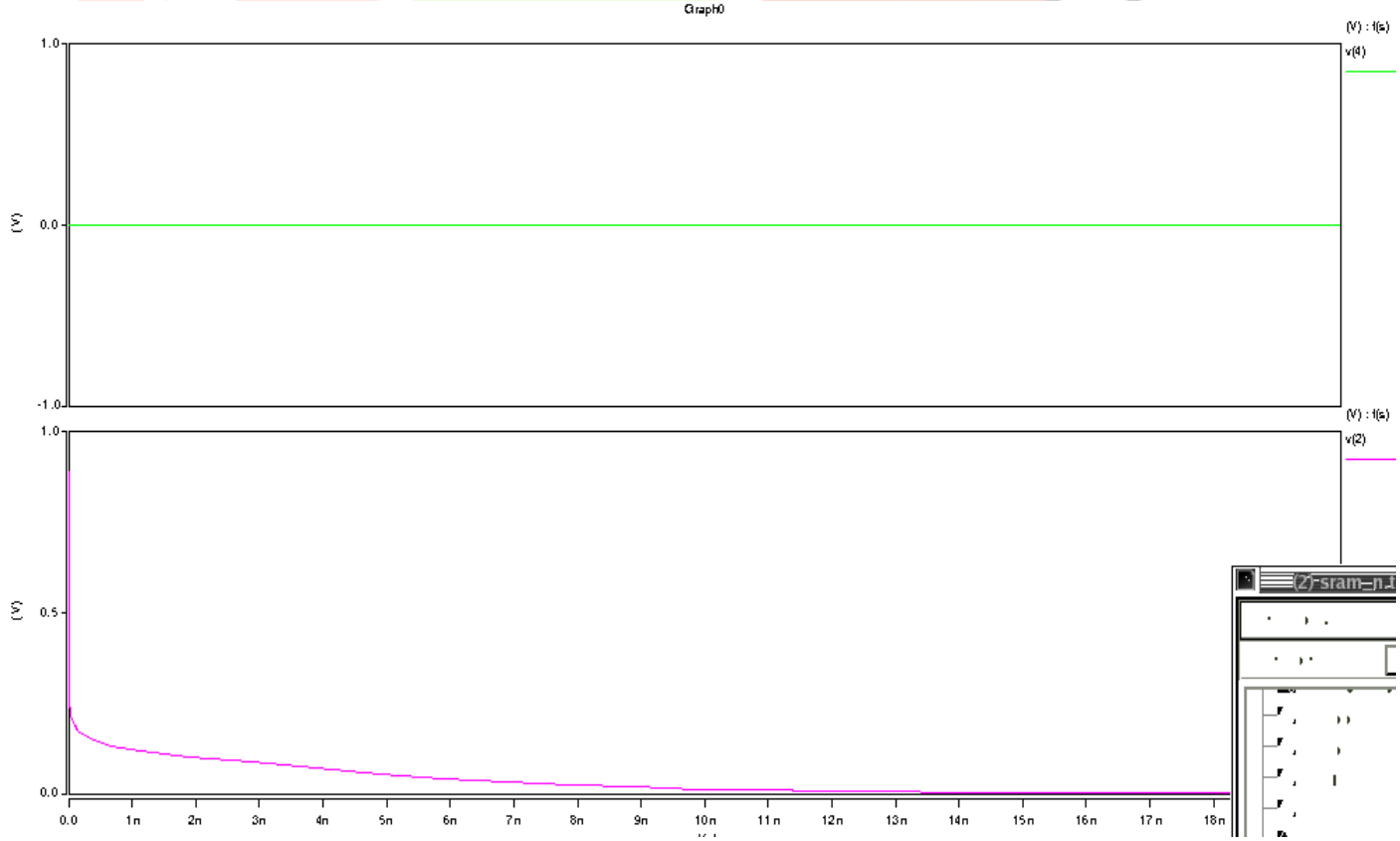

Fig 3.6 Read operation in the 7T SRAM, reading “0” from the memory.

IV. RESULTS AND DISCUSSION

4.1 Result Analysis

Table 4.1: HSPICE Simulation results of 6T and 7T SRAM Cell

Parameter	7T SRAM Cell	6T SRAM Cell
Process technology	65nm	65nm
Power supply	1.4v	1.4v
Precharge value	1.4v	1.4v
Power consumption during write(for DC input)	8µw	20µw
Power consumption during the Read(DC)	2.885 pw	6.674nw
Leakage current during the Write operation	0.217nA	0.4n A
Leakage current during the Read operation	4.824pA	6.9359pA
Static noise margin(SNM)	0.212v	0.119v
Write delay	15.90ps	26.780ps
Read delay	Read zero 6.432ps Read one 4.824ps	Read zero 29.50ps Read one 22.32ps

Table 4.2 Read and Write Delay in 6T and 7T SRAM Cell

	Write operation	Delay (ps)	Read operation	Delay (ps)
SRAM 6T	Write 0	330	Read 0	390
SRAM 7T	Write 0	260	Read 0	350
SRAM 6T	Write 1	330	Read 1	380
SRAM 7T	Write 1	270	Read 1	263

This paper uses stacking technique with 65nm technology to reduce the leakage power and SNM. This paper analyses standard 6T, new 7T SRAM and 8T SRAM (static random access memory) cell in light of power consumption, leakage current and time delay to verify their functionality and robustness at 65nm Technology. The 7T SRAM cell consumes 50%-70% less power during write operation and 30%-60% less power consumption during the read operation. It shows 80% improvement in static noise margin (SNM), 85% improvement in read static noise margin (RSNM) and 45% improvement in write static noise margin (WSNM). Leakage current reduction is 10%-20%.

4.2 AREA PENALTY

The 7T SRAM Cell Bears the area penalty of 11% as compared to the 6T SRAM Cell due to extra access transistor taken into account.

V. Advantages over 6T SRAM Cell

i. It consumes less power in both read and write operation
ii. Leakage currents are reduced in the new 7T SRAM design process at 65nm.
iii. It has better read and write stability.
iv. It has very good process ability at ultra-low power regime.
v. It operates on single bit line instead of conventional two bit line.
vi. Static Noise Margin is improved to 0.212v.

REFERENCES:

[1] Khushboo Mishra, shyamAkashe IEEE, "Modelling and simulation of 7T SRAM Cell at various process corners at 45nm process technology", 2012 second international conference on Advance computing & communication Technologies,DOI 10.1109/ACCT.2012.71.

[2] Vikasnehra, rajeshsingh, shilpibirla "simulation and Analysis of 8T SRAM Cell's stability at deep sub-micron CMOS technology for multimedia applications", 2012 Canadian Journal on Electrical and Electronics Engineering Vol. 3, No. 1, January 2012

[3] Aminulislam, mohd. Hassan, IIUM "Variability analysis of 6T and 7T SRAM Cell in sub-45nm technology", 2011, IIUM journals Vol.12, No.1, 2011.

[4] Madhavsingh, shailendrasinghTomer, IJRRCS "Analysis of stability and SNM of 7T SRAM Cell on 45nm technology", vol.2, NO.6, December 2011, ISSN 2079-2557.

[5] Sunil kumarmaravi, prithvi raj singhchouhan, IJERA "comparative Analysis of 6T and 7T SRAM Cell at 0.18um technology", vol.2, issue 1, jan-fab 2012, ISSN: 2248- 9622.

[6] Ramy E. Aly and magdy A. Bayoumi, IEEE "Low power cache design using 7T SRAM Cell". IEEE transaction on circuits and systems –II, vol.54, No.4, April 2007.

[7] Young Jun Lee, young-bokkim,young-bin kim, IEEE "Low power 8T SRAM Design technique for CNFET", International SoC Design Conference, 2008.

[8] Shilpibirla, kapilrathi, manishapattanaik "Analysis of 8T SRAM Cell at various Process corners at 65nm process technology", circuits and systems, 2011, 2,326-329, doi:10.4236/cs.2011.24045.