Implementation of 16-Bit RISC Microprocessor Using Verilog

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Abstract

The main aim of the paper is simulation and synthesis of the 16-bit RISC CPU based on MIPS. The project involves design of simple RISC processor and simulating it. A Reduced Instruction Set Compiler (RISC) is a microprocessor that has been designed to perform a small set of instructions, with the aim of increasing the overall speed of the processor .In this work, we analyze MIPS instruction format, instruction data path, decoder module function and design theory based on RISC (Reduced Instruction Set Computer) CPU instruction set. We use pipeline design process to simulate successfully, which involves instruction fetch (IF), instruction decoder (ID), execution (EXE), data memory (MEM), write back (WB) modules of 16-bit CPU based on RISC CPU instruction set. In this project we are using hazard detection unit helps for accurate behavior of the system. In this project for simulation we use Modelsim for logical verification, and further synthesizing it on Xilinx-ISE tool using target technology and performing placing & routing operation for system verification. The language we used here is VERILOG, and tools required here are XILINX -ISE 13.1-Synthesis.This processor make it especially suited to embedded control applications.

Keywords: *MIPS, RISC, Simulation Synthesis, Instruction Set, MODELSIM, RTL Schematic, Technology Schematic.*

I. INTRODUCTION

Processors are divided into 3 categories 8- bit, 16-bit and 32-bit processor, depending upon the demand of performance, cost, power and programmability. 8-bit processors have extreme low cost and consume less powerfor simple control system. In contrast to 8-bit, 32-bit processors have high programmability, high performance and are widely used in cellular phone and PDA that need high computation but it has high power consumption. On the other hand 16-bit processors have high performance and power than 8-bit processorand low power consumption than 32-bit processor.

They are often used in 16-bit applications such as disk driver controller, cellular communication and airbags, etc.

The reduced instruction set computer, or RISC, microprocessor CPU designphilosophy that favors a smaller and simplerset of instructions that all take about thesame amount of time to execute. The most common RISC microprocessors are ARM, DEC Alpha, PA-RISC, SPARC, MIPS, and IBM's PowerPC. The idea was inspired by the discovery that many of the features that were included in traditional CPU designs to facilitate coding were being ignored by the programs that were running on them.

The features which are generally found in RISC designs are uniform instruction encoding which allows faster decoding, ahomogeneous register set allowing any register to be used in any context and simplifying compiler design, simple addressing modes, It was also becoming cost-effective to employ small amounts of higher-speed cache memory to reduce memory latency. The instruction set can be hardwired to speed instruction execution.

The rest of the paper is organized as follows: Section II gives the MIPS architecture. Section III highlights simulation results and analysis. Finally Section IV gives the concluding remarks.

II LITERATURE SURVEY

[1] P.V.S.R.Bharadwaja et.al, suggests that the instruction set can still be increased by increasing number of instructions which makes the system more complex. The Data gating technique is applied to the work to check the efficiency of the processor.

[2] Sharda P. Katke and G P Jain proposed the 5 stage pipelined architecture of 32 bit RISC Processor (MIPS) has been designed using VHDL. The simulations is done with Model Sim simulator. A Reduced Instruction Set computer is a microprocessor that was designed to perform a small set of instructions

[3] M Kishore Kumar and MD.Shabeena Begum introduced a 32 bit RISC Processor implemented on a FPGA board. The design is implemented using VHDL

[4] N. Alekya and Ganesh Kumar designed a Simple RISC Processor analyzed MIPS instruction format, instruction data path, decoder module function and design theory based on RISC (Reduced Instruction Set Computer) CPU instruction set. They used the pipeline design process to simulate successfully, which involves instruction fetch (IF), instruction decoder (ID), execution (EXE), data memory (MEM), write back (WB) modules of 32-bit CPU based on RISC CPU instruction set.

[5] Jinke Vijay Kumar et.al, implemented a FPGA based pipelined 32-bit RISC processor with Single Precision Floating Point Unit is designed and Verilog coding is adopted. The design is implemented on Altera DE2 FPGA on which Arithmetic operations, Branch operations, Logical functions and Floating Point Arithmetic Operations are verified.

III MIPS ARCHITECTURE

A. Structures Used In MIPS Design

The MIPS processor is compilation of a lot many structures which are used as blocks of interconnection. The utilization of all these blocks is explained here.

B. Instruction Fetch Unit

The first stage in the pipeline is the Instruction Fetch. Instructions are fetchedfrom the memory and the Instruction Pointer (IP) is updated. The function of the instruction fetch unit is to obtain an instruction from the instruction memory using the current value of the PC and increment the PC value for the next instruction.

This stage is where a program counter will pull the next instruction from the correct location in program memory. In addition theprogram counter will updated with eitherthe next instruction location sequentially, or the instruction location as determined by a branch.

The instruction fetch stage is also responsible for reading the instruction memory and sending the current instruction to the next stage in the pipeline, or a stall ifa branch has been detected in order to avoid incorrect execution. The instruction fetch unit contains the following logic elements that are implemented in VERILOG: 8-bitprogram counter (PC) register, theinstruction memory, a multiplexor, and an AND gate used to select the value of the next PC.

Program counter and instruction memory are the two important blocks of Instructions Fetch Unit

C. Program Counters (Pc)

It is an 8 bit device that is connected to the data bus and the address bus. It will hold its value unless told to do something. If the I/P is kept high the device will count.

D. Instruction Memory (Im)

The Instruction memory on these machines had a latency of one cycle. During the Instruction Fetch stage, a 16-bit instruction is fetched from the memory. The PC predictor sends the Program Counter (PC)to the Instruction memory to read the current Instruction.

At the same time, the PC predictor predicts the address of the next instruction byincrementing the PC by 1.

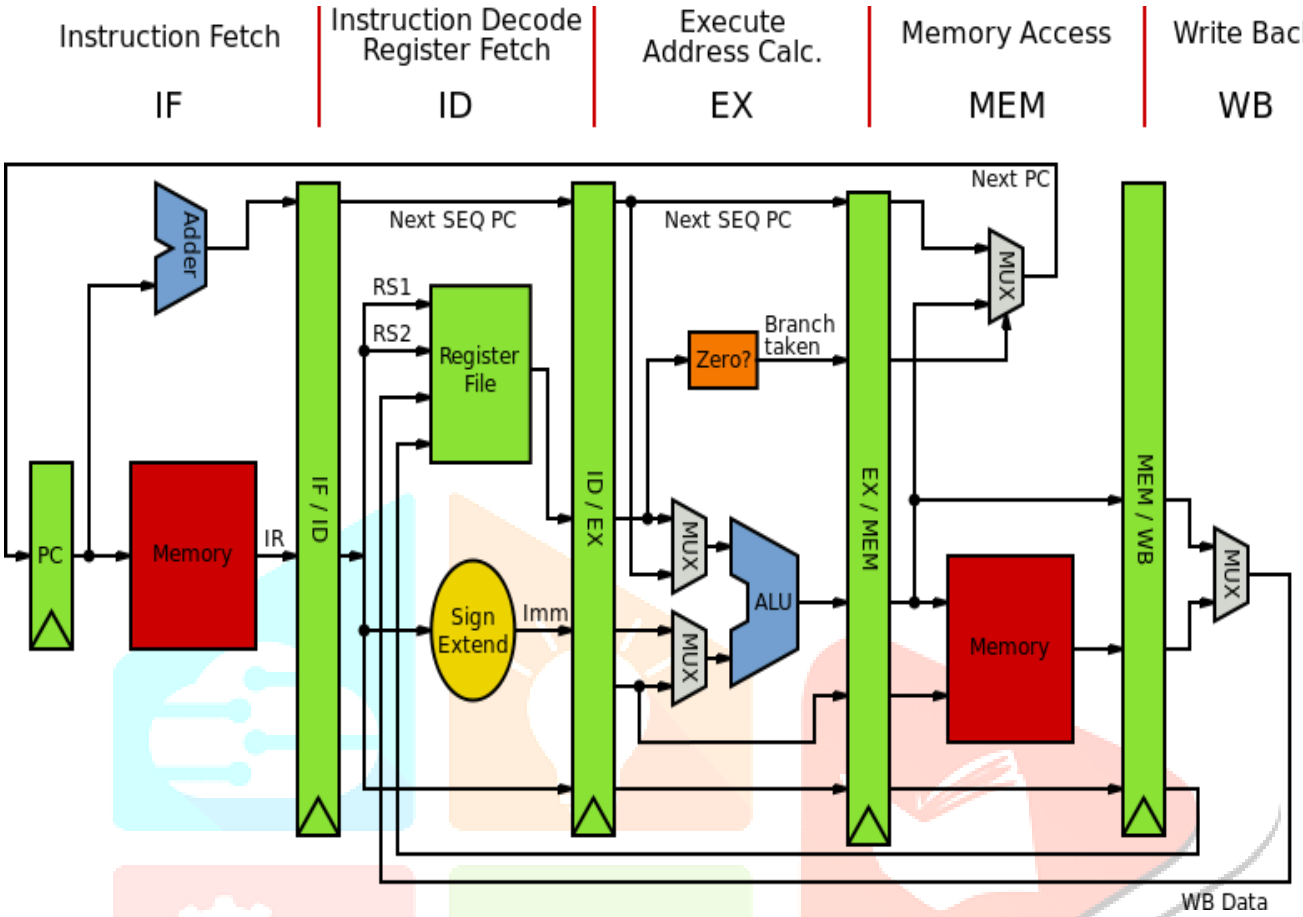

Fig.1: MIPS Single-Cycle Processor

E. Instruction Registers (Ir)

An instruction register (IR) is the part of control unit that stores the instruction currently being executed or decoded. In simple processors each instruction to be executed is loaded into the instruction register which holds it while it is decoded, prepared and ultimately executed, which can take several steps. RISC processors use a pipeline of instruction registers where each stage of the pipeline does part of the decoding, preparation or execution and then passes it to the next stage for its step. Modern processors can even do some of the steps of out of order as decoding on several instructions is done in parallel.

Decoding the opcode in the instruction register includes determining the instruction, where its operands are in memory, retrieving the operands from memory, allocating processor resources to execute the command. The output of IR is available to control circuits which generate the timing signals that controls the various processing elements involved in executing the instruction. **See Figure 2.**

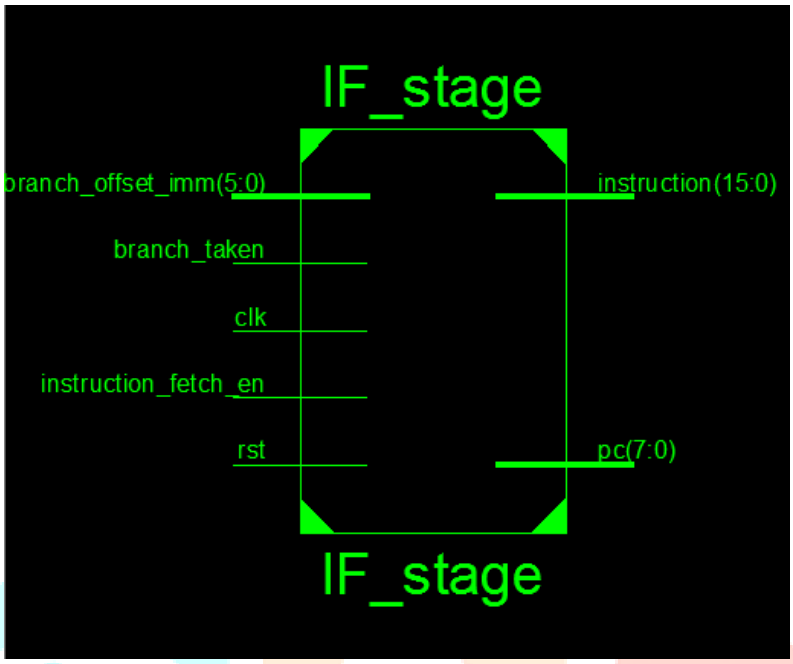

Fig.2: RTL Schematic for IF Unit

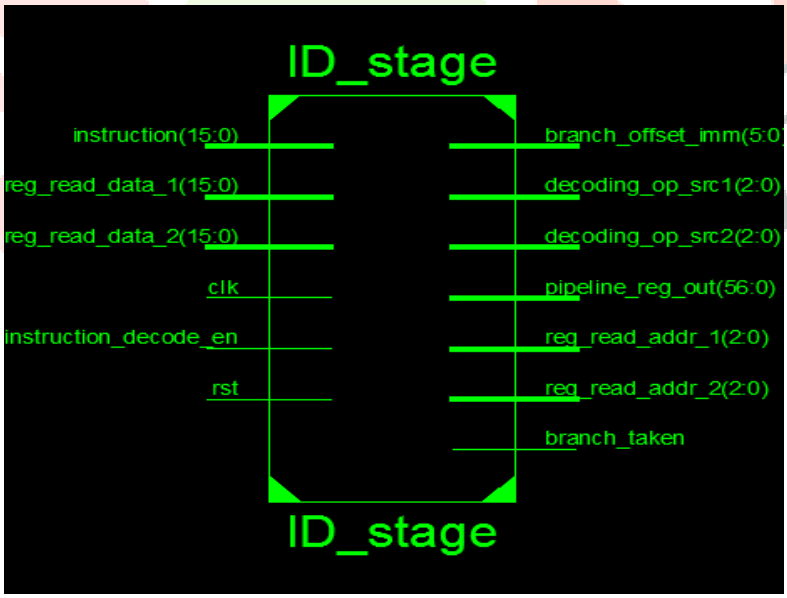

Fig. 3: RTL Schematic for ID Unit

F. Instruction Decode Unit

The Instruction Decode stage is the second stage in the pipeline. Their function is to detect if the register to be fetched in this stage is written to in a later stage.

The Decode Stage is the stage of the CPU's pipeline where the fetched instruction is decoded, and values are fetched from theregister bank. It is responsible for mapping the different sections of the instruction into their proper representations. Register files(RF): During the decode stage, the two register RS1& RS2 are identified within the instruction, and the two registers are readfrom the register file. In the MIPS design, the register file had 32 entries. At the same time the register file was read, instruction issue logic in this stage determined if the pipeline was ready to execute the instructionin this stage. If not, the issue logic would cause both the Instruction Fetch stage and the Decode stage to stall. If the instruction decoded was a branch or jump, the target address of the branch or jump was computed in parallel with reading the register file. **See Figure 3.**

G. Execution Unit

The third stage in the pipeline is where the arithmetic- and logic-instructions will be executed. The execution unit of the MIPS processor contains the arithmetic logic unit (ALU) which performs the operationdetermined by the ALU op signal.

H. Arithmetic Logic Unit

The ALU is the unit used forComputations. This is the basic unit text which performs allthe operations required by the processor.

I. Data Memory Unit

This is the second memory of the MIPS. This memory can be used for both Read and Write applications. Hence this circuit can bereplaced by a Random Access Memory (RAM). The input is the address and if read signal is enable it reads the data from the inputs memory location. If write signal is enable it writes the data into the input's memory location.

J. Write Back Unit

During this stage, both single cycle and two cycle Instructions write their results into the register file.

K . Hazard Detection Unit

It compares the source register of theinstruction in ID_stage and its previous 3 instructions' destination register. If the source register is equal to any of the three

destination register and not equals to zero, the Hazard Detection Unit will assert pipeline_stall signal.

That signal will freeze the IF & ID stage,and insert bubbles into EX stage. When the hazard instruction was flushed out of the pipeline, pipeline_stall signal will be canceled.

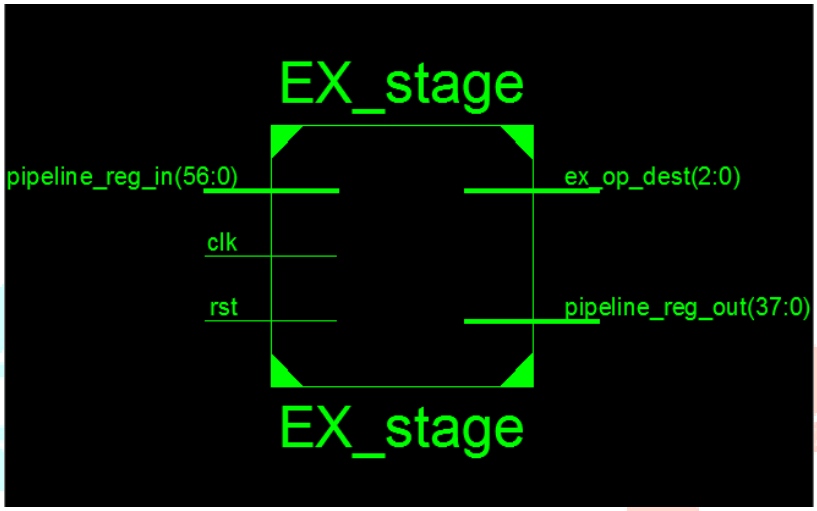

Fig. 4: RTL Schematic for EXE Unit

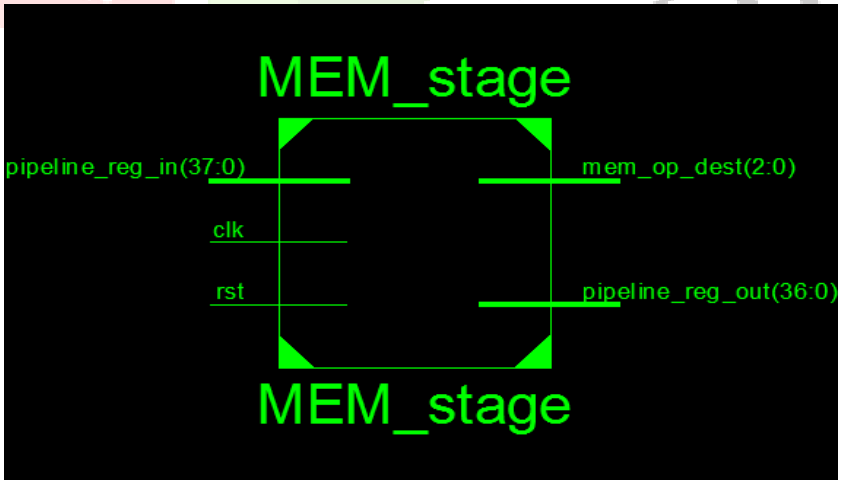

Fig. 5: RTL Schematic for Data Memory Unit

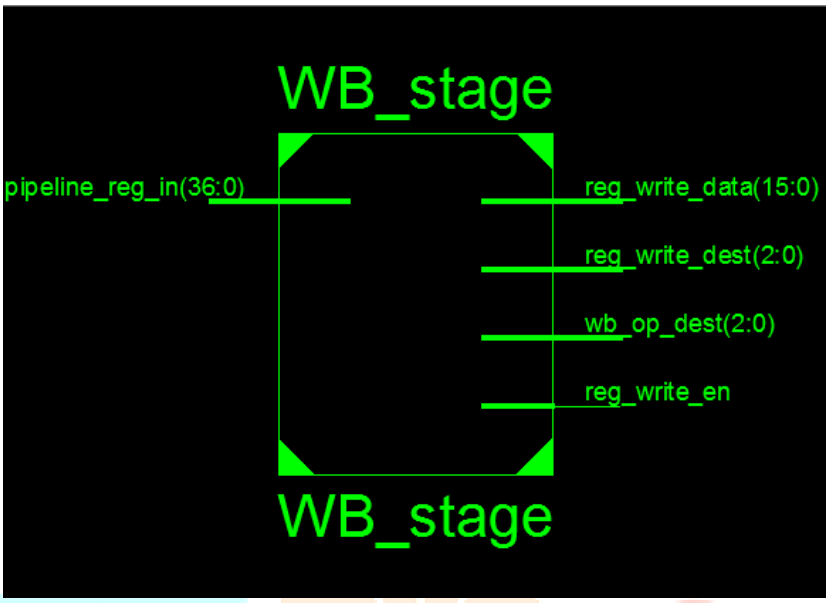

Fig. 6: RTL Schematic for Write Back Unit

IV SIMULATION RESULTS AND ANALYSIS

A Simulation Results

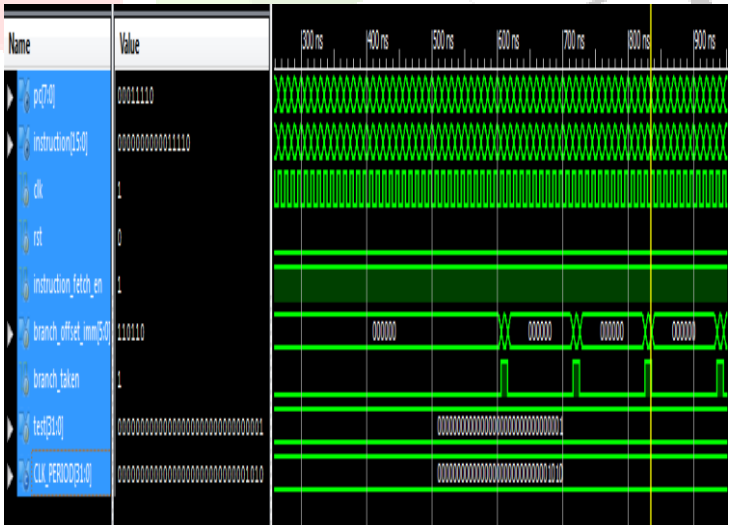

Fig.7: Simulation Waveform of Instruction Fetch Unit

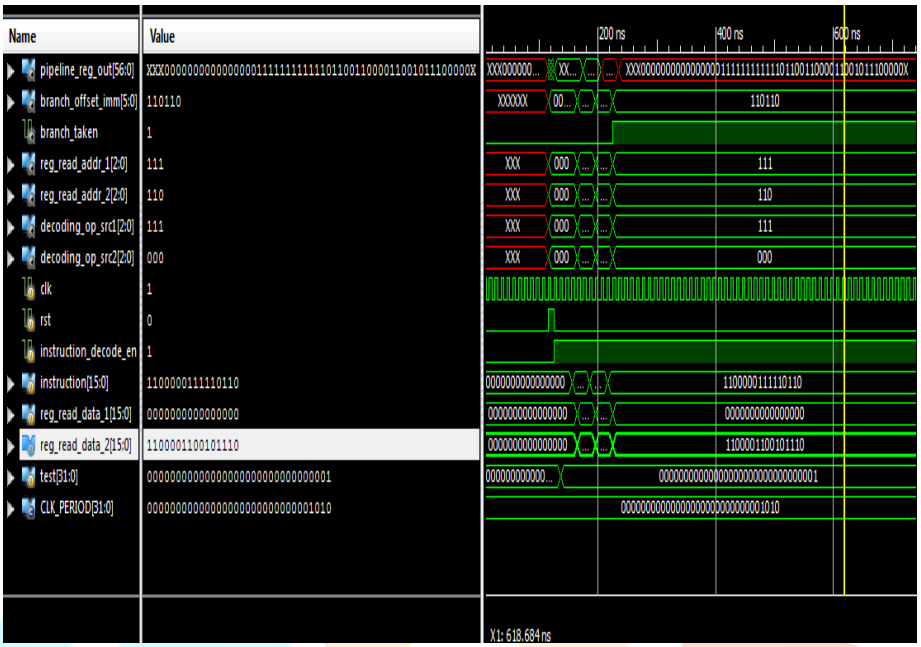

Fig.8: Simulation Waveform of Instruction Decoder Unit

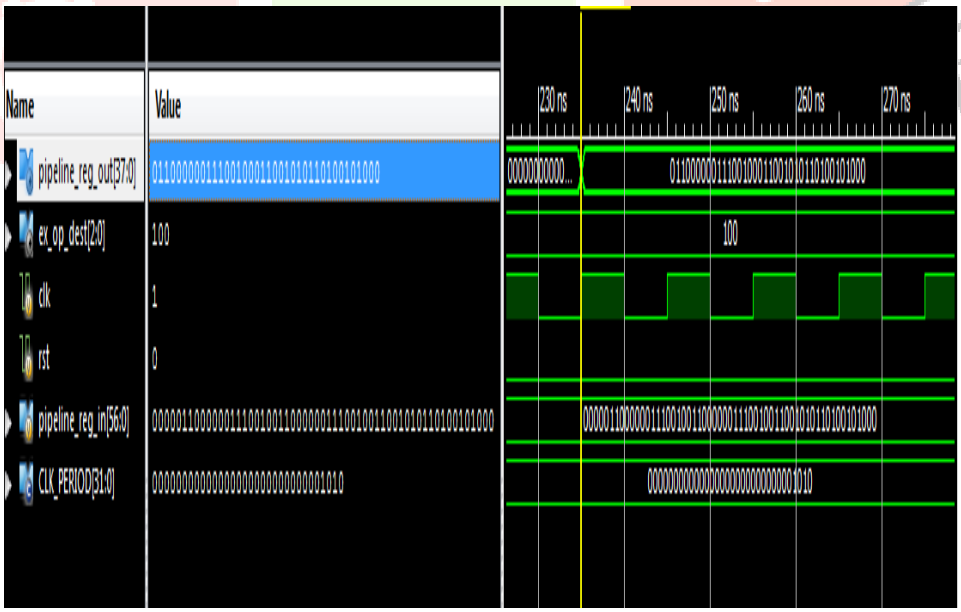

Fig. 9: Simulation Waveform of Execution Unit

Fig. 10: Simulation Waveform of Write back Unit

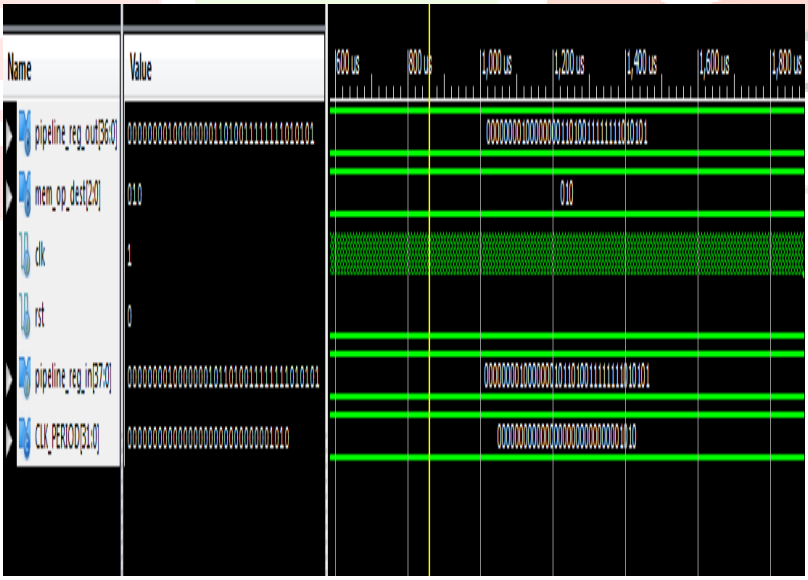

Fig. 11: Simulation Waveform of Data memory unit(RAM)

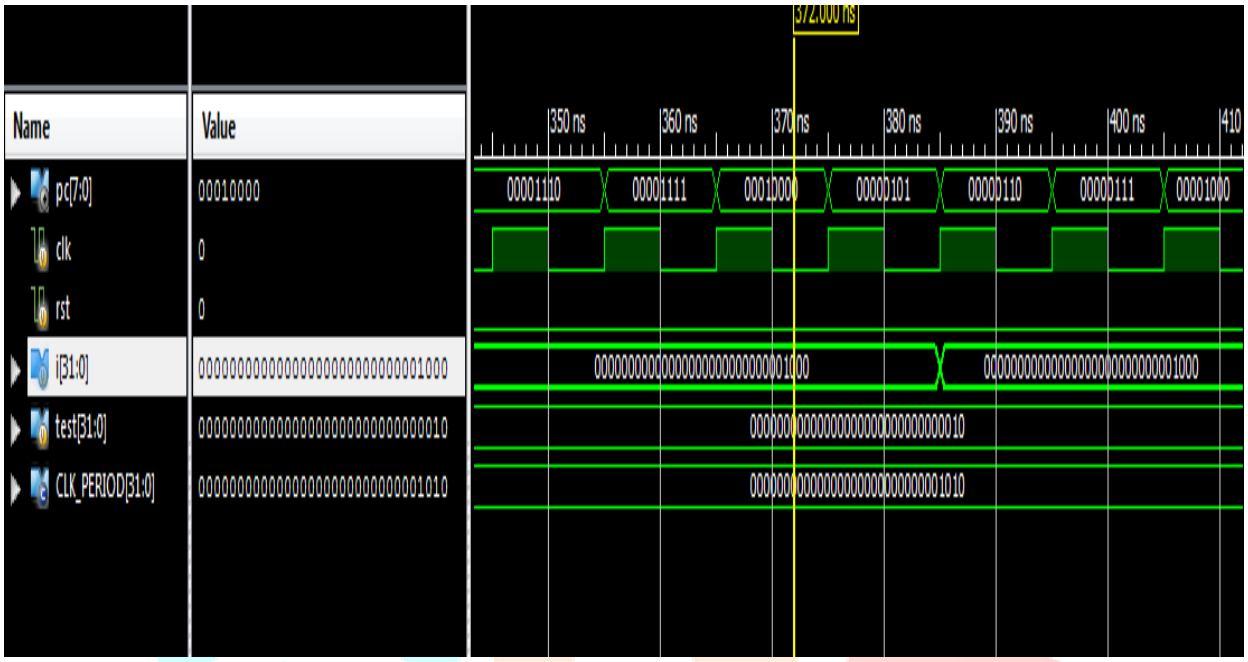

Fig.12: Simulation Waveform of 16-bit RISC(MIPS) Processor

B Synthesis Result

The developed convolution project is simulated and verified their functionality. Once the functional verification is done, the RTL model is taken to the synthesis process using the Xilinx ISE tool.

In synthesis process, the RTL model will be converted to the gate level net-list mapped to a specific technology library. Here in this Spartan 3E family, many different devices were available in the Xilinx ISE tool.

C Rtl Schematic

The RTL (Register Transfer Logic) can be viewed as black box after synthesize of design is made. It shows the inputs and outputs of the system. By double-clickingon the diagram we can see gates, flip-flops and MUX.

Device Utilization Summary is as shown in figure 14.

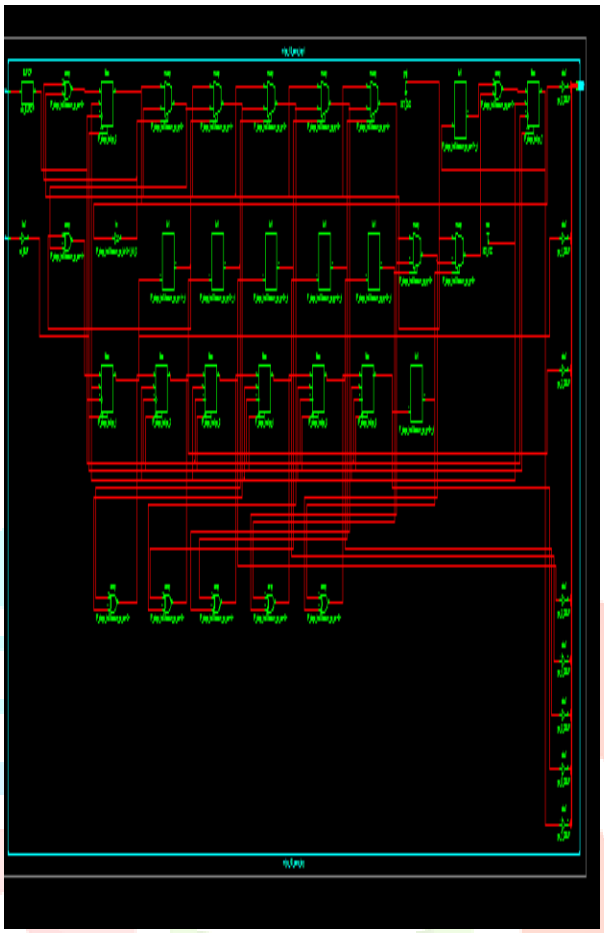

Fig. 13: RTL Schematic internal view of RISC(MIPS) Processor

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	4	3584	0%
Number of Slice Flip Flops	8	7168	0%
Number of 4 input LUTs	8	7168	0%
Number of bonded IOBs	10	97	10%
Number of GCLKs	1	8	12%

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Minimum period: 4.414ns (Maximum Frequency: 226.552MHz)
Minimum input arrival time before clock: No path found
Maximum output required time after clock: 7.241ns
Maximum combinational path delay: No path found
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Fig. 14: Device Utilization Summary

V CONCLUSION

Thus the 5 stage pipelined architecture of 16bit RISC Processor (MIPS) has been designed using VERILOG. The simulations are done with Model Sim simulator. Thesimulation result shows that the processor works perfectly. A Reduced Instruction Set computer is a microprocessor that had been designed to perform a small set of instructions, with the aim of increasing the overall speed of the processor .The RISC concept proved that 20% of instruction did 80% of the work .The RISC architecture follows the philosophy that one instruction executes in one clock cycle.

Future work will be added by increasing the number of instructions and to add more pipelined stages in the design to improve theperformance of the design and to increase the speed of the processor.

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