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4 BIT SIGNED CALCULATOR IMPLEMENTATION USING UART

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ABSTRACT

ALU's are the basic building blocks of any microprocessors and microcontrollers. It defines the implementation of various combinational and logical functions. This paper describes the designing of the UART AND ALU, their communication and implementation on the FPGA. The UART takes input from the keyboard and FPGA Board communicates with each other and through this operation the user can use various operations according to its need. The user can input data through the keyboard with the help of data transmitting software. The UART, which acts as an interface, processes this data to the ALU block. The block performs the desired operation given by the user. Once the operation is done it is carried to the FPGA board which is acting as the output terminal and the output will be displayed on the Seven Segment Display of FPGA. The advantage of using the board is that it provides high processing speed and also very effective in debugging of errors. Implementation is done using XC7A35T1CPG236C Basys3 FPGA Board. Simulation and synthesis are carried on Vivado 2014.2 software.

Index Term: UART, FPGA, Verilog, ALU, and Seven Segments Display.

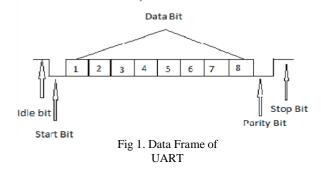
I. UART

UART stands for UNIVERSAL ASYNCHRONOUS RECIVER/TRANSMITER. It is being used for asynchronous serial electronic communications by changing the data via parallel to serial at transmitter with some further overhead bits victimization register and contrariwise at receiver. Due to its low cost, low power, and simple architecture it Is being prefer for the short communication. It is usually connected between a processor and other peripherals. UART have different necessities and attributes that is needed electronics communication between its practical units. In such communication it communicates personally with each other. The transmitting UART change parallel data that is input via CPU into serial form and transmit it to serially tothe given UART which finally changes serial data back toparallel data for the accepting devices. For such communications only 2 wires (one for transmitting and another for receiving data) are needed to transmit data between 2 UART devices. The data moves from the Tx pinof the UART to the Rx pin of receiving UART. As it transmits the data asynchronously i.e. It does not require any type of clock to synchronize the output of the transmitting UART to the sampling of the bits by receiving UART. As an alternative of the clock signal, the sending UART adds bits for the data transmission these bits are start bit and stop bit. These bits tell the staring and ending of a data packet so that the receiving UART could know when it should start reading the data bits. So whenever receiving UART found a start bit, it start reading the incoming

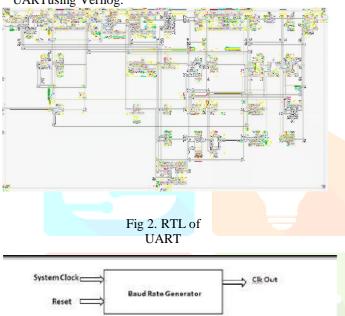
Bits at a particular frequency, which is known as baud rate. It is a measure of data transfer rate which is represented in bits per sec (bps). For the perfect working both the communicating devices must operate the same data transfer rate. The data transmission rate between the transmitting UART and receiving cannot exceed 10 percent before the timing of bites gets too far. While communicating both UART must be configures to the same data structure. The UART which is at the transmitting end receives data from the data bus. The data buses are used for sending data to UART by various devices like memory, CPU or microcontroller. Data is transferred in the parallel form from the bus to the transmitting UART. After getting the parallel data from the data bus the transmitting UART adds bits like start bit, stop bit, parity bit to form a packet. The parity bit tells if there is any change in data or not to the receiving UART. Data packets is output serially bit by bit at Tx pin. Receiving UART reads the data packets at its Rx pin. Then the receiving UART changes the data back to its original parallel form and therefore removes the extra bits like start bit, Parity bit, and stop bits. At last, the receiving UART transfers data packet in parallel form to data bus on the receiving end.

A fixed size of data frame is transmitted when we transmit or receive signal using UART which

contains a Start Bit then followed by 8bit ASCII value corresponding a character then a parity bit and to acknowledge a Stop bit is send so that the device can get acknowledgement that the data is transmitted.



RTL of UART means the major blocks used to make the **UARTusing Verilog.**



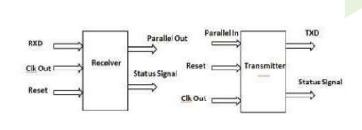


Fig 3. Basic Diagram of UART

II.FPGA

FPGA stands for field-programmable gate array. FPGAs are semiconductor devices. An FPGA is an matrix of interconnected digital subcircuits that implement common functions while also offering very high levels of flexibility. The FPGA architecture specially created using HDL languages. HDL stands for Hardware Description Language, are Verilog, VHDL. FPGA is similar as application specified integrated circuits (ASIC). It allows a ranking of interconnects which allows blocks to be grouped together in dissimilar configurations. These blocks then can be set to perform some complex functions for example Division, Multiplication and some simpler

logic gates like AND, OR, XOR. The FPGA logic blocks also have memory elements which is simple flip-flops or complete blocks of memory.

The advantages of using FPGA are given.

- IT has skill to re-program in field to remove bug.
- Prototyping is fast
- Very low cost
- Very high Speed

We are using **XC7A35T-1CPG236C Basys3 FPGA** Board. Features

- 1800 Kilobits RAM
- 100 Megahertz Clock
- 4-digit and 7-segment display
- 16- user switches
- 16- user LEDs

III.Verilog

Verilog is a hardware description language (HDL) that was standardized as IEEE Std 1364TM-1995 and first revised as IEEE Std 1364-2001. It is used for describing electronic circuits and systems like a microprocessor or a flip-flop.it is also used in verification of various circuits like analog and mixed signal circuits. By using a HDL we can describe any digital hardware at any level. It includes various types of modeling methods in which the code can be written. Modeling are basically the types of coding we can use to design our code. The techniques include:

- Gate level modeling
- Data flow modeling
- Behavioural modeling
- Switch level modeling

The user can use any of the above form to write code so as to achieve its desired result. In our project we uses three modeling. Data Flow and Behavioral Modeling for making sub modules like UART, ALU, and ASCII to Decimal Converter. Gate Level modeling to combine all the sub modules used here.

IV.ALU

It stands for Arithmetic Logic Unit. ALU is the basic building block of microprocessor, Microcontroller or Microcomputers. ALU is responsible for performing various logical functions which includes both the combinational functions named as Addition, Subtraction, Division, Multiplication and logical operations like AND, OR and NOT, etc. The ALU reads the inputs and the function which needs to be implemented which is selected by the user. According to our ALU, user can give input operands up to 8 bits and can the ALU can perform its desired operation according to the inputs provided to it. The desired operation is performed and the output is displayed on the seven-segment display.

Operations of ALU

Mode	Operation
5'b00000	Addition
5'b00001	Subtraction
5'b00010	Multiplication
5'b00011	Division
5'b00100	Bitwise AND
5'b00101	Bitwise OR

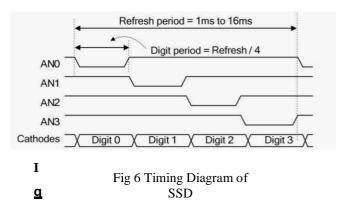
5'b00110	Bitwise NOR
5'b00111	Bitwise NAND
5 'b 01000	Bitwise XOR
5 'b 01001	Bitwise XNOR
5'b01010	Greater Than
5'b01011	Equal To
5'b01100	Less Than
5'b01101	Shift Left
5'b01110	Shift Right
5'b01111	Rotate Right
5'b10000	Rotate Left

Fig 4. RTL of ALU

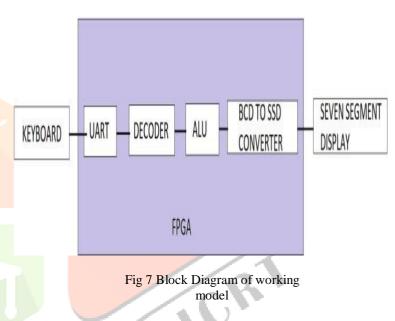
V. **Seven Segment Display**

SSD stands for Seven Segment Display is basically an electronics device which is generally used to display the numerical or alphanumerical values. It is a combination of LED's with a common anode or cathode and are arranged in such a manner it looks like 8 and there are total 8 LED for one SSD 7 for the formations of numerical or alphanumerical values and 8th for displaying a dot and if we uses a module which contain 2 or 4 SSD then we must use a proper timing to work on all the segments.

If one is using a 4 Digit Seven Segment Display the timings are AN0 to AN3 are the digits. One must refresh the display according to the timings diagram.



VI. <u>BLOCK DIAGRAM</u>



VII. WORKING

INPUT -The user will firstly select the mode then set inputin operands with the help of keyboard then select the operations as per the requirement.

OUTPUT -The FPGA board will take the data from the modules which will be in coded form and will reflect that on the seven segments which will the show the output with the help of LED combination. The user can change the output ports according to his needs at any time. If Mode is0 then it will display 1st operand, if mode is 1 then it will display 2ndoperand and if mode is 2 or 3 then it will display the result on Seven Segment Display.

INTERFACING - The UART will act as the interface between the keyboards is helping in setting inputs operands with the help of FPGA. Then the input is processed by the ALU block which is connected with the input setting block. After that the outputs are send for displaying. For displaying outputs a binary to BCD converter block is used which send output to the seven segment display block. The result is according to the operation selected by the user.

VIII. CONCLUSION

From this work it can be concluded that establish the connection between the UART and the FPGA. The user will input the data and the modes according to his requirements and it will be passed to UART. These will be then passed to the ALU. The ALU will perform the specified function like addition, subtraction, multiplication and division given by theuser which then be converted to BCD so that the final output can be displayed on the Seven Segments.

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IX. LIST OF ABBREVIATIONS

UART: Universal Asynchronous Receiver/Transmitter.

FPGA: Field programmable gate array

ALU: Arithmetic Logic Unit LED: Light Emitting Diode

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