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CASCADED HALF BRIDGE MULTILEVEL INVERTER WITH FILTER FOR VOLTAGE BOOSTING APPLICATIONS

[1]Rahna Rajeev,[2]Rahul Rajesh,[3]Savanth S Dev,[4]Lekshmipriya K J,[5]Amjith S

[1]UG Scholar,[2] UG Scholar,[3]UG Scholar,[4]Assistant Professor,[5]Assistant Professor

[12345]Mahaguru Institute of Technology, Kattachira

Abstract: In many applications, the cascaded multilevel inverter (CMI) topology is common. However, the CMI's biggest disadvantage is that it necessitates numerous switches and segregated dc sources. As a result, the CMI topology becomes more expensive, complex, and large, and its efficiency suffers. Compared to the conventional CMI, the proposed inverter uses almost half the number of switches, while maintaining a boosting capability. Additionally, the main drawback of switched-capacitor multilevel inverters is the capacitor inrush current. This problem is also averted in the proposed topology by using a charging inductor or quasi-resonant capacitor charging with a front-end boost converter with a L-C filter. The capacitor will enhance the diode current while decreasing the ripple voltage. This high current could harm the diode, exacerbate the heating issue, and reduce the filter's effectiveness. On the other hand, a straightforward series inductor lowers the output voltage and current's peak and effective values. An ideal practical filter circuit can be created by combining the functions of a series inductor filter and a shunt capacitor to stabilize voltage and smooth current, respectively**.** The effectiveness of the suggested inverter topology is confirmed by simulation results**.**

Index Terms **- Multilevel Inverter, switched-capacitor cell, switch reduction, reduce harmonics**

I. INTRODUCTION

The Cascaded multilevel (CMI) inverter is unique in that it offers a larger voltage amplitude from given input dc voltages and has a high degree of adaptability. However, the CMI needs a lot of discrete DC sources and switches. In this topology, half-bridge cells take the place of full-bridge cells to lower the switch count. Since each half-bridge cell can only produce unity and zero per-unit voltages, the design of cascaded half-bridge cells results in a periodic staircase waveform. As a result, the cascaded half bridge cell MI (CHMI) and an unfolder H-bridge are utilized to transform the stepped dc voltage into a staircase ac voltage. If the number of switches is decreased while assuming a constant overall value for the voltage stress of all switches in a CHMI, the voltage stress will rise. The switches in the unfolder H-bridge are exposed to the peak value of the output voltage, but the switches in the half-bridge cells in the CHMI architecture can withstand only one per-unit voltage magnitude.

The requirement for numerous isolated DC sources is another problem with the CMI and CHMI architectures. To reduce the number of dc sources in the CMI,[2]-[3] which may be divided into three groups, various solutions have been put forth. The first approach is to swap out the dc-sources for separate transformers with a low frequency. The transformers' ability to convert voltage of any magnitude and to give galvanic isolation are both advantages. Transformers, on the other hand, are expensive, large, and ineffective. The second tactic is to use switched-capacitor cells instead of dc sources, which could result in a reduction in the size, weight, and price of MIs because capacitors are less expensive and lighter than dc voltage sources and transformers. The capacitors have a high failure rate, which is a disadvantage. The switched-capacitor cells' sharp inrush current during the capacitors' charging cycle is another drawback. This flaw increases the risk of capacitor failure and lowers the reliability of switched-capacitor-based MIs [4]-[5]. The inrush current through an inductor in the dc side was reduced by the switched-capacitor based CMI. The final option is to employ a high-frequency transformer to provide certain isolated dc voltages via a high-frequency link. However, because so many components are utilized to provide the dc voltages, this technique has low reliability and efficiency. In order to address the aforementioned and avoid the constraints mentioned, this study proposes a switched-capacitor cascaded half-bridge MI (SC-CHMI) with a modular architecture, voltage boosting capability, and self-balancing management of the capacitor voltages. In the proposed SC-CHMI, just one DC source is employed, and switched-capacitor cells are used in place of the other DC sources. The self-balancing ability of the capacitors enables them to charge without assistance from an outside source. The projected SC-CHMI uses a charging inductor or a front-end boost converter to lower the capacitor inrush currents. Additionally, the front-end boost converter in use can limit the fault current and adjust for voltage drop. Voltage-boosting property, low switch count, and single dc source make it a flexible inverter that can be employed in renewable energy systems.

The multilevel inverter (MLI) is a modified version of the two-level inverter. Multilevel inverters utilize multiple voltage levels achieve a smoother stepped output waveform instead of relying on only two-level voltages. The voltage levels have a direct impact on the smoothness of the waveform. As the voltage level increases, the waveform becomes smoother, but this also results in an increase in complexity. This paper purposes a a L-C filter the capacitor will reduce the ripple voltage, but causes the diode current to increase. This large current may damage the diode and will further cause heating problem and decrease the efficiency of the filter. On the other hand, a simple series inductor reduces both the peak and effective values of the output current and output voltage. Then if we combine both the filter (L and C), a new filter called the L-C filter can be designed which will have a good efficiency, with restricted diode current and enough ripple removal factor .The voltage stabilizing action of shunt capacitor and the current smoothing action of series inductor filter can be combined to form a perfect practical filter circuit for SC-CMI.

II. PROPOSED SC-CMI AND SYSTEM ANAYLSIS

A converter consisting of twelve modules with a DC sources will result in huge number of diverse output voltages levels. This composition will be compared with the predictable approach with identical DC voltage source. Two different control methods for a single-phase converter are offered. Both algorithms imagine a steady sampling interval of the control. Pulse width modulation technique is employed. The methods can receive that the DC source voltages are not steady but variable in time. The definite voltages on the capacitors are therefore calculated, and the phase voltage vector is created. In order to compute all attainable output voltages, the phase voltage vector is multiplied with all possible switching states. This inverter connected series gives different levels of output voltages without changing the circuit except the ratio of input voltages. Switching of the converter is done by staircase control technique. Pulse width modulation technique can also be applied by appropriate calculation of the switching time period. Moreover in order to improve efficiency a L-C filter is connected and it will offer a better choice of attenuating switching frequency harmonics.

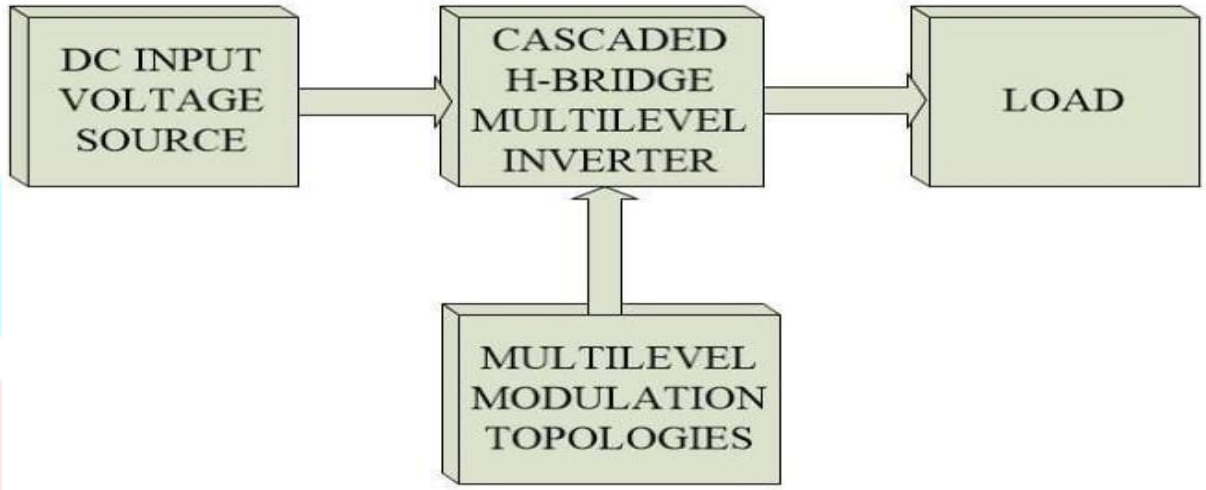

Fig 1: Block diagram for MI

The multilevel inverter offers great advantages over traditional inverter such as increasing power quality with reduced harmonics content. Several DC voltage levels are combined in the Multilevel Inverter topology (MLI) concept to provide a smoother output waveform. The output waveform that was obtained had less harmonic and dv/dt distortion. The rise in voltage levels has made the circuit design more intricate. Additionally, a challenging switching controller circuit is required.

Inverter maintains a boosting capability despite using approximately half as many switches and single dc source is used. The capacitor inrush current is another problem with switched-capacitor multilevel inverters. The proposed design also avoids this issue by employing a charging inductor or quasi-resonant capacitor charging in conjunction with a front-end boost converter.

This novel cascaded H-bridge architecture multilevel inverter with this method, total harmonic distortion is decreased compared to previous multilevel inverters, this idea aid reducing complexity of switching A simple L-C filter load is used to validate the 11 level proposed MI.

III. METHODOLOGY

To address the drawbacks of the traditional single-source CMI, the suggested SC-CHMI design substitutes capacitors for the dc sources and uses just one dc source to charge the capacitors. The proposed topology's general construction is shown in Fig. 8, where the inductor (Lch) and the diodes can minimize the fault current and electromagnetic interference while smoothly charging the capacitors.

To demonstrate the concept, the nine-level SC-CHMI. The charging and discharging modes are denoted by "C" and "D" in Table I, while the "on" and "off" states of the diodes and switches are, respectively, denoted by "0" and "1". is analyzed in the paragraphs that follow. The proposed SC-CHMI has two distinct operating modes for each capacitor: charging and discharging. Only the states of the inner switches (i.e., S1, S2, S3) are shown in Table I since the switches in the half-bridge cell have an opposite action. The unfolder switches likewise operate in this manner the switching modes and current courses of the positive voltage levels.

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Table 1: Switching states of the SC-CHMI

Levels	Main switches	Unfolder Switches	Charging diodes	Capacitors	V out
	S_1,S_2,S_3,S_4	SL_1, SL_2	D_1-D_5	C_1-C_5	
5	1111	10	10000	D, D, D, D, D	$5V_{dc}$
4	0111	10	11000	C, D, D, D, D	$4V_{dc}$
3	0011	10	11100	C, C, D, D, D	$3V_{dc}$
2	0001	10	11110	C, C, C, D, D	$2V_{dc}$
1	0000	10	11111	C, C, C, C, D	$1V_{dc}$
0	0000	11	11111	C, C, C, C, C	0
-1	0000	01	11111	C, C, C, C, D	$-1V_{dc}$
-2	0001	01	11110	C, C, C, D, D	$-2V_{dc}$
-3	0011	01	11100	C, C, D, D, D	$-3V_{dc}$
-4	0111	01	11000	C, D, D, D, D	$-4V_{dc}$
-5	1111	01	10000	D, D, D, D, D	$-5\ V_{dc}$

IV. COMPONENT DESIGN

For the proposed topology to operate steadily, the capacitors and the charging inductor need to be constructed properly. It should be observed that in the purely resistive loading condition, the capacitors experience a greater voltage ripple. As a result, this loading is taken into account while designing the capacitors. The time length of the discharging mode for the k^{th} capacitor is estimated as,

$$T_{\mathrm{dis},k} = 2\sin^{-1}\frac{2k}{l-1}$$

The capacitances can be designed for a desired maximum voltage ripple and discharge time.

$$c_k = \frac{2I_s}{\omega\Delta v_k}\sin(T_{\mathrm{dis},k}/2)$$

To maintain the modularity of the proposed SC-CHMI, the capacitors can be chosen to be identical to the one in the first half bridge, and the voltage ripple can be compensated by adding an additional semiconductor switch to the topology and synthesizing a front-end dc-dc converter at the input side, as shown in the following section. Because the discharge durations of the capacitors in the upper cells are longer than those in the lower cells, the voltage ripple is greater.

If the suggested topology is begun under no-load conditions, a large charging inductor may create over voltages on the capacitors. To prevent overvoltage, eliminate electromagnetic interference, and limit fault current, the charging inductor is built as follows.

$$L_{\mathrm{ch}} \geq \frac{1}{(4\pi f)^2 C_t}, C_t = \sum_{k=1}^{(l-1)/2} C_k$$

But if a larger inductor is used to lower the inrush current, the soft starting technique can be employed to prevent the capacitors' overvoltages.

A. The suggested SC-CMI's topologies are compared to those of single source CMI.

The standard single-source CMI topologies described in Section II of this section are compared to the proposed SC-CHMI. In general, the transformerless switched-capacitor topologies are more effective and have a more compact design than the CTMI topology. It should be noted that the suggested SC-CHMI only requires around half as many switches as previous topologies. Moreover, the suggested SC-CHMI and the CTMI only require half as many diodes as the HFLMI, which uses almost two diodes per voltage level.

Since it uses fewer switches than the SC-CMI, the suggested topology is more effective. a nine-level configuration with an output voltage peak of 320 V. The recommended SC-CHMI performs more efficiently than the SC-CMI. Since fewer switches are used in the proposed architecture than in the SC-CMI, less conduction power loss occurs as a result of switches being in the current path. It is crucial to note that the suggested SC-CMI and SC-CMI topologies are more effective than CTMI and HFLMI topologies because they do not require transformers.

V PROPOSED TOPOLOGY

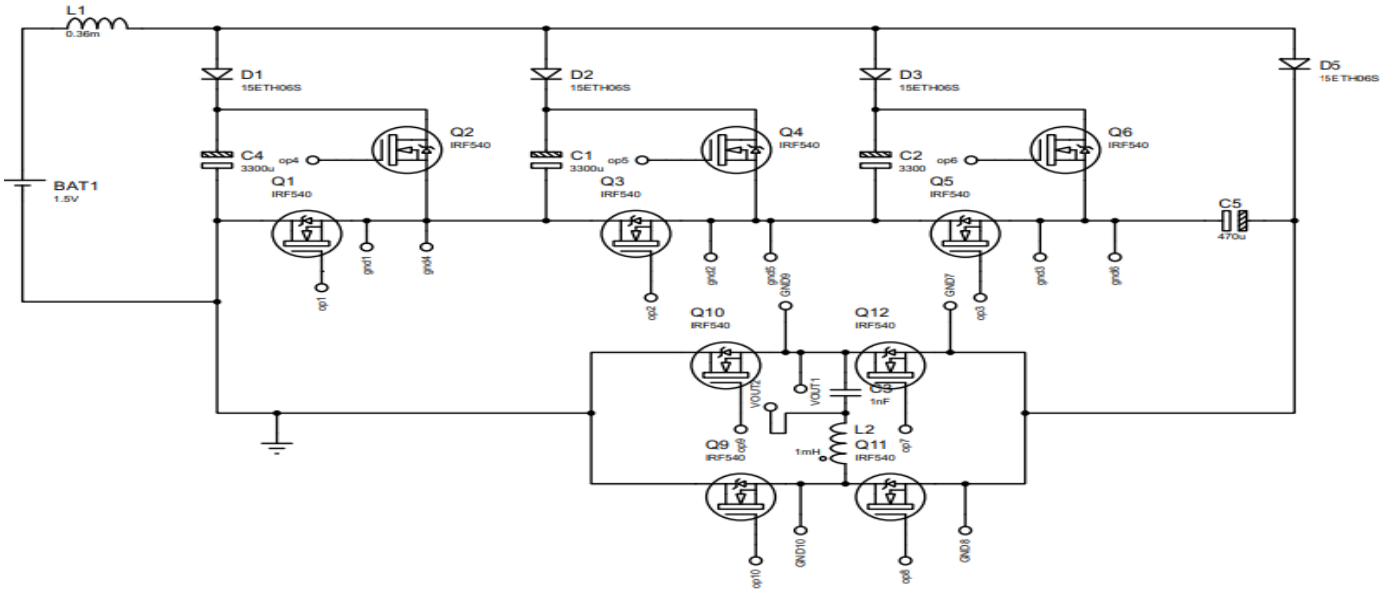

Fig 2: Proposed topology

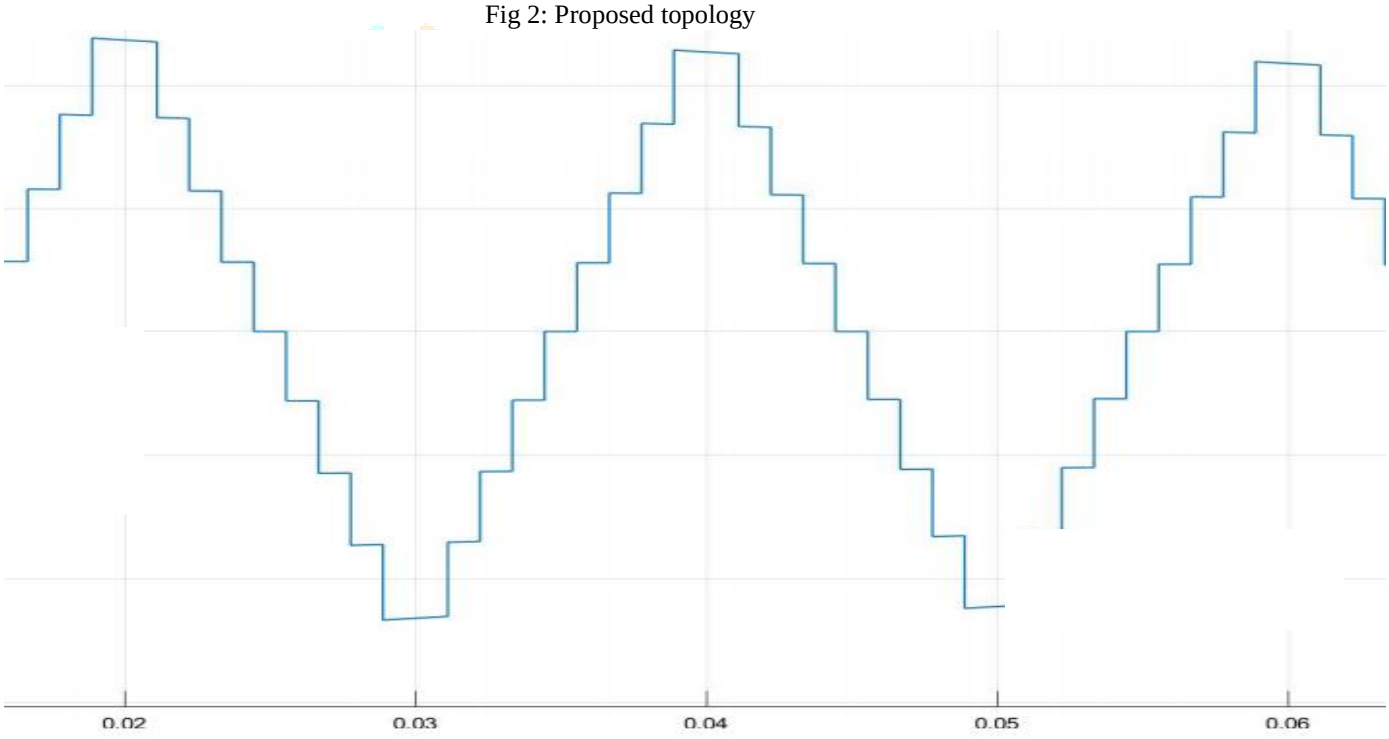

Fig 3 : Simulation of 9 level inverter

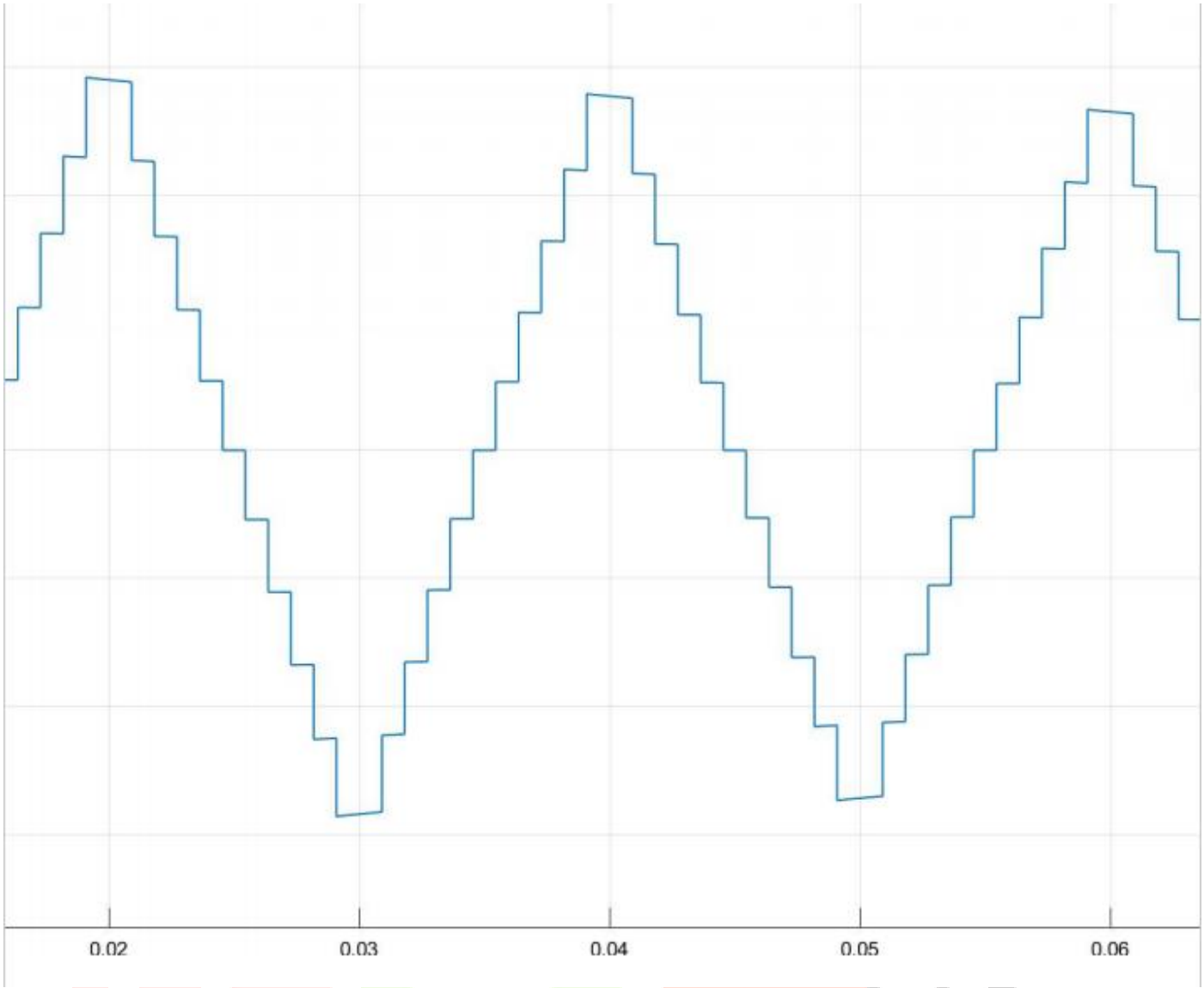

Fig 4 : Simulation of 11 level inverter

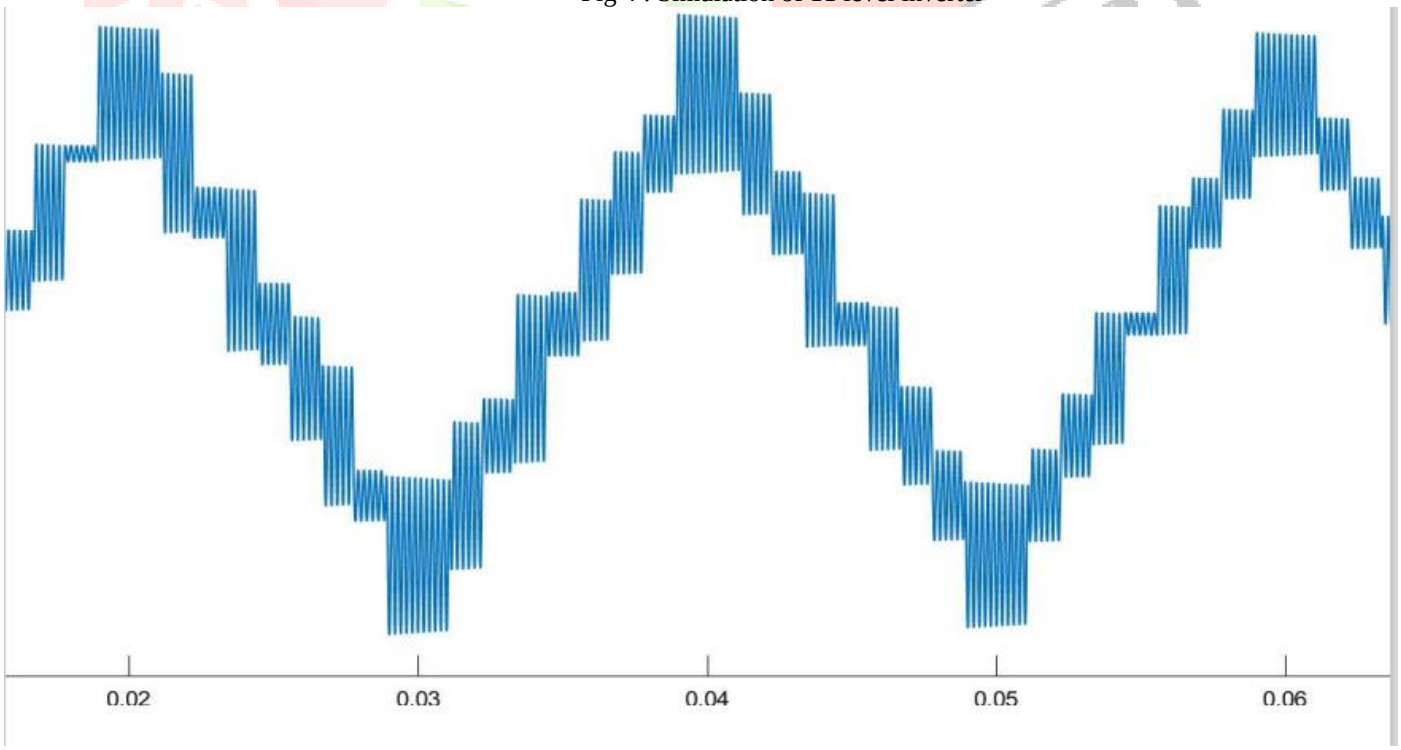

Fig 5 : Simulation of proposed system

VI . SIMULATION RESULTS

To test the effectiveness of the suggested SCCHMI, a simulation of an eleven-level configuration is run in Matlab/Simulink. IEEE Standard 1547 is used to evaluate the proposed SC-CHMI's capacity to supply reactive power with an inductive-resistive load of 0.461 kVA and a power factor (PF) of 0.87. Under the given load condition, the output voltage, load current, and capacitor voltages are displayed, illustrative of the proposed SC-CHMI's capability to supply the required reactive power. As can be observed, the capacitors of the uppermost cells experience a greater voltage ripple than those of the lower ones. Additionally, it is evident from comparing the current that the load's inductive nature causes the high-frequency components of the load current to be filtered out. Consequently, when an inductive-resistive load is applied, the load current has a pure sinusoidal waveform.

The performance of the proposed topology with the front-end dc-dc boost converter under heavy loading conditions is evaluated for a pure resistive load of 5 kW. The produced voltages with and without the front-end boost converter under the stated loading condition. The L-C filter produced pure sinusoidal ac waveform.

VII. CONCLUSION

This paper presented a revolutionary single-source switched-capacitor cascaded half-bridge multilevel inverter (SC-CHMI) with an L-C filter architecture. For the intended SC-CHMI, a single DC supply and fewer switches are required. The suggested topology is more effective and capable of boosting. The proposed SC-CHMI topology also features a modular architecture and may be scaled up to a desired voltage level. In the suggested topology, the capacitors are charged via a charging inductor and L-C filter to lessen repulse and remove inrush currents during the charging stages. The viability and practicality of the proposed topology are verified using the simulation results and the findings of the lab-scale experimental testing. The findings indicate that the proposed SC-CHMI is practical and performs better in terms of capacitance charging currents, reduce ripples.

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