IJCRT.ORG ISSN : 2320-2882

INTERNATIONAL JOURNAL OF CREATIVE RESEARCH THOUGHTS (IJCRT)

An International Open Access, Peer-reviewed, Refereed Journal

Performance Analysis of 16bit-Mac Unit Using Vedic and Booth Multiplier

Samanthapudi Swathi[1], R.Devi[2], D.Bhavani[3], PSSN Mowlika[4], V.Bhavani[5]

[1,2,3,4]Assistant professor, Department of ECE, SRKREC, Bhimavarm-2

[5]Assistant professor, Department of ECE, DNRCET, Bhimavarm-2

Abstract

Multiply and Accumulate operation is one of the fundamental methods in signal processing and other areas (MAC). A digital signal processor's (DSP's) multiplier is the device's single most important physical component. Power consumption, LUT use, and latency are the limited factors in Digital signal processors performance. The development of a low-power, low-latency multiplier is so essential. The study's focus is on finding the best design for a 16-bit MAC unit that employs a multiplier and a carry save adder with a bit depth of 8. We may make use of the booth multiplier as a benchmark. Verilog HDL is used throughout the whole of the design's implementation. Vivado 2018.2 was used for both the synthesis and the simulation. The proposed architecture provides a means of drastically cutting down on the waiting time. The energy consumption is reduced by almost 15% as a result.

Index Terms—Vedic mathematics, carry-save adder, MAC unit, Verilog HDL, Look-up Table.

Introduction

Developing methods to efficiently dissipate power in digital signal processors has risen to the top of the research and development priority list due to increasing consumer demand. There are several methods, such as the use of add-on circuits, for reducing power consumption in VLSI architecture. Common "DSP" operations include MAC, fast-Fourier transforms , and so on [1]. One additional possible operation is convolution. It is believed that the multiplier is an essential part of such procedures. The MAC unit of a DSP has a significant impact on its overall power usage. A MAC device includes Any one of multiplier, an adder to total its partial products, and an accumulator to hold the intermediate totals. That being stated, before working on increasing the MAC unit's speed, the multiplier's speed must be increased to the next tier. Because of this, we use both a carry save adder and Vedic-inspired ancient mathematics. With the use of an 8-bit Vedic-multiplier based on urdhva tiryakbhyam (UT) logic and a carry save adder, this study aims to create a 16-bit MAC unit. The booth multiplier is then used for comparison. The essay then includes short explanations of two techniques to explaining Vedic mathematics after a quick survey of the relevant literature. Presentations of sections two and three are presented separately.

Vedic-mathematics

Vedic mathematics is an ancient system that may be used to many branches of mathematics, from arithmetic to algebra, and which simplifies the mathematical process by doing away with unnecessary steps. There are 16 sutras that serve as the foundation for Vedic mathematics.

Urdhva Tiryakbhyam (UT) and the Nikhilam Navatashcaramam Dashatah both allow for the recording of a pair of identical integers (NND). In addition to the two shown here, there are more than sixteen more sutras available. For numbers with many significant digits, the NND sutra is preferred whereas for numbers with few significant digits, the UT sutra is preferred. This is why the UT sutra is being employed in this effort.

1. Urdhva Tiryakbhyam (UT)

Urdhva Tiryakbhyam, abbreviated UT, means "in an upward direction and cross-wise" [4]. This technique may be used to multiply any of two numbers with any base. Let us Consider the process of multiplication between two three-digit numbers, such as P[2:0] and R[2:0], where S[3:0] is the carry and T[2:0] is the partial product of the multiplication.
When that time comes, we must implement the additional improvements that go along with it.
step1: S0T0 = P0R0
step2: S1T1 = {(P0*R1) + (P1*R0)} + S0
step3: S2T2 = {(P0*R2) + (P1*R1) + (P2*R0)} + S1
step4: S3T3 = {(P1*R2) + (P2*R1)} + S2
step5: S4T4 = {(P2*R2)} + S3
Henceforth, the result = S4T4T3T2T1T0

DESIGN OF MAC

There is an eight-bit multiplier built into the design of a sixteen-digit MAC. It's something that's crossed the minds of 4bit multipliers. The 4-bit multiplier will use the 2-digit multipliers in a manner like how the 2-digit multipliers have been utilized by the 4-bit multiplier. See Figure 1 for an example of the MAC. Figure 2 uses the UT sutra method to illustrate the operation of a two-digit multiplier with half-adders. Nevertheless, because of the time delay it causes, the technique is not applicable to multipliers of higher orders. Many people, as a result, resort to using a carry-save adder to tally the uncompleted things. As with an array multiplier, partial products are made fairly and uniformly in this case.

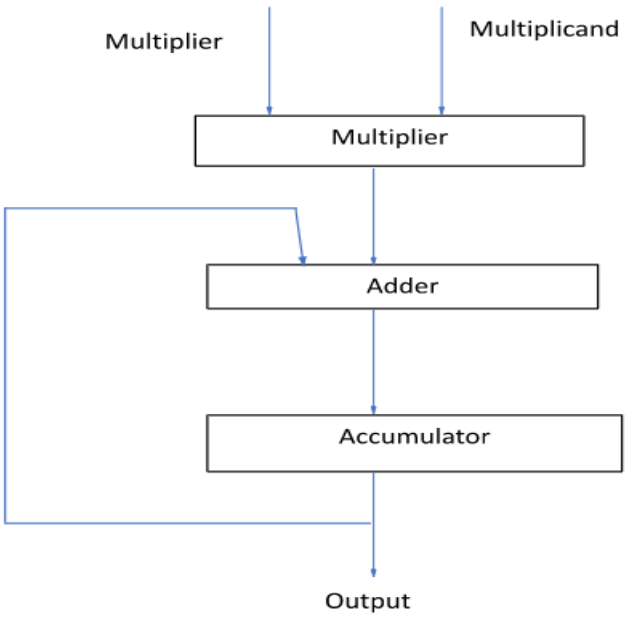

Fig 1 shows Basic MAC Unit

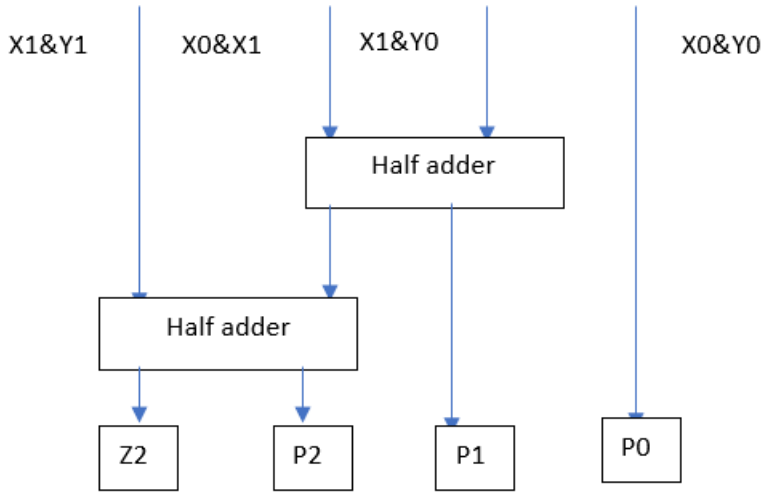

Fig 2 Implementation of Multiplier With Half Adder's

Carry-Save Adder

The addition of integers with bit widths from 3 to n is its most common use. This transformation of the three inputs yields two outputs; one of which deals with carry and the other with partial sum. The final total may be calculated by moving the carry to the left by one bit position and then zeroing off most significant bit (MSB) of the partial sum.

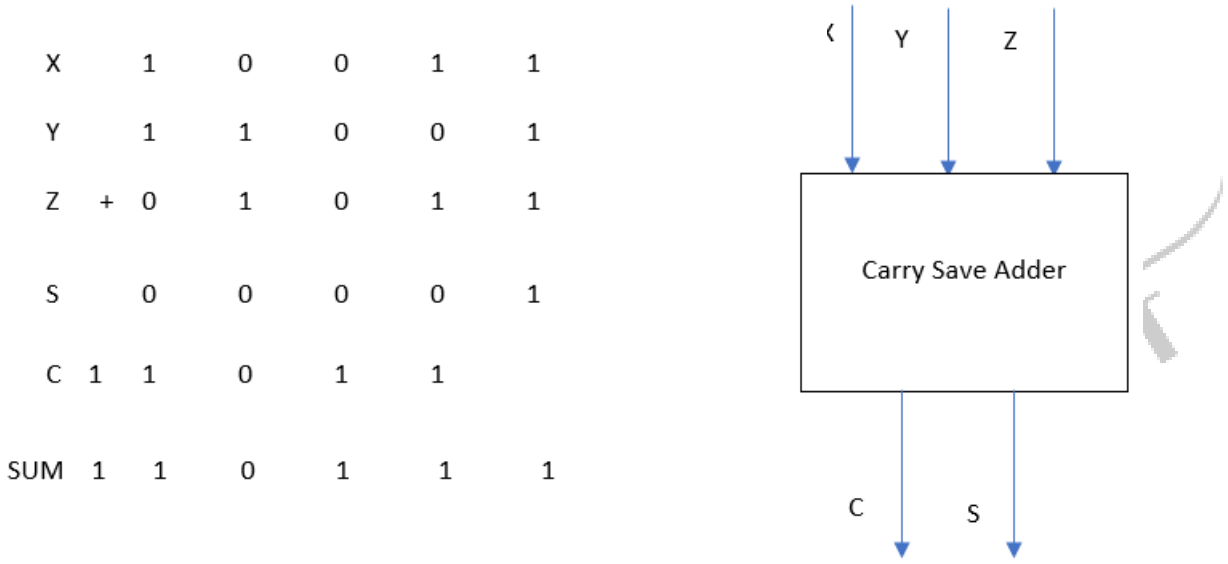

Fig 3 Shows Carry Save Adder Implementation

2. Existing 8 Bit Multiplier

To design the 8-bit Vedic multiplier, four 4-bit multipliers were required. The inputs of a [7:0] and b[7:0] are decomposed into their constituent pieces, a[3:0], a[7:4], b[3:0], and b[7:4]. A 16-bit integer is produced because of the multipliers' operations. The optimal design for an 8-bit multiplier is seen in Figure 4.

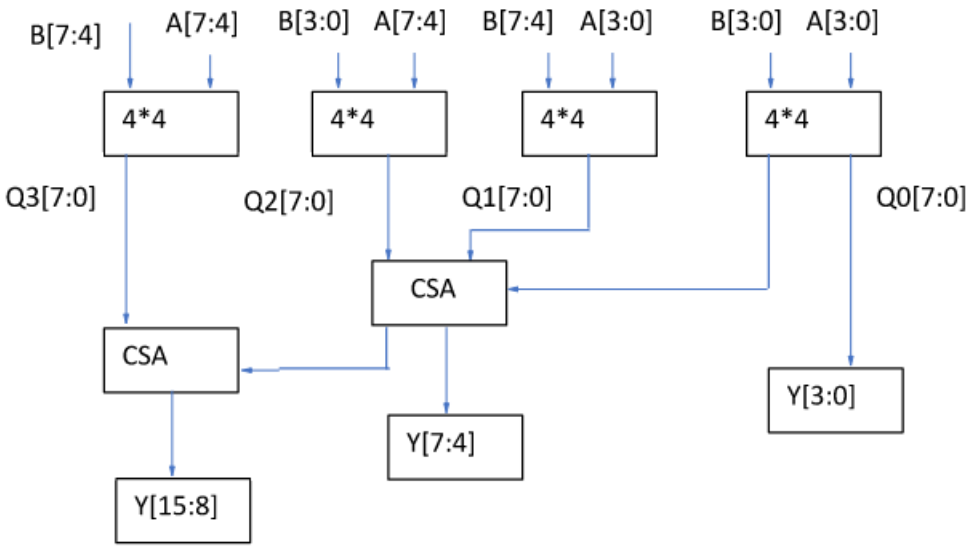

Fig 4 design of 8 bit multiplier using 4 bit multiplier based on LUT sutra

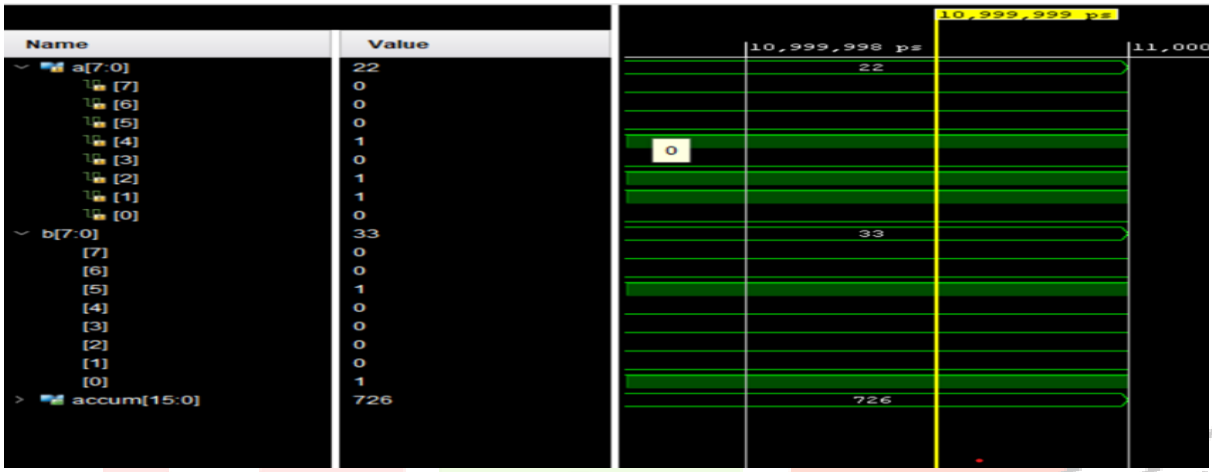

Fig 5 Shows the Timing Diagram for Booth Multiplier

Table 1 Comparison of Parameters for Vedic & Booth Multipliers

Parameters	**16-Bit Booth MAC unit**	**16-Bit Vedic MAC unit**
Power Consumption (W)	13.585	11.377
Delay (ns)	10.790	7.554

3. Conclusion

A 16-bit MAC unit was developed by fusing an 8-bit Vedic-multiplier with a carry save adder and 8-bit booth multiplier. Verilog HDL was used as the programming language, which is based on the Urdhva Tiryakbhyam (UT) sutra. Power usage was reduced by 15%, and latency was cut drastically. There were two sets of numbers crunched: one with the old multiplier, and one with the new one. The recommended booth multiplier is compatible with the corresponding MAC unit, which was designed for DSP tasks. Programmers

might utilize this to improve efficiency. Potential future work might include replacing the multipliers with reversible logic gates in an effort to further minimize power usage and increase overall performance.

References

1 Dwivedi, Kavindra & Sharma Sharma, R.K. & Chunduri, Ajay, "Hybrid Multiplier- Based Optimized MAC Unit", 2018 9th International Conference on Computing, Communication and Networking Technologies (ICCCNT), Bangalore, 2018, pp.1-4

2 .Jithin S, Prabhu E "Parallel Multiplier - Accumulator Unit based on Vedic Mathematics", in ARPN Journal of Engineering and Applied Sciences, Vol.10, no.8, pp. 3608-3613, May 2015.

3. S. N. Gadakh and A. K. Khade, "Design and Optimization of 16×16 Bit Multiplier Using Vedic Mathematics", in proc. Int. Conf. on Automatic Control and Dynamic Optimization Techniques, 2016.

4. K. Bathija, R & S. Meena, R & Sarkar, S & Sahu, Rajesh "Low Power High Speed 16x16 bit Multiplier using Vedic Mathematics", in International Journal of Computer Applications. 59. 41- 44. 10.5120/9556-4016.

5. M. V. Durga Pavan and Ramesh. S R, "An Efficient Booth Multiplier Using Probabilistic Approach", in 2018 International Conference on Communication and Signal Processing (ICCSP), Chennai, 2018, pp. 365-368.

6. L.Ranganath, D. Jay Kumar, P. Siva Nagendra Reddy, "Design of MAC Unit in Artificial Neural Network Architecture using Verilog HDL", in international conference on Signal Processing, Communication, Power and Embedded System (SCOPES)-2016.

7. Carry-Save Addition. Prof. Loh. CS3220 – Processor Design - spring 2005.

8. R. Balakumaran and E. Prabhu, "Design of high-speed multiplier using modified booth algorithm with hybrid carry look-ahead adder", in 2016 International Conference on Circuit, Power and Computing Technologies (ICCPCT), Nagercoil, 2016, pp. 1-7.

9. A. Eshack and S. Krishnakumar, "Implementation of Pipelined Low Power Vedic Multiplier", in 2nd International Conference on Trends in Electronics and Informatics (ICOEI), Tirunelveli, 2018, pp. 171-174.