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A CHAMELEON PROCESSOR-DIRECTED METHOD FOR CONCEALING CONFIGURATION LATENCY

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Abstract: Currently, too many architectural boundaries are crossed in chip design. Nobody has found out how to make a chip fit every need for the ideal consumer product. But I think we're getting there. A new type of chip can now adapt to any programming requirement by wiping its existing hardware design and creating new hardware that is ideal for running the required software. Reconfigurable processors is the term used to describe these semiconductors. These new chips can instantly rewire themselves to build the precise hardware required to execute a piece of software at the highest speed. The name of this new chip is CHAMELEON CHIP.

Index Terms **- Global Overview, General Simulation Flow, Test Case Generation.**

I. INTRODUCTION

Chameleon is a program of next-generation microprocessors developed by SGS-THOMSON Microelectronics. It is based on a modular, core-based 64-bit superscalar architecture. The first microprocessor generation is targeted at the consumer computing market. It implements multi-media features, as well as common microprocessor capabilities. For such highly complex microprocessor developments, functional verification is estimated to take between 30 and 50% of the design resources. Imperfections in the verification process not only affect time to market but also lead to costly mask revisions. The goal of silicon design functional verification is to gain a high level of confidence that the silicon implementation satisfies the specification of behavior. To achieve the verification of such a highly complex chip, and to ensure quality improvement throughout the design process, different technologies are used: simulation, acceleration, emulation, test generation, formal verification, and ASIC prototyping. Priority is given to the objective of reaching a high level of confidence in the first stages of the design. In fact when the physical design starts, the RTL (Register Transfer Level) specification has already been verified by running billions of machine cycles and making use of as much as possible of formal verification techniques. Each step of the physical design is checked versus the RTL specification.

This paper explains the functional verification methodology used for the design of Chameleon processors. It consists of 2 major points:

-verify that the VHDL specification is conformant to architecture and microarchitecture specifications.

-verify that actual layout is conformant to the VHDL specification.

The first issue is addressed in Sections 2 (Description levels), 3 (Simulation-based verification) and 4 (Sequential verification). Verification of the VHDL reference specification uses both simulation-based (including acceleration and emulation) and formal verification-based techniques. The second issue is addressed in Section 5 (Circuit verification): transistor abstraction and combinational formal proof are the primary mechanisms used for circuit-level verification.

Fig.1: Chameleon Chip

II. LITERATURE SURVEY

Mikel Luján, Javier Navaridas, and Sebastian Werner, ACM Computing Surveys (CSUR), 50(6), 1-37, 2017. It is commonly acknowledged that silicon photonics (SiP), which enables optical on-chip data transfer, is a vital technology for overcoming the bandwidth and energy constraints of electrical interconnects. Optical Networks-on-Chip (ONoCs), a fascinating new research area that has been attracting a lot of attention from the community, may be integrated into the on-chip communication fabric. However, SiP materials and devices are still in the early stages of development, and dealing with optical data transmission on a chip presents designers and researchers with a completely new set of difficulties and problems. Developing effective ONoCs is a difficult endeavour that calls for in-depth knowledge of everything from on-chip traffic patterns and needs to the physical layout and effects of combining both electronic and photonic components. We present a thorough analysis of recently suggested ONoC designs in this work, point out their advantages and disadvantages, and list current topics of development. Furthermore, we cover current research initiatives in key enabling technologies that are necessary for a potential widespread commercial use of ONoCs. These technologies include on-chip and adaptive laser sources, automatic synthesis tools, and ring heating approaches.

2005, 645–678 in IEEE Transactions on Neural Networks, 16 (3) Adaptability must be enabled for a design to endure unanticipated physical consequences like ageing, temperature change, and/or the advent of new application requirements. Reconfigurable processors have full strength adaptability, which makes it a crucial IP in contemporary System-on-Chips (SoCs). Over the past ten years, reconfigurable processors have become a prominent computing platform across embedded, general-purpose, and high-performance application domains. Identifying the benefits of reconfigurable platforms, their modelling, implementation process, and finally towards early commercial acceptance are just a few of the many areas where significant progress has been made. This study examines these advancements from a number of angles, placing special emphasis on underlying problems and potential remedies. With the use of historical analysis, a roadmap for future study is suggested.

The 21st Saudi Computer Society National Computer Conference will be held from January 6 to 12, 2018. Multi-Processor Systems-On-Chips (MPSoCs), which integrate hundreds or thousands of cores on a single die, are developing as a key technology for the Internet of Things (IoT) sector. However, the on-chip connection network between the cores is the main issue and a crucial performance limiting factor for MPSoCs. The development of hybrid and optical NoCs has become a workable solution. This work examines the major contributions of newly presented optical/hybrid NoC architectures in a thorough review. A thorough analysis of the performance parameters, such as latency, throughput, and power/energy efficiency, has been conducted, offering insightful information about ONoC/HNoC architectures. Also, a thorough description of recent developments in optical/hybrid interconnects is explored in the proposed work. The ramifications of upcoming research efforts can be understood based on the comparison of various on-chip connecting techniques.

III. OBJECTIVES

Modern modeling techniques include compact models for the active and passive components, field solving, model order reduction algorithms, and tools for simulating such devices, such as those created in the FP5/IST project CODESTAR. Unlike the CODESTAR project, which focused on developing design tools for studying the coupling of electromagnetic effects by examining basic design components like spiral inductors, varactors, capacitors, and interconnects, here we will build on these findings by actually combining them via the proposed "hierarchical field solving using compact models with connectors" paradigm with the aim of handling full circuit blocks rather than just one or a small number of them. Reassessing the modeling processes and premises is necessary. The behavior these blocks is becoming more sensitive to outside elements that are challenging to regulate, which complicates the development of the design techniques even more. Rising manufacturing variability is a result of shrinking feature sizes. The dependence on temperature and other operating factors also grows as operation frequencies rise.

The consortium's overall goal is to create a methodology and prototype tools that can take a layout description of typical RF functional blocks that will operate at RF frequencies up to 60 GHz and convert it into electrical simulation models that are sufficiently accurate and reliable while also taking variability into account.

The major objective of the project is the silicon-accurate modeling of RF functional blocks (such as a VCO or an LNA) with up to 10 transistors, and 10 passive devices, implemented in 90 and 180-nanometer technology, and for frequencies up to 60 GHz, with a maximum of 10 levels of metal.

IV. METHODOLOGY

4.1 Simulation-based verification

4.1.1 Global overview

The key feature of the adopted methodology is that functional verification is carried out at the chip level. Before integrating their blocks into the entire model, the designers must validate each of their blocks using the proper testbench. Following the integration of the various parts into the overall model, chip-level verification is used to functionally validate the VHDL specification.

4.1.2 General Simulation Flow

The following diagram illustrates the overall process for chip validation, from test generation to a comparison of the hardware models and the software simulator.

4.1.3 Test Case Generation

A test plan with two components—architectural verification and implementation verification—drives the creation of tests. The chip's adherence to its architectural specification is tested in the first section. Without taking into account implementation difficulties, architecture verification tests try to confirm access to and updating of architectural resources as stated in the architecture manual. They aim to stress the architecturally visible resources in a similar way to how a chip user might by utilizing the CPU in a system and running a programmer on it.

Known as Architectural Verification Patterns (AVP) and Implementation Verification Patterns (IVP), both components lead to the creation of tests. These tests are essentially assembler programs that are either directly generated as binaries to avoid the restrictions and optimizations applied by the assembler-linker, or they are compiled with the Chameleon software toolchain (assembler-linker) to produce Chameleon microprocessor binary code. Programs for Assembler can be developed by hand or automatically generated. Both an internal tool and the Chameleon Test Generator (CTG), which is based on model-based technology created by IBM research laboratories in Haifa, are used by Chameleon.

The internal tool produced tests for the verification of an internal project-developed Chameleon ASIC prototype. A test database of 17 million clock cycles was created, all of which were AVPs and single instruction based (that is, dependencies between instructions are not taken into account for example). Thus, the team decided to use CTG because the needs in terms of test creation were greater for the verification of the Chameleon.

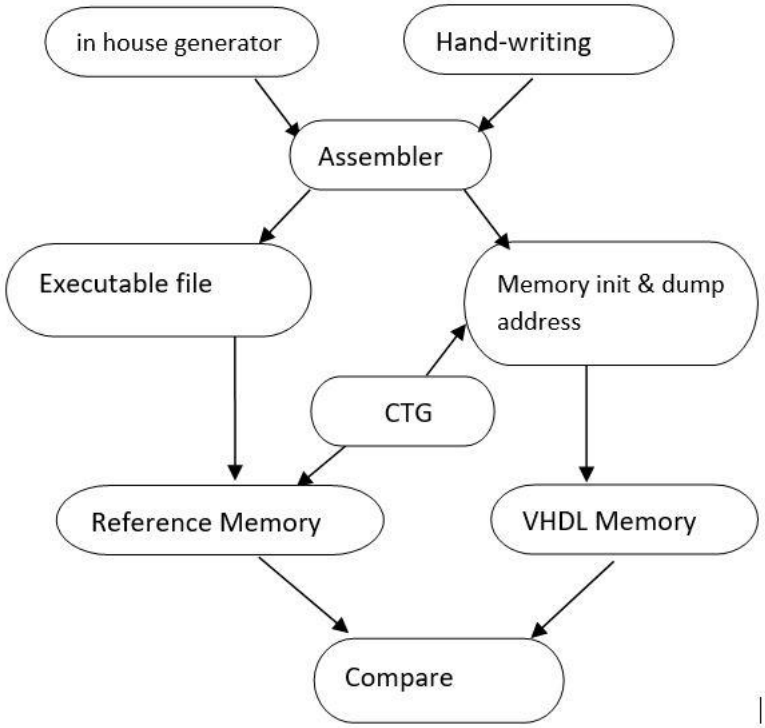

Fig.2: Simulation flow chart

V. ARCHITECTURE

The Chip incorporates three core architectural technologies:

5.1 A Complete 32-bit Embedded Processor system

It offers a 32-bit ARC processor, 32-bit interface, and 64-bit high-performance memory controller, which are all essential components for a full system. Design, debugging, and verification are made simpler by these fully integrated and verified modules.

5.2 A high-performance 32-bit Reconfigurable Processing Fabric (RPF)

The RPF contains 108 parallel computation units, which offers a lot of processing capability. The "hard lifting" (Rec Roadrunner Bus connections between these system elements) happens here. This 128-bit split-transaction bus gives the RPF and embedded processor system's subsystems a 2GByte/sec on-chip bandwidth.

5.3 Data and Sources of Data

These fundamental technologies work together to end the performance/flexibility trade-off, take advantage of platform-based design, and let you use your own algorithms to distinguish your product.

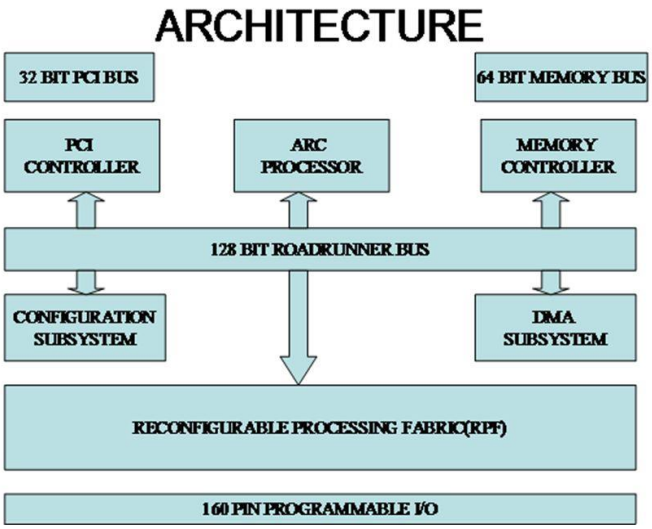

Fig. 3: Architecture

VI. CONCLUSION

Setting up solid verification procedures becomes increasingly necessary as the size and complexity of the design rise. Modern methods are employed in the SGS-THOMSON Microelectronics Chameleon project to handle this difficulty. An RTL VHDL description serves as the basis, and functional verification is completed by performing tests that require billions of machine cycles. Technologies for acceleration and emulation significantly boost the power in terms of simulated cycles per second and offer a respectable turnaround time. Where possible, formal verification approaches are utilized to supplement the specification's verification. Combinational proof has reached a level of maturity where it can be used nearly exclusively for circuit-level verification. This methodology's major goal is to leverage cutting-edge technologies like acceleration, emulation, and formal verification within the very initial stages of the design process rather than after physical design. Beginning with a functional specification that can be used as a reference at each stage, the design implementation reduces the possibility of running into significant functional issues right before tape out.

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