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A Single-Phase Asymmetrical Multilevel Inverter Topology with Minimum Number of Switches for Renewable energy sources

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Abstract: An induction motor drive inverter with a decreased number of switches is shown. If you're working with medium or high voltage power electronic drives, a multilevel inverter is your best bet. Utilizing a unique ability to synthesize a sine wave with fewer harmonics using several DC sources. For high voltage applications, this concept presents a three-phase framework that may be expanded in both modular and cascaded configurations. Using just four active switches in the conduction channel, this topology may create negative polarity without an H-bridge structure, which reduces power losses and voltage stress on the switches. Using the PSO method, this work presents a novel way of determining the optimal magnitude of DC sources because of the wide range of switching patterns that may be used. The optimal switching angle (OSA) modulation method is used to calculate the ideal switching angles via the PSO algorithm to increase voltage quality and decrease total harmonic distortion (THD). 25 and 31 level MLI is designed and analyzed result using the suggested topology and its optimization technique are shown to be viable.

Index Terms **- Multilevel Inverter (MLI), Voltage Quality, Particle Swarm Optimization (PSO).**

I. INTRODUCTION

For many years, industries have relied on induction motor drives to provide precise control over speed. This is due to the induction motor's simple design and low maintenance requirements. Asymmetrical Multilevel Inverter topology's for reduced switches is feasibility and its optimization approach is validated by a single-phase prototype utilizing 15- and 25-levels [1]. For induction motor driving applications, multilevel inverters (MLI) are becoming more common [2-4]. Medium to high-voltage and high-current driving applications call for it in particular. Multilevel inverters provide several benefits over regular inverters. THD, switching losses, power quality, and decreased electromagnetic interference are the main benefits (EMI). The reduced voltage stress on each component is the primary benefit of a multilevel inverter [5-9]. Multilevel inverter topologies may be broken down into three sorts. They are flying capacitors, diode clamped, and H-bridge cascaded multi-level inverters.

For medium voltage (MV) drives, the most common inverter architecture is the H-bridge multilevel inverter. Single-phase H-bridge power cells make up the majority of the structure. In reality, the number of power cells in an H-Bridge inverter is controlled mostly by its operating voltage and manufacturing costs. For the same voltage level, the H-bridge multilevel inverter needs fewer components than any other form of the inverter [10,11]. Various modulation strategies were developed as a result of the evolution of multilayer inverters [13]. However, because the output of these inverters has a higher harmonic content, it is preferred to use pricey and large low pass passive filters before supplying the electricity to the utility grid. Furthermore, the use of these inverters in high power applications is discouraged by high voltage stress and considerable switching loss. [14]. Voltage fluctuations, an increase in loss, improper functioning, and a negative influence on power quality are the main effects of those harmonics. The aforementioned problems can be successfully resolved by implementing an effective control strategy for an MLI [15]. Nine alternative reduced switch MLI (RS MLI) topologies were explored on both quantitative and qualitative grounds by the authors in [16], and a review of only a few cross-connected sources-based MLI topologies was provided in [17]. Agrawal and Jain [18] have studied only six RS MLI topologies for grid-tied applications.

Asymmetrical reduced component count MLI architecture with numerous DC sources and the ability to create both positive and negative voltage levels without the aid of an extra series H-bridge section is proposed in this work. Each module's current loop has three active switches instead of the usual four, resulting in lower power losses and higher overall efficiency. As a three-phase construction, it may be readily enlarged and features modular and cascaded connections as well. Instead of employing typical algorithms (binary, trinary, and other algorithms) and mathematical operations, an optimization process based on the PSO algorithm is given for determining the optimal voltage magnitudes of DC sources. In next section discussed about operating principles of proposed MLI.

II. PRINCIPLES OF OPERATION FOR THE PROPOSED MLI

Multilevel inverters are emerging as widely used and most recent types of breakthroughs in the use of power electronics. It produces a desired output voltage waveform from a variety of dc sources utilized as input to the inverter. There are methods for enhancing the output voltage and performance. First, an unique architecture for a multilevel inverter is presented, which decreases the count of switches when compared to different stages of output voltage. Second, a stepped waveform technique to selective harmonics removal is employed to exclude the lower order harmonics.

To generate a staircase AC output voltage, separate dc-sourced full-bridge modules are connected in series. The 3-stage converter given rise to the name "multilevel." As a result, various multilevel converter topologies were devised. The benefits of cascading multilevel inverters for motor drives and application packages were noteworthy. Because of the high need for medium - voltage high - strength inverters, the cascade type inverter has sparked a lot of interest. These multilevel inverters can increase the inverter's rated voltage and energy by expanding the voltage ranges. It can also enhance the equivalent switching frequency without increasing the actual one (switching frequency), lowering the ripple element output voltage of the inverter and effects like electromagnetic interference etc.

Multilevel converter can be used in a variety of unusual ways. To shape the desired waveforms, the most successful way uses a parallel or collection connection of classic converters. Highly complex structures place converters within converters successfully. Voltage or current rating of the multilevel converter becomes more than one of the character switches, and therefore the converter's power rating might surpass the limit set by the character switching devices.

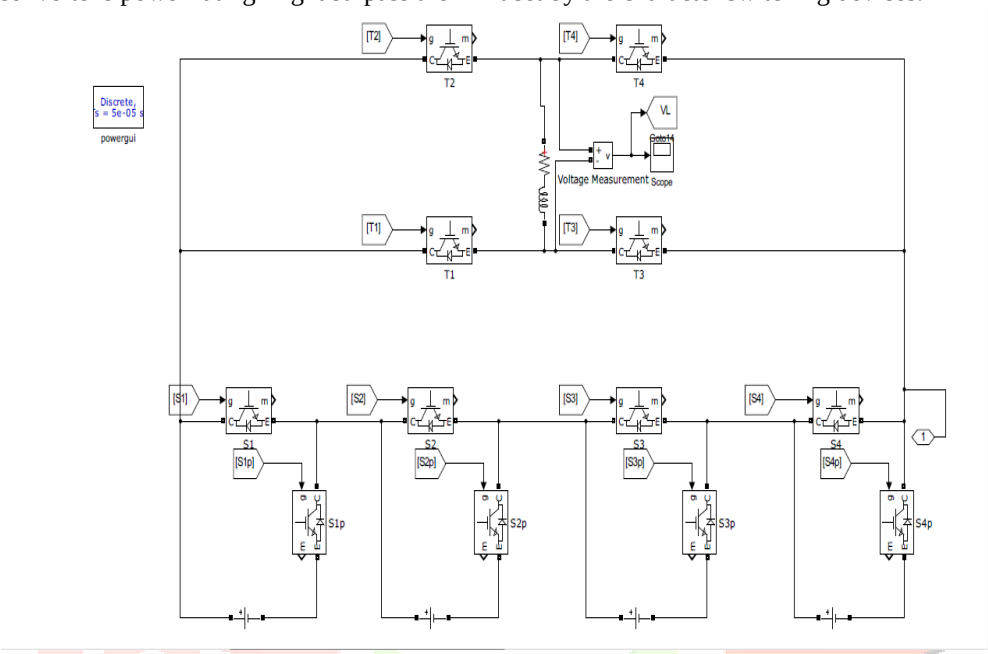

Fig. Proposed Matlab/Simulink model for 31-level Multi Level Inverter output

The suggested MLI architecture lowers the number of on-nation switches in each module's current loop to a few active switches, lowering strength losses and increasing total performance.

Switches ON	Voltage Level (V_{out})
T_2, S_{1P}, S_{2P}, S_{3P}, S_{4P}, T_3	+7.5 V_o
T_2, S_1, S_{2P}, S_{3P}, S_{4P}, T_3	+7 V_o
T_2, S_{1P}, S_2, S_{3P}, S_{4P}, T_3	+6.5 V_o
T_2, S_1, S_2, S_{3P}, S_{4P}, T_3	+6 V_o
T_2, S_{1P}, S_{2P}, S_3, S_{4P}, T_3	+5.5 V_o
T_2, S_1, S_{2P}, S_3, S_{4P}, T_3	+5 V_o
T_2, S_{1P}, S_2, S_3, S_{4P}, T_3	+4.5 V_o
T_2, S_1, S_2, S_3, S_{4P}, T_3	+4 V_o
T_2, S_{1P}, S_{2P}, S_{3P}, S_4, T_3	+3.5 V_o
T_2, S_1, S_{2P}, S_{3P}, S_4, T_3	+3 V_o
T_2, S_{1P}, S_2, S_{3P}, S_4, T_3	+2.5 V_o
T_2, S_1, S_2, S_{3P}, S_4, T_3	+2 V_o
T_2, S_{1P}, S_{2P}, S_3, S_4, T_3	+1.5 V_o

T_2, S_1, S_{2P}, S_3, S_4, T_3	+1 V_o
T_2, S_{1P}, S_2, S_3, S_4, T_3	+0.5 V_o
T_2, S_1, S_2, S_3, S_4, T_3	0
T_1, S_{1P}, S_2, S_3, S_4, T_4	-0.5 V_o
T_1, S_1, S_{2P}, S_3, S_4, T_4	-1 V_o
T_1, S_{1P}, S_{2P}, S_3, S_4, T_4	-1.5 V_o
T_1, S_1, S_2, S_{3P}, S_4, T_4	-2 V_o
T_1, S_{1P}, S_2, S_{3P}, S_4, T_4	-2.5 V_o
T_1, S_1, S_{2P}, S_{3P}, S_4, T_4	-3 V_o
T_1, S_{1P}, S_{2P}, S_{3P}, S_4, T_4	-3.5 V_o
T_1, S_1, S_2, S_3, S_{4P}, T_4	-4 V_o
T_1, S_{1P}, S_2, S_3, S_{4P}, T_4	-4.5 V_o
T_1, S_1, S_{2P}, S_3, S_{4P}, T_4	-5 V_o
T_1, S_{1P}, S_{2P}, S_3, S_{4P}, T_4	-5.5 V_o
T_1, S_1, S_2, S_{3P}, S_{4P}, T_4	-6 V_o
T_1, S_{1P}, S_2, S_{3P}, S_{4P}, T_4	-6.5 V_o
T_1, S_1, S_{2P}, S_{3P}, S_{4P}, T_4	-7 V_o
T_1, S_{1P}, S_{2P}, S_{3P}, S_{4P}, T_4	-7.5 V_o

III. MODULATION STRATEGY

The best switching angle modulation approach is used in this work to organize the power switches. Selecting the optimal switching angles improves output voltage quality using this method. Switching losses and total harmonic distortion (THD) are reduced when this technology is used. The output voltage is free of DC terms and even harmonics when done in this manner. Based on Fourier analysis, the output voltage function is as follows:

$$\begin{cases} V_{L1} = \sum_{j=1,3,5}^{\infty} \frac{4V_{DC}}{j\pi} \cos(jA_1) \\ V_{L2} = \sum_{j=1,3,5}^{\infty} \frac{4V_{DC}}{j\pi} \cos(jA_2) \\ \dots \\ V_{L\frac{(n-1)}{2}} = \sum_{j=1,3,5}^{\infty} \frac{4V_{DC}}{j\pi} \cos(jA_{\frac{(n-1)}{2}}) \end{cases} \quad (1)$$

$$V_{out} = V_{L1} + V_{L2} + \dots + V_{L\frac{(n-1)}{2}} \quad (2)$$

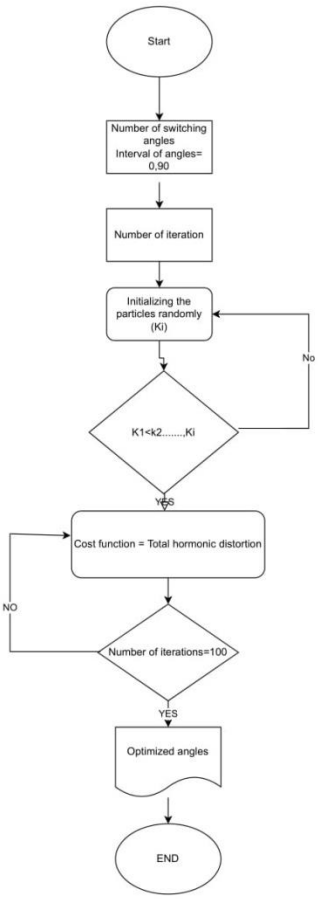

Figure : Flow chart of the particle swarm optimization method that was used to identify the best angles

The number of switching angles is defined by the number of output voltage steps. n2 1 is the value of this parameter (there is one angle at each level, as shown in Figure. The switching angle intervals are taken into account [0 2]. All 50 iterations are equivalent in population size nP OP and iteration count. K1°K2°, ..,Ki° establishes the conditions for the computation of a Fourier series and the subsequent assessment of THD. As a cost function, the THD must be minimized using the method referred to above.

The obtained THD from the OSA modulation technique in this study is better than the obtained optimum results in [13].

IV. RESULTS

Figure 6 to figure 10 illustrate the complete simulation results.

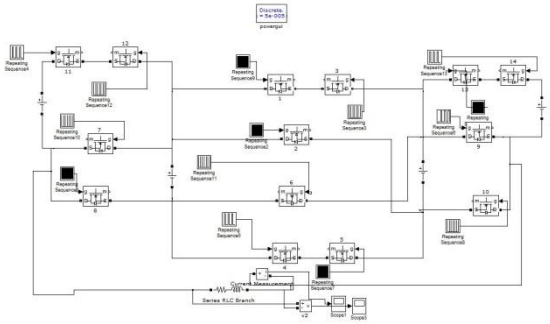

Figure 6: Simulink Diagram of 25 Level Inverter R-L Load

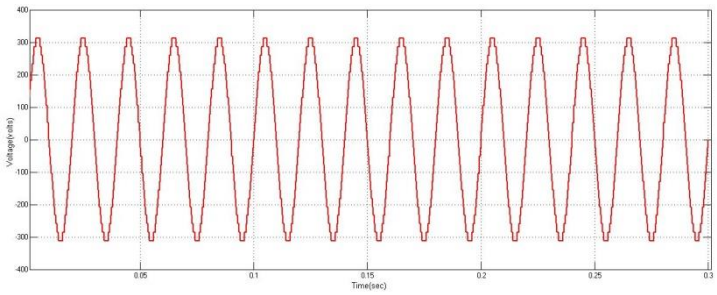

Figure 7: Simulation waveform of 25 Level Inverter with R-L Load Output Voltage

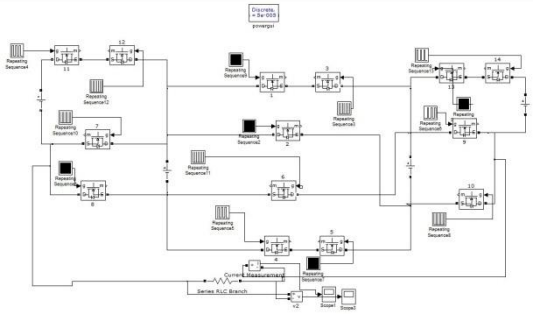

Figure 8: Simulink Diagram of 25 Level Inverter R Load

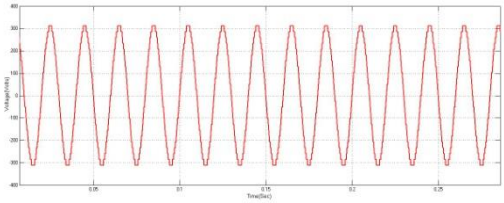

Figure 9: Simulation waveform of 25 Level Inverter with R Load Output Voltage

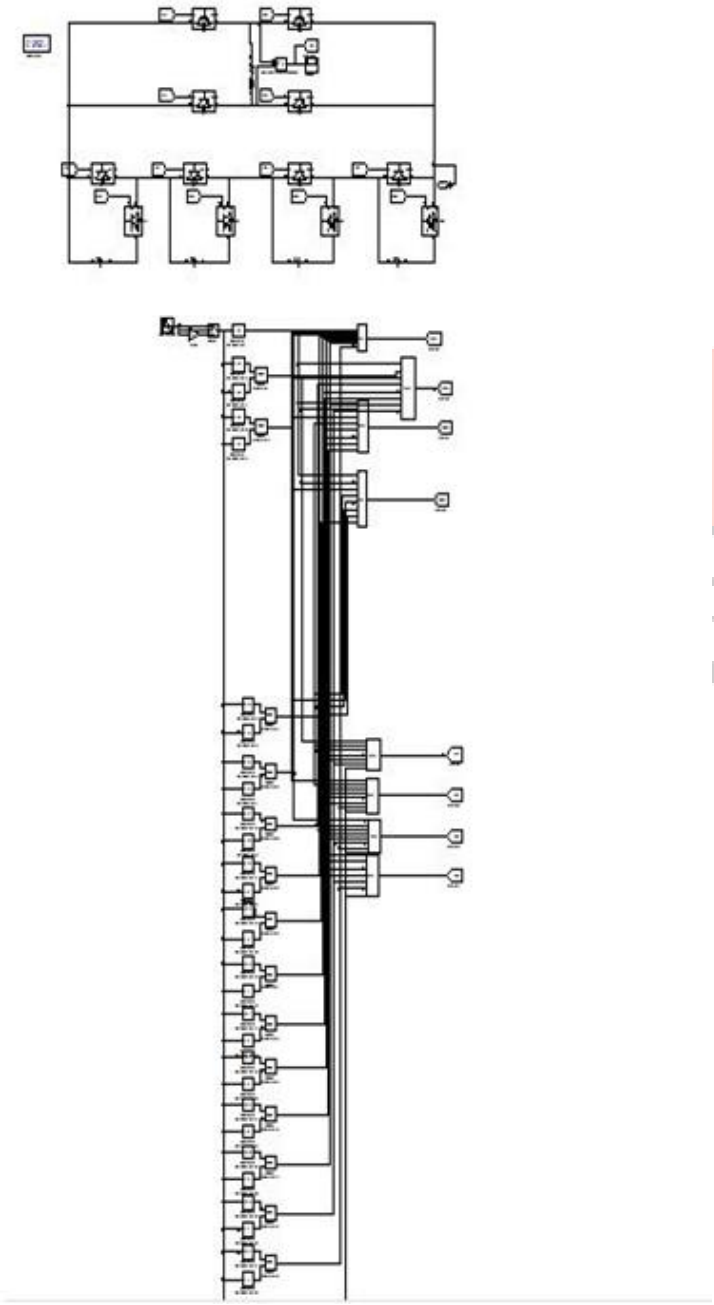

Figure 10: Simulink Diagram of 31 Level Inverter R-L Load

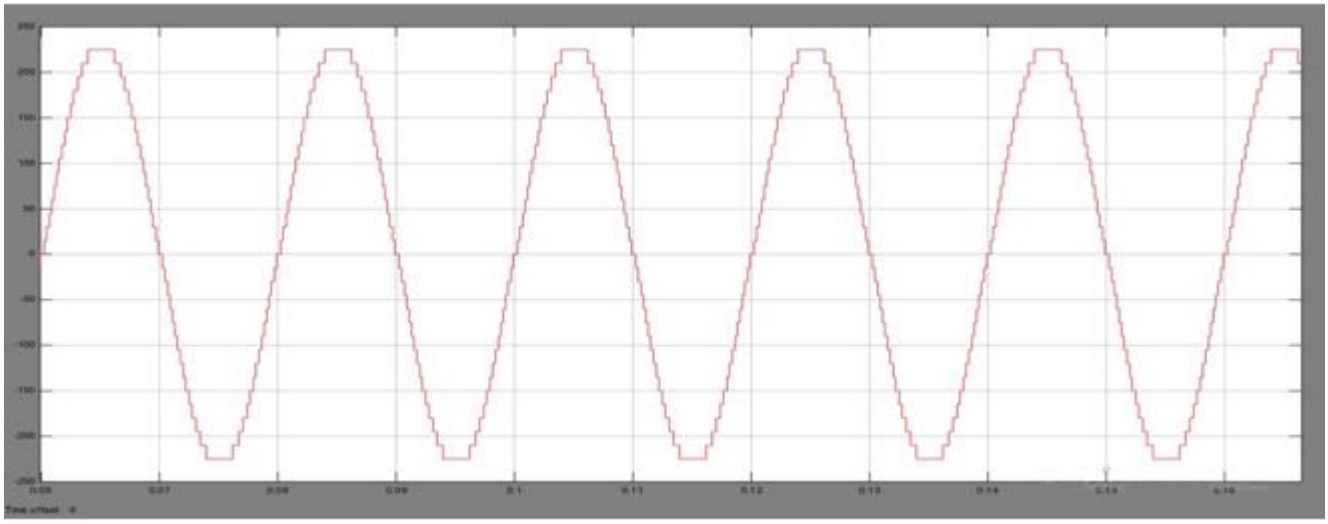

Figure 11: Simulation waveform of 31 Level Inverter with R-L Load Output Voltage

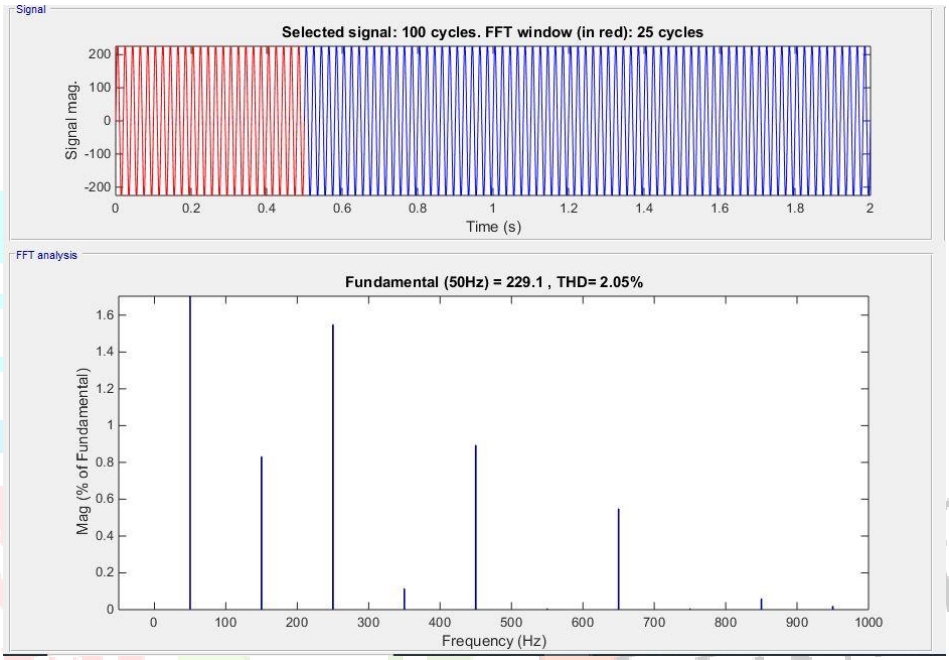

Figure 12: THD calculation of 31 level inverter output

Simulation results of the proposed topology using a 31-level inverter with optimized switching angles are presented in Fig. 11. The stepped waveforms of the output voltage and current are presented. Total harmonic distortion of above MLI is 2.05% only. In [1] 25 level MLI is designed it has THD of 7.60%, In 31 level MLI THD value is very low is achieved. Simulation circuits of proposed MLI also shown in figure 10. Higher order harmonics all are eliminated completely, only 3rd , 5th order harmonics only present, and these values are also very less. This proposed concept reduces THD value to 2%.

V. CONCLUSION

A novel multilevel inverter design has been presented. Renewable energy production is claimed to be achieved using the proposed topology, which is a unique asymmetrical MLI with a decreased component count. Extending the suggested topology to a three-phase structure and modular or cascaded connections is a piece of cake. Power switches may be less stressed by using them in high-voltage applications. In the proposed MLI, the ability to create negative voltage levels without a series H-bridge module reduces power losses. Module voltages may be created using just four on-state power switches. To lower the overall blocking voltage, the PSO method is utilized instead of more usual techniques or algorithms to optimize the magnitude of the DC sources. For example, the suggested optimization technique allows for all potential combinations of input DC sources to be taken into account when determining voltage levels. Furthermore, it may be used on any MLI topology. A low switching frequency was employed in conjunction with OSA modulation and PSO algorithm-optimized switching angles. To thoroughly evaluate the proposed topology against other existing MLI topologies, numerous indicators are used in the comparison process. In comparison to previously published topologies, the suggested topology has better performance and suffers fewer losses.

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