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Multi-Level SMES-Based DVR for Improving Voltage Quality in Primary Distribution Network

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Abstract: A dynamic voltage restorer (DVR), intended to protect customers from voltage changes, is one of the modern power electronic controllers in the distribution system. The distribution system's voltage signal is organized by DVR output compensating signals. To increase voltage quality, this study introduces SFCL's fault current limiter and SMES's integrated DVR. The performance of the SMES integrated DVR for improving voltage quality is considered to be presented during voltage sag conditions. Furthermore, because of the additional voltage enhancement offered by SFCL, the power that DVR injects into the load is reduced. Utilizing MATLAB/Simulink, the simulation model and outcomes are analyzed.

Index Terms - Dynamic voltage restorer (DVR), Voltage quality

I. INTRODUCTION

Voltage variations and short-circuit failures are the two main issues that modern power systems must handle [1], [8]. The grid has generators that use renewable energy sources (such as wind and solar) and can provide a range of outputs. Additionally, the popularity of distributed generation and the exponentially rising demand for power have raised fault current levels.

To reduce voltage fluctuations, a dynamic voltage restorer (DVR) may produce a compensation voltage that is introduced into the grid via a series transformer [12]–[16]. However, when there is a fault, a significant short-circuit current will be introduced into the VSI via a transformer. An alternative for this issue is a bypass strategy. The DVR can be taken down as a "fail-safe" system [6]. Enhancing DVR effectiveness is a different strategy [20]. The series compensator can perform load-side voltage restoration for upstream faults and current restriction for downstream faults thanks to the control techniques depicted in [20]. This method's drawback is that a sizable storage system is required on the dc side. The proposed method also includes a varistor and a few antiparallel thyristors that are connected in parallel to the series transformer's secondary winding [6]. The main method of protection is a varistor, and it is challenging to produce the low-saturation magnetic properties of the series transformer. Nevertheless, the architecture simply shields the series VSI from the excess current and does not prohibit big currents from flowing in the system [2].

The topologies of fault current limiters (SFCLs), superconducting magnetic energy storage (SMES), solid-state SFCLs, and resonance-type SFCLs, on the other hand, differ [19], [13]. The extra equipment will, however, necessarily increase the total investment and capital cost. Therefore, it would be preferable to enhance the DVR's current capabilities to also reduce the short-circuit current. By including a new branch, the series compensator might accomplish various functions [5], [11]. A thyristor-switched inductor branch in the proposed DVR also allows for power factor adjustment [5]. Additionally, a typical method involves connecting the bypass in parallel to the primary of the series transformer [11]. The apparatus comprises a mechanical bypass switch that enables bypassing of the static series compensator (SSC) and a bypass electronic switch composed of two parallel thyristors [4]. The fault current is not constrained to the desired value even though the SSC is protected during faults.

Superconducting magnetic energy storage (SMES) was suggested as a fault current-limiting dynamic voltage restorer (SFCL-DVR) in [21]. The SFCL-transient DVR's condition, however, was not fully characterized. The current-limiting module's thermal stability and maximum withstand voltage were also disregarded. The series transformer ratio's ideal parameter selection has not been considered [21]. In contrast, a high-power multilayer inverter generates less harmonic current and necessitates power switches with lower ratings [3]–[10]. The design and use of the multifunctional system depend greatly on the aforementioned characteristics.

To lower the transformer's ratio, a brand-new multilayer Diode Clamped dynamic voltage restorer (MD-DVR) is presented in this work. Similar cascade inverter performance advantages, such as lower power ratings and cheaper power devices, are offered by the MD-DVR. Additionally, it immediately restricts the short-circuit current during failures and provides the system with more effective protection.

II. The Principle and Control Strategy of SMES DVR

1 Principle

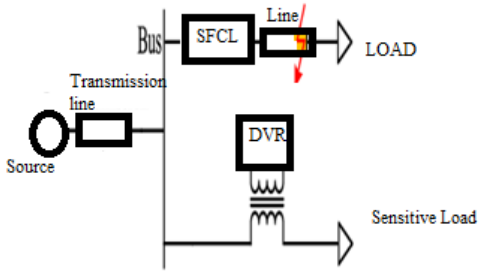


Fig.1. (a) block diagram for the proposed system

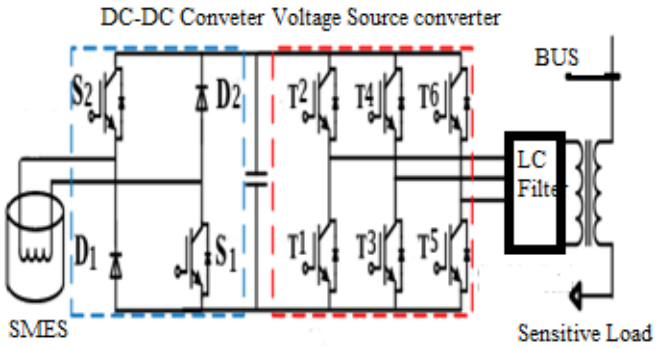


Fig.1. (b) SMES-based DVR.

Figure 1a shows the SMES-based DVR and SFCL circuit architecture. Figure 1 depicts the major components of the sensitive load side SMES-based DVR: a VSC, in-grid transformer, DC-link capacitor, and SMES device formed from a single SMES magnet and Chopper. (b). SFCL connects the feeds in series.SMES and SFCL reduce voltage sag for sensitive loads. If a 3-ϕ fault appears in a line without a sensitive load, the fault current and bus voltage will be limited. As soon as a voltage sag is noticed, the SMES-based DVR corrects the voltage of the sensitive load.

2. SMES-DVR Management Technique

Figure 2 depicts the control approach for the SMES-based DVR, which includes controlling the DC-DC converter and the VSC. The DC-DC converter uses the DC voltage control method to keep the DC voltage constant. The difference between the dc voltage reference and the actual value is passed to a hysteresis buffer to generate a PWM control signal to operate the two switches (S1, S2). The dc voltage can be regulated by manipulating the on-off state of two switches to achieve a repeat transition between charge mode (S1 ON, S2 ON) and discharge mode (S1 OFF, S2 OFF) for SMES. It is crucial to stress that the SMES cannot be guaranteed to operate normally if the magnet current is excessive.

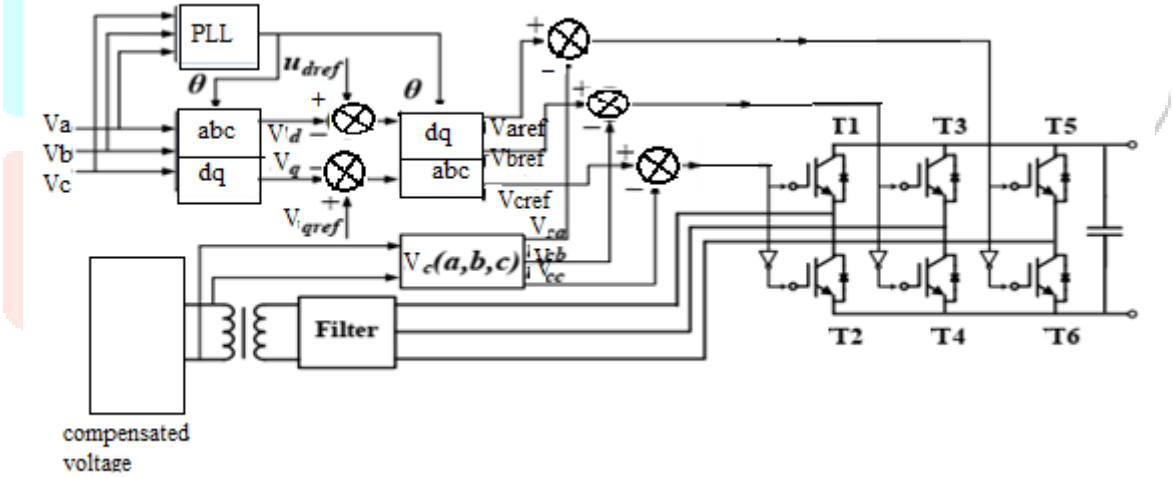


Figure. 2. The VSC presag compensation plan.

Additionally, as illustrated in Fig., a pre-sag compensation technique with dq transform is used to manage the VSC [11]. To accurately correct voltage quality disturbances caused by instantaneous reactive power theory and hysteretic voltage management method, The sensitive load voltage's real-time magnitude, and phase angle are individually locked and saved. The pre-sag strategy produces the least amount of transient voltage waveform distortion when compared to other approaches such as phase or optimized-energy compensation.

3 Equivalent Resistance Modelling of SFCL

The resistance feature of the SFCL has been studied in our earlier work [7], [15], which suggests that the SFCL will behave differently in terms of its physical state and resistance features depending on the current passing through it. Additionally, under various operating situations, the SFCL resistance value is separated into 5 operational sectors.

$$R_{sf} = \begin{cases} 0 & t<t_s \\ SE_c I_r^{n-1} / I_c^n & t_s<t<t_e \\ Rm & t_1<t<t_1 \\ R_m e^{-(t-t_e)/\tau_2} & te<t<t_2 \\ 0 & t>t_2 \end{cases} \quad (1)$$

III. Estimation of SMES and SFCL Parameters

Design of SMES Magnet

A high critical current is required when using the SMES magnet with a resistive SFCL device because of the necessity for the short-term, high-power energy exchange. [21] An inductance of 1.5 H and 800 A critical current are employed in this research [21]. The SMES magnet has a set of nine pancake assemblies at each end. The central assembly consists of ten parallel pancakes, each with fifty coil turns. It measures 270 millimeters across the top and 240 millimeters across the bottom. Four symmetrical assemblies on each side, with 5 serial pancakes from each coil end to the centerpiece, are used to generate a step-shaped cross-sectional shape. Two-inch, two-inch, and two-and-a-half-inch inner diameters are available. To meet the extended standards of the SMES, four step-shaped components are coupled parallel in series. The total tape length for this SMES magnet is around 20 kilometers. B. Estimation of SFCL's Resistance

Equivalent circuit diagrams for the distribution system shown in Figure 1(a) are illustrated in Figure 4. Faults in one line cause the switch K to be closed and bus voltage to be stated in terms of volts.

$$Vbus = \frac{Zi}{Z_t(Z_i+Z_s)+Z_iZ_s} V_s \quad (2)$$

Where,

$$Z_l = R_m + Z_i + \frac{Z_l+Z_f}{Z_lZ_f} \quad (3)$$

Total transmission line impedance (Zt) is equal to the sum of the load impedance and the equivalent line impedance (Zi), and sensitive load impedance (Zs) is equal to the impedance of the sensitive load.

The bus voltage (Vbus) is dependent on the SFCL resistance Rm, according to equation (2). Accordingly, it is possible to estimate the SFCL resistance to meet the required bus voltage requirement (2).

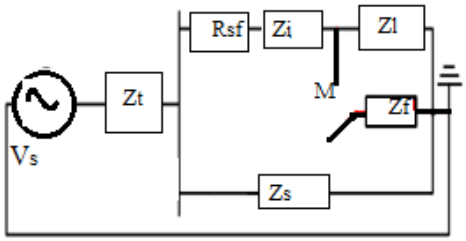


Fig. 4. Block diagram of distribution system equivalent circuit.

II. 5-LEVEL DIODE CLAMPED INVERTER

Basic bridge inverters have been modified to produce multi-level devices. The most common configuration is to link them in series to create level stacks.

The multilevel inverter's topological structure must address the following issues:

1. To the extent practical, it should contain fewer switching devices.

2. It should be able to withstand very high input voltages, such as those used in high-voltage direct current (HVDC) transmission. Due to the multi-level strategy, each switching device should have a reduced switching frequency.

1. Types of Multilevel Inverters

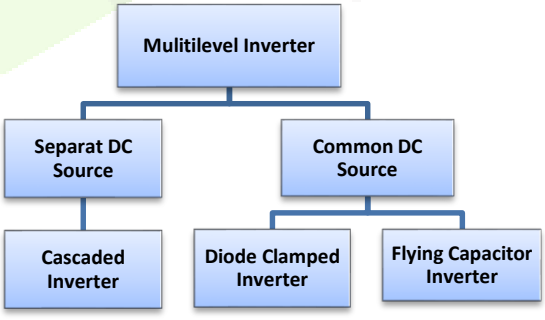


Figure 5 Multilevel Inverter types

Diode Clamped Multi-Level Inverter

Recent years have seen an increase in the number of industrial uses calling for greater power equipment. Megawatt power levels are required in several medium voltage motor drives and utility applications. Only one power semiconductor switch may be directly connected to a medium voltage grid without causing issues. As a consequence, in circumstances requiring high power and medium voltage, a multilayer power converter structure has been proposed. In addition to achieving large power ratings, a multilayer converter also makes it possible to utilize renewable energy sources. It is simple to connect high-power renewable energy sources like photovoltaics, wind turbines, and fuel cells to converter systems with many levels of output regulation. NABE-EL has brought the idea of multi-level converters to the industry. Low distortion and lower dv/dt, low input current distortion, reduced common-mode (cm) voltage, and lower switching frequency are some of the advantages of using MOSFETs in the 1970s and early 1980s. There are several benefits to using multi-level inverters. The diode clamped multilevel inverter also went by the name of the "neutral point clamped" (NPC) inverter. To effectively double device voltage levels without requiring precise voltage matching, a three-level NPC inverter was used for the first time.

Advantages

The harmonic content will be so low as to obviate the need for filters if there are enough levels. A great degree of efficiency is achieved by using a single fundamental frequency to switch all devices. Controlling the flow of reactive power is possible. A back-to-back intertie system has a simple control mechanism.

DCMI may be used as a multiplexer to link an output to one of the available nodes. However, despite their lower current, primary diodes are authorized to operate at the same voltage as the main power devices. DCMI capacitors are only required to filter out low-order components as they naturally cancel each other out. Only a capacitor's voltage is impeded in each power supply. Clamping diodes are used to protect electronic equipment from the damaging effects of a reverse current.

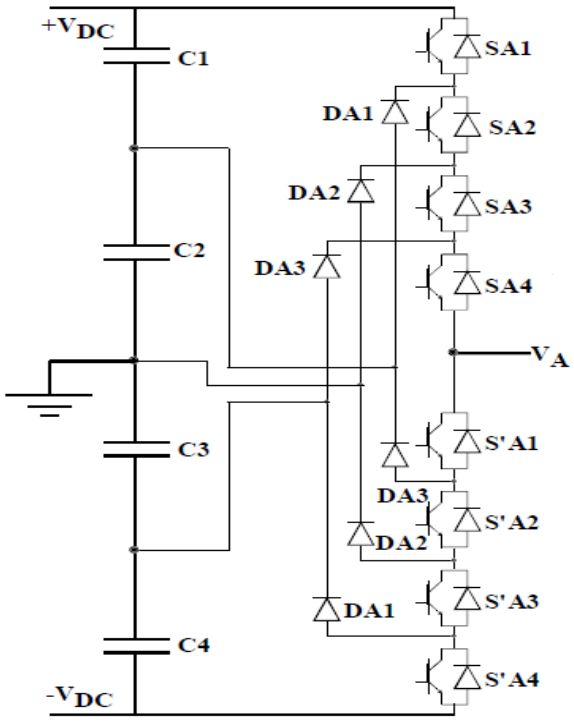


Figure 6 Schematic diagram of Diode Clamped Multi-Level Inverter

Table 1 Switching Sequence For 5 Level

output	s1	s2	s3	s4	s1'	s2'	s3'	s4'
$3V_{dc}/4$	0	1	1	1	1	0	0	0
0	0	0	0	0	1	1	1	1
$V_{dc}/4$	0	0	0	1	1	1	1	0
$V_{dc}/2$	0	0	1	1	1	1	0	0
0	0	0	0	0	1	1	1	1

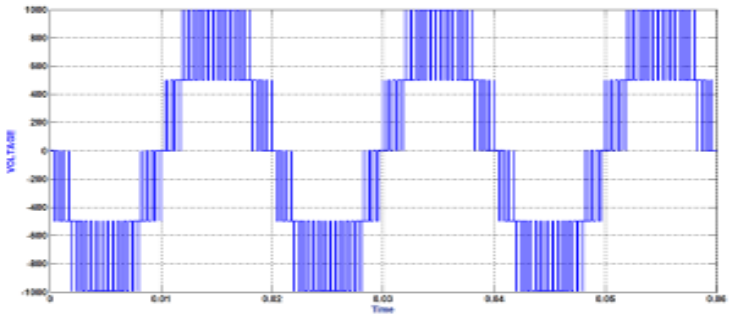


Figure 7 Output waveform of Diode Clamped Five level Inverter

III. SIMULATION RESULTS:

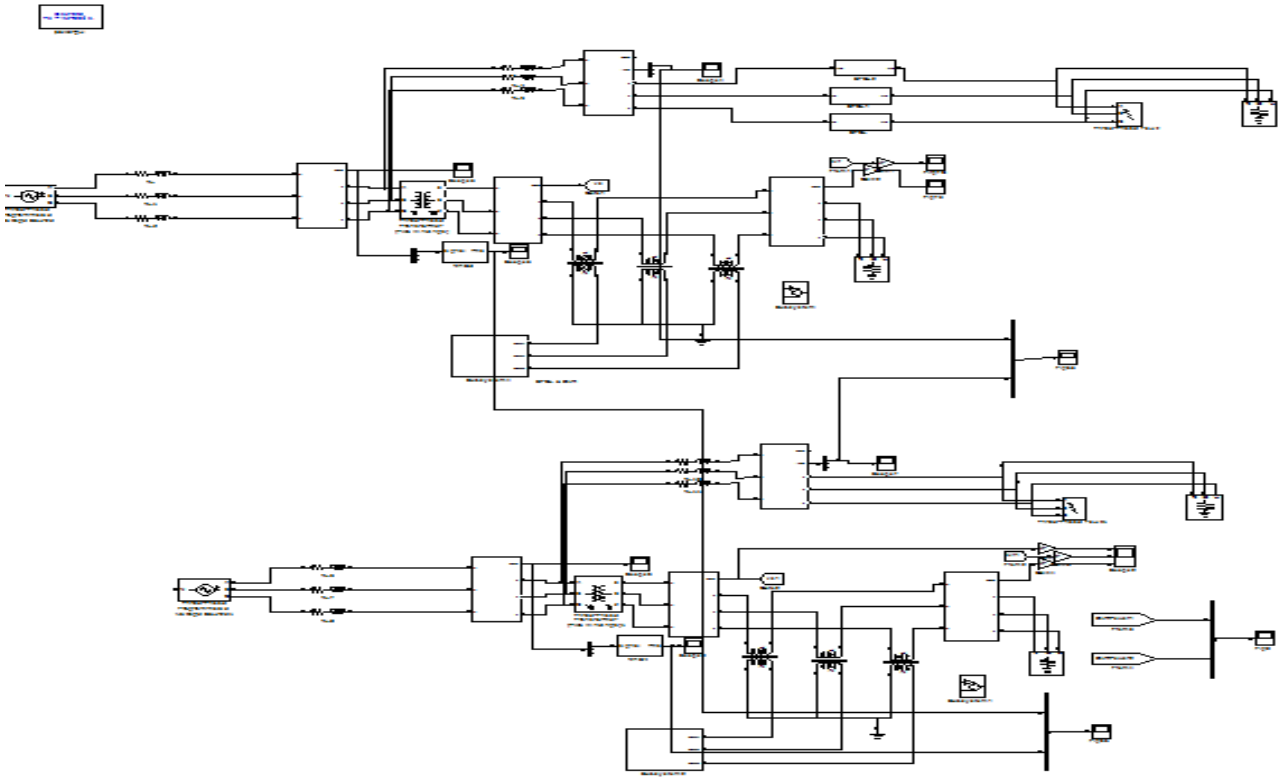
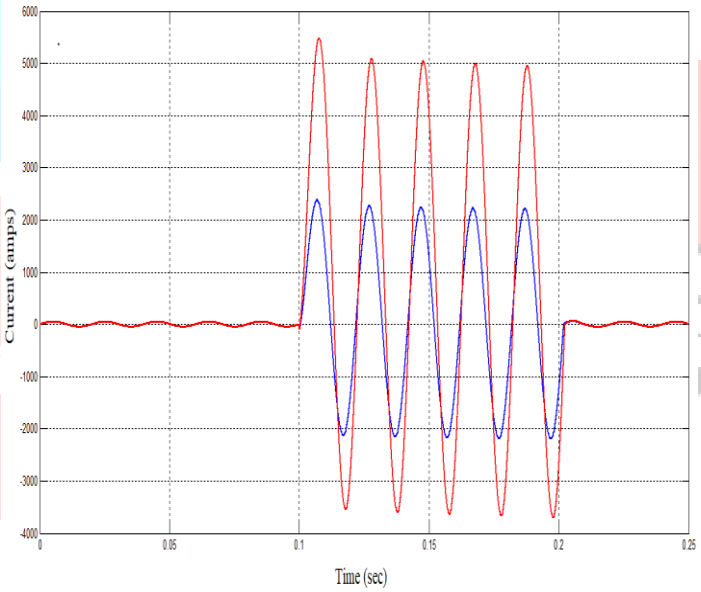
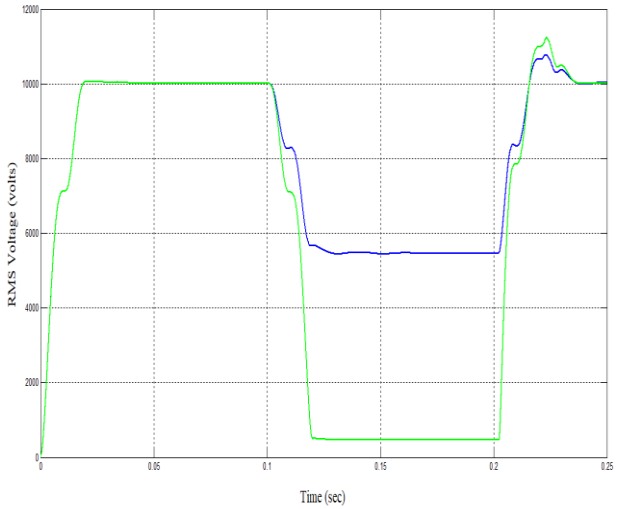


Figure 8 Simulink Diagram of Proposed System



8. (a) distribution line 1 fault current with a single DVR and the suggested SFCL&DVR.



8. (b) The suggested SFCL&DVR and the common bus RMS voltage with a single DVR.

The distribution line 1 fault current is shown in Fig. 8 along with two voltage compensation techniques. The first peak value of the fault current is reduced and is lower with the suggested cooperative strategy integrating SFCL and DVR (SFCL&DVR) than it is with the solo DVR scheme.

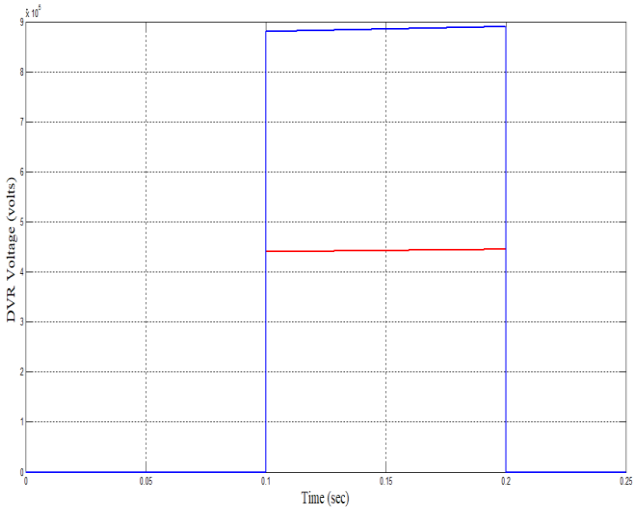


Fig.9. The suggested SFCL&DVR and a single DVR's output compensated for the power of the DVR.

Figure 9 displays the output corrected power of the DVR using two compensation strategies. The output compensated power of the DVR is decreased by the suggested SFCL&DVR method to 0.54 MW, which is 1.63 times less than that of the single DVR design (0.88 MW). This is a result of the additional SFCL's ability to reduce common bus voltage sag depth through its voltage-enhancement effect, hence reducing the adjusted power demand for DVR and capital costs.

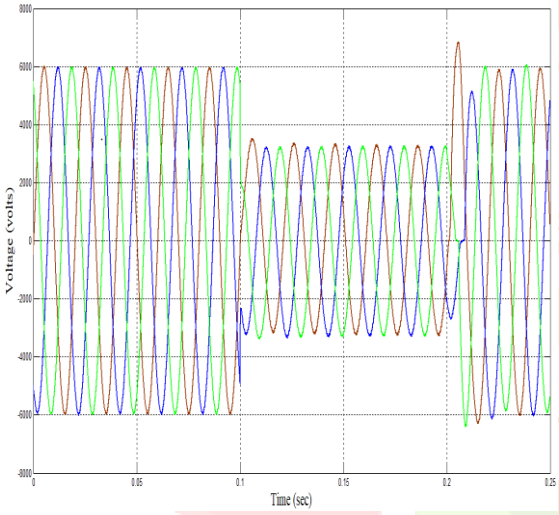


Fig.10. (a) The sensitive load voltage without compensation.

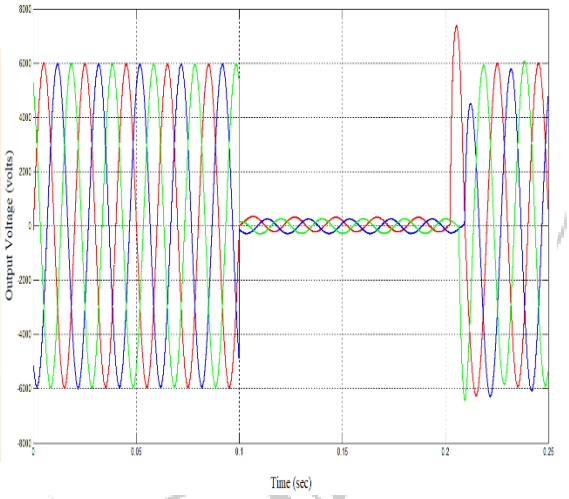


Fig.10. (b). The DVR output voltage with a single DVR.

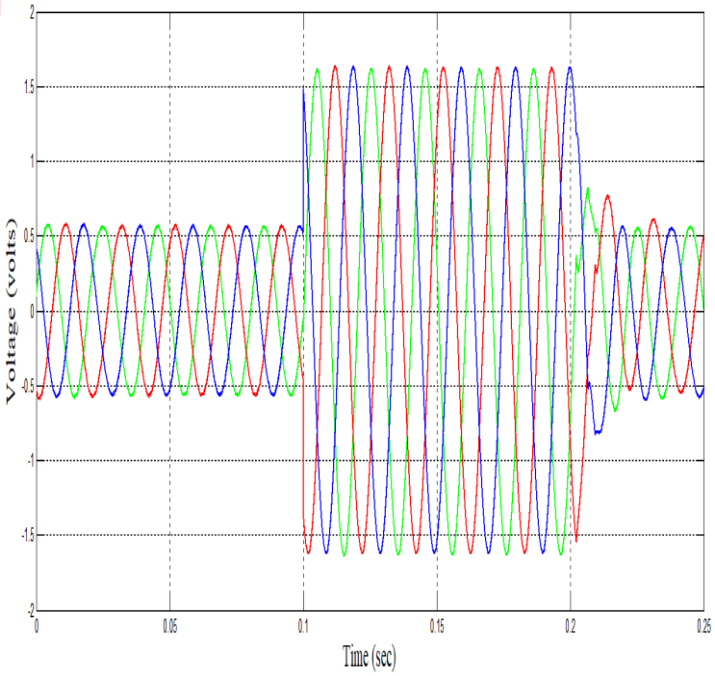


Fig.10. (c). The DVR output voltage with proposed SFCL&DVR.

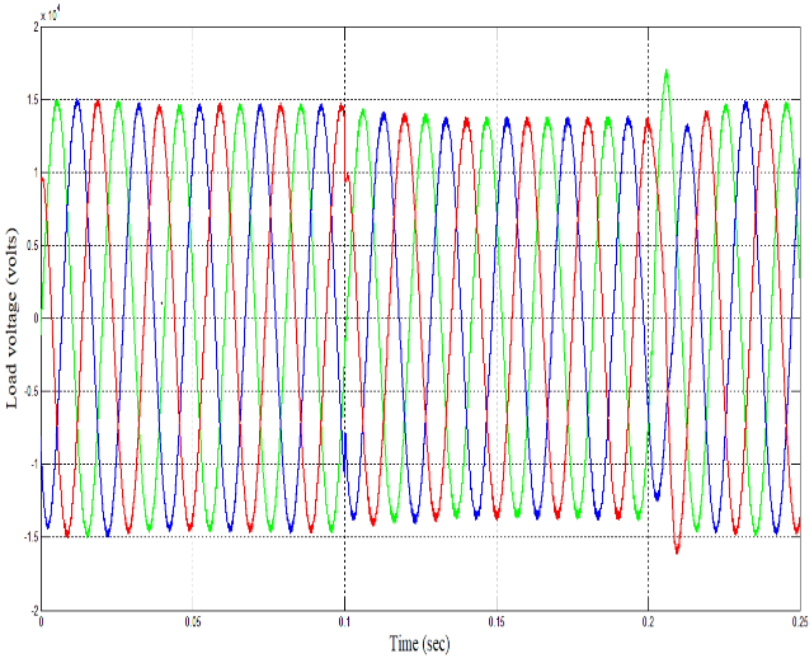


Fig.10.(d). The sensitive load voltage with compensation.

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Fig. displays the terminal voltage of the delicate load and the DVR output voltage with various voltage compensation strategies. 10. Comparing Fig. combined with Fig. In Figure 10(d), it is clear that both the single DVR and the suggested SFCL&DVR scheme are capable of fully increasing the sensitive load voltage to pre-fault value in under 8 milliseconds, essentially removing the negative effects of voltage sag on sensitive loads.

Additionally, the proposed SFCL&DVR strategy will boost the DVR output voltage compared to the single DVR scheme due to the additional voltage enhancement of the common bus via SFCL.

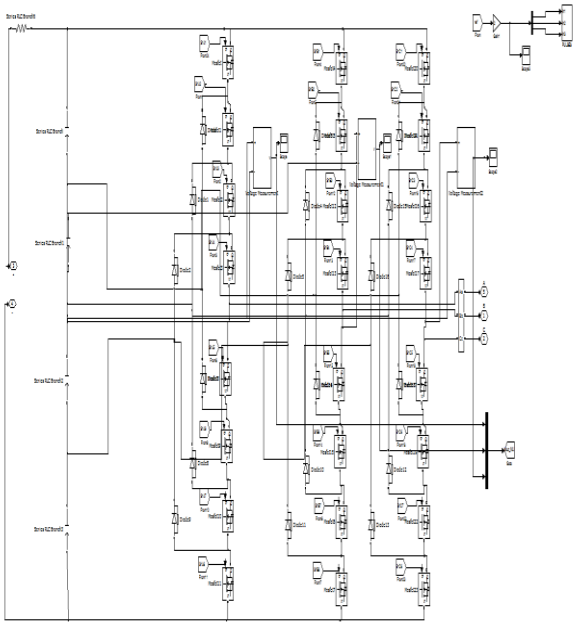

Figure 12 Simulink Diagram of Proposed Five Level Diode Clamped Multi-level Inverter System

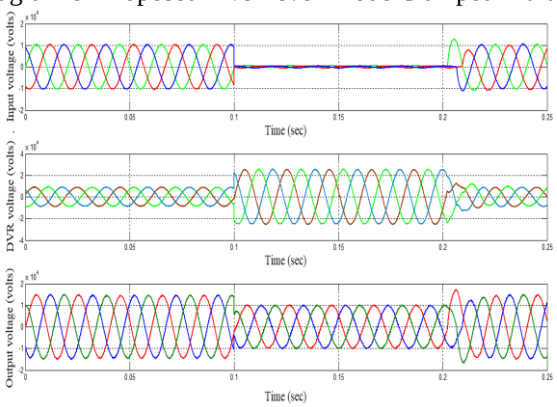

Fig.12. Simulation waveforms of Proposed Five Level Diode Clamped Multi-level Inverter System (a) Input Voltage (b) DVR Voltage (c) Output Voltage

IV. CONCLUSION

SMES-based DVR system coupled with SFCL has been suggested and tested to compensate for voltage sags. This paper presents and discusses in depth the conceptual design as well as the compensation principle, control technique, parameter assessment, simulation results, and performance evaluationSMES-based DVR system with pre-sag compensation may be able to retain the sensitive load voltage at its pre-fault value as long as the common bus fails. The additional SFCL's high resistance does more than only aid in the reduction of fault current. A further benefit of this approach is that it reduces DVR's total capital expenditures by reducing DVR's voltage-enhancement impact on a single common bus to a minimum. An MW-class SMES-based DVR system with SFCL may improve transient voltage quality in a modern distribution power system.

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