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OPTIMIZATION OF HIGH SPEED SIGNALS ON CIRCUIT BOARDS

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Abstract: Most of the connection paths between the sender and the receiver are formed by Transmission lines and via transitions. The impedance of the connection path should be as uniform as possible to minimize signal reflections and maximize system performance at high signal rates. The impedance of the transmission line is easy to control, but the impedance of the vias is much more difficult to control. In this project, we are trying to optimize the signal by using different optimization techniques. There are different parameters with effect the signals. By using the equation $Z=\sqrt{L/C}$, we are trying to maintain the signal impedance uniformly by varying capacitive and inductive effects throughout the board.

Index Terms – Time Domain Analysis for high speed signals

I. INTRODUCTION

1.1 Signal Integrity

The capacity of a signal to propagate without distortion is referred to as signal integrity (SI). The quality of the signal transmitted over the transmission line is called signal integrity. The signal is sent from the driver to the receiver. This problem is less of a problem at low frequencies, but it becomes more serious if the board is operating at higher speeds and frequencies (> 50MHz). Both the digital and analogue parts of the signal must be considered in the high-frequency realm. All signals within a PCB propagate without distortion, its devices and interconnections are not susceptible to extraneous electrical noise and Electromagnetic Interference (EMI) from other electrical products in its vicinity as per or better than regulatory standards, and it does not generate, introduce, or radiate EMI in other electrical circuits/cables/products either connected to it or in its vicinity as per or better than regulatory standards.

1.2 Optimization techniques in signal integrity

As the signal travels from the driver to the receiver, it changes. Everything originally sent will be received with varying degrees of distortion. Impedance mismatch, reflections, ringing, crosstalk, jitter, and ground bounce all contribute to signal distortion. The fundamental goal of a designer should be to minimize such influences so that the original signal can reach its destination with little distortion. Signal quality must also be maintained and unwanted effects in electrical circuits must be controlled. Via, Pad, Transmission lines, Shapes, Components, and Stack up are some of the approaches used to maximize or sustain the quality of a signal. There is a discussion of through optimization and stackup optimization.

1.3 Via optimization

A PCB via hole is made up of two pads in corresponding places on different layers of the board that are connected electrically through a hole through the board. Electroplating makes the hole conductive. When vias are used in a PCB design, the trace's distance which is going to be routed to accomplish its connection, is reduced. The most important thing is to understand the meaning of the various terms. Types of via and applications should be used effectively for both signal integrity and manufacturing. The Different via Types and their application vias are metal-plated holes that connect to the metal circuits of the circuit board and conduct electrical signals between the layers of the circuit board.

1.4 Stackup optimization

The stackup optimization is one of the important optimization techniques in signal integrity. This technique is used to increase the signal strength by modifying the stackup. Board thickness, kind of cores, prepreg utilized, thickness tolerance, and impedance requirements are all important factors to consider when designing a stack up. The Board's bow and twist are reduced thanks to the symmetric stack design. The plane and signal layers must be symmetrical in terms of dielectric and copper thickness, distribution, and position. For impedance-controlled circuit boards, dielectric thickness is critical.

II. EXISTING SYSTEM

Unprecedented demand for high-bandwidth applications has improved the data rates of major high-speed differential connection protocols such as PCIe and Thunderbolt and USB. Transmission cables and via transitions make up most of the connection path between the transmitter and receiver. Consistent impedance must be maintained in the system to create minimal signal reflections and to provide maximum system performance at high signaling rates path of interconnection. This study uses time-domain impedance waveforms and channel simulations to improve the impedance profile of three types of differential vias: through-holes, blind vias, and embedded vias. To achieve the optimization, many factors such as via diameter, pad diameter, anti-pad diameter, via pitch (distance between centers) is modified. A strategy for maximizing SNR by optimizing differential vias has been provided. The ideal impedance profiles of three types of vias: through hole vias, blind vias, and buried vias are also shown using a full factorial technique. Most notably, it provides a simple approach for optimizing vias based on whether they are overly capacitive or overly inductive. The purpose of fast optimization is to get an impedance profile that is close to a complete factorial optimization of the profile. The main disadvantage of this system is that, vias are based on geometry and because of the double barrel effect (Pad + Barrel), losses are unpredictable and so not possible to optimize the signal only by considering the vias.

III. PROPOSED SYSTEM

The proposed work focuses on the signal's full path between ICs in the circuit board, whereas the existing only has the characteristic analysis of via. The initial analyzes for the signal will be made , from which the optimization technique can be adopted from different optimization techniques such as, Via, Pad, Transmission lines, Shapes, Components, and Stack up. Then the signal will be simulated using Anysis HFSS (3D) tool for the adopted optimization technique and plotted eye diagram. In this work, we adopted stackup optimization and via optimization (adding ground via).The five different cases have been proposed for the above optimization. The simulation for the five cases has been performed, captured the results and compared for the best case. Our proposed optimization technique will provide the maximum or constant impedance throughout the signal, avoiding reflections and noises. This results in improving the signal strength. The signal path is complemented by impedance jumps through vias. As per the proposed optimization, timing analysis (eye opening) with Gigabit / sec serial channels reduce rise and fall times to less than 50ps. It can eliminate transmission line failures, thereby avoiding eye closure problems at the receiver. The via tuning method described in this application note helps to minimize the effects of signal vias on the transmission line and improve channel performance. The main advantage of this system is that along with via, stack up is also considered for optimizing the signal in PCB. And hence it is possible to reduce impedance mismatch created by the vias by adjusting the stack up parameters. The eye diagram is the main factor that defines the signal for each case.

A data eye diagram is a high-speed digital waveform representation that can be used to instantly display and determine key parameters of the electrical quality of a signal. Some of the most important parameters such as the high speed data signal requirements can be measured with an eye diagram. High-speed signal sources or transmitters are described using eye diagrams (receiver testing usually requires a BER test). In the eye diagram, the eye height measures the vertical aperture. The eye amplitude measurement should correspond to the eye opening measurement. Eye noise causes the eyes to close in the actual eye diagram measurement. As a result, by measuring eye height, noise-induced eye closure is determined. The size of the eye closure also directly indicates the signal-to-noise ratio of the high-speed data signal. The horizontal openness of the eye diagram is measured by the width of the eye. The difference between the statistical averages of the eye intersections is used in the calculation. The average transition time of the data at the rise of the eye diagram is called the rise time. Gradients are usually measured at 20-80 percent or 10-90 percent. The average transition time of the data on the downhill slope of the eye diagram is called the fall time. Gradients are usually measured at 20-80 percent or 10-90 percent. The five optimization approaches used are described below.

3.1 Adding ground vias

One technique is to connect a large area of copper to individual layers via stitching, providing a strong vertical connection through the board structure, allowing for low impedance and short returns. Via stitches can also be used to connect copper joints that are separated from the mesh. Via Shield has a different purpose in RF systems. It helps prevent crosstalk and electromagnetic interference in the RF signal path. A via shield, also known as a via fence or picket fence, is formed by inserting one or more rows of vias along the signal path.

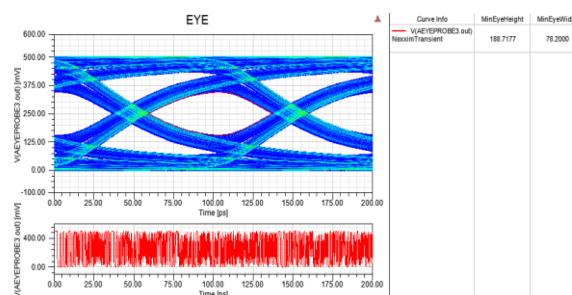

Fig 3.1 simulated for eye diagram– ground via

3.2 Reducing dielectric thickness

Microstrip structures have greater characteristic impedance than stripline structures with the same thickness of insulating material applied. As a result, high-frequency and high-speed digital signal transmission prefers microstrip construction. Furthermore, when the thickness of the insulating material increases, the characteristic increases. As a result, when it comes to high-frequency circuits with precise characteristic impedance, CCL insulating material thickness must adhere to a strict tolerance of no more than 10%. However, for multi-layer boards, insulating material thickness is also a manufacturing characteristic that must be tightly regulated. To summarize, even minor changes in trace width, trace thickness, dielectric constant, and insulating material thickness can cause a change in characteristic impedance.

Apart from those, it is linked to a number of other components. As a result, producers must be completely aware of the elements that cause variations in characteristic impedance and alter manufacturing settings to keep characteristic impedance within an acceptable range. In this situation, the dielectric material thickness is lowered during the stack up.

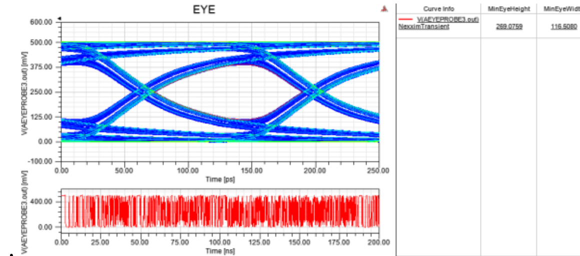

Fig 3.2 simulated for eye diagram– thickness reduced

3.3 Increasing dielectric thickness

A manufacturer is usually aware that high-frequency transmissions require components such as microwave impedance matching, and capacitance should be considered on each layer. Without impedance matching, board functioning is nearly non-existent. It normally ranges from 3" to 10". The designer or manufacturer may choose to employ either calibration method. Because of the dielectric's ubiquitous use, the range of its following board thickness might be quite wide. Capacitance decreases as dielectric height rises, resulting in better impedance.

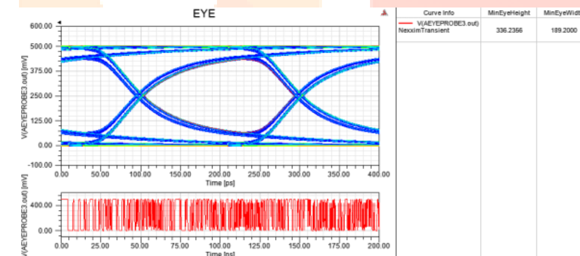

Fig 3.3 simulated for eye diagram– thickness increased

3.4 Increasing via-to-via distance

Although spacing the ground vias at 1/8th of a wavelength provides decent isolation, it has been discovered that for the best isolation, via spacing should be limited at 1/20th of a wavelength or less. The design difficulty here is more of a "waveguide beyond cutoff" type of problem, and it has been analyzed in the past that way. These types of analyses agree well with the 1/20th-of-a-wavelength rule of thumb and my experience developing PCBs with very high isolation.

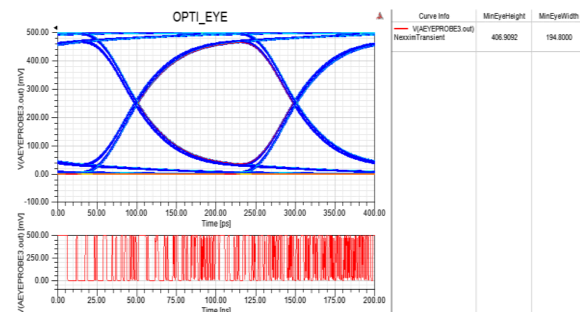

Fig 3.4 simulated for eye diagram– thickness between via increased

3.5 Increasing dielectric thickness

Almost any board with several components will simply not have enough area for return traces to be routed alongside all signal lines. The same effect can be achieved by inserting a ground plane on the bottom layer of a two-layer PCB; additionally, placing the ground plane below signal traces minimizes the loop area viewed by signals. You can also route ground returns straight from a component to the ground plane through a via by placing a ground plane underneath the required components and signal traces. The return signal will then return to the power supply return via the path of least resistance. This also makes it simple to include bypass/decoupling capacitors between important component power connections and the ground plane, preventing any high-frequency variations in the power connection (such as conducted EMI from a switched power source) from reaching the relevant components.

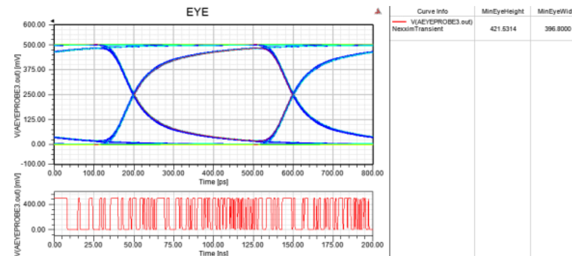

Fig 3.5 simulated for eye diagram– ground layer added

IV. RESULTS

4.1 Results of various optimization techniques

Table 4.1: Result comparison

Cases	Simulation Results	
	Min Eye height(mv)	Min Eye Width(ps)
Existing	355	190
Case1	188.7	78.2
Case2	269	116
Case3	336	189
Case4	406.8	194
Case5	421.5	396.8

From the Table 4.1, we could find that the case 5 which is the optimization technique of adding ground layer to the stack up is the best case as the defined specifications are achieved.

V. CONCLUSION

This paper analyzes the high-speed signal in the circuits from the aspect of signal integrity, and gives possible optimization techniques to improve the signal strength. A signal path between ICs is analyzed and simulated for all the provided optimization techniques. The tool used for 3D simulation is HFSS. We have performed the five different cases through simulation and captured the results. The different optimization techniques are Ground via added, stackup decreased, stackup increased, via to via distance increased, Add ground layer below first layer. Among the five cases, fifth case is considered as the best case as it achieved the increased minimum eye height and minimum eye width.

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