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SIMULATION OF 9 LEVEL MLI USING POD-SPWM

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Abstract: Multilevel inverter is usually utilized in high voltage and high-power applications because of their lower filtering requirement smaller dv/dt changes medium voltage. But, as the output voltage level increase, the number of using the semiconductor device is increased. The demerit of conventional MLIs is that it requires a greater number of components which in turn increase the complexity of gate pulse generation. Therefore, the cost of MLI will increase.

Conventional MLI topologies are classified into DCMLI (Diode Clamped Multilevel Inverter), Flying Capacitor,

Cascaded h-bridge MLI (CHBMLI).

In this paper we have used hybrid cascaded h-bridge MLI. It has more advantages over other topologies. It is proposed with a minimum number of switching devices like diodes, dc source etc. cost and space required is considerably reduced with increase in no of steps in output voltage.

This paper includes the design and simulation of hybrid

Cascaded h-bridge multi-level inverter using POD SPWM technique with R and RL load as shown in the paper

Keywords - Hybrid Cascaded H-Bridge Multilevel Inverter (Hybrid CHBMLI), Multilevel Inverter (MLI), Pulse Width Modulation (PWM), Harmonics, Total Harmonic Distortion (THD), Phase Opposition Disposition (POD-SPWM), FFT(Fast Fourier Transform), MATLAB.

I. INTRODUCTION

Inverter is a type of energy conversion device that converts Dc input power to Ac power as output. Multilevel inverters is modification of conventional two level inverters but the output in MLI's contain more than two level due to which many disadvantages of normal conventional inverters are reduced. Numerous staggered inverter arrangements are displayed accurate output voltage with reduced harmonics range and to decrease the network intricacy.[2] In any case, as the amount of voltage levels fabricate the need of trading devices Multilevel inverters are of three types i.e., Diode clamped multilevel inverter, Flying capacitor multilevel inverter, Cascaded H- bridge multilevel inverter. Because of simple switch arrangement and ease of control the H-bridge conventional inverters were used in many industrial applications for many years. [3-4]

The topology of Hybrid Cascaded H-Bridge Multilevel Inverter with two dc sources, two capacitors and seven switches. This topology is a combination of T-Type single phase inverter and H-Bridge MLI module with sub switches. This combination eliminates the need of extra dc sources and also reduces number of switches required. In these the output we get is not desirable as per users need and also has more harmonics contents which is also not acceptable, and gives rise to heating problems due to which not only the inverter but the other devices may also get harmed. Due to these drawbacks, the Pulse Width Modulated inverters and conventional H-bridge inverters have been replaced by new multilevel inverters. Now a days most of the industries around the globe uses multi-level inverter techniques to decrease the voltage stress developed on power devices, due to which heating issues is reduced and hence produces output voltages of good quality.[1] MLIs can accomplish practically unadulterated output pure sine voltages with low total sources as required by many industrial applications, such as ASDs, which are the most popular application of inverters.

Harmonic Distortion (THD) in average voltage source inputs. Multi-level inverter appreciates critical focal points over the conventional two-level inverters as far as less consonant issues, reduced THDs, highly effectiveness, upgraded voltage quality, and lower conversion stresses.[2] These multi-level inverters improve the output ac power quality by performing the power conversion in small voltage steps due to which harmonics are less generated. Hence harmonic content of output voltage waveform of these multilevel inverters is greatly reduced compared to the basic two-level output voltage waveform. Due to such advantages the use of multilevel inverters is increased considerably in different sectors like UPFC, Industrial Drives, Electric Vehicles, Renewable Energy Conversion, Distributed Generation, Active Filtering and many more. Also, multilevel inverters have lesser THD (Total Harmonic Distortion), voltage stress across the switches, heating issues, power losses and higher power rating as compared to two-level inverter.

The main objective of our topological of multilevel inverter is to reduce the number of switching devices, reduce THD, and also reduce overall losses as compare to conventional MLI topologies. Hence here in this paper we are willing to design a 9 level MLI with seven switches with hybrid cascaded H-Bridge topology. Today efficient power conversion is more important than earlier days due to the alternative energy sources like fuel cells, solar energy, wind energy and ocean energy that require power output to assume different loads. Further the area of electrical drives is still demanding for new topologies in order to find more efficient and cheaper ways of converting the form of energy from electrical to mechanical or vice versa.[1].

II. MULTI-LEVEL INVERTER

The main objective of static power converters is to produce an ac output waveform from a dc power supply. These are the types of waveforms required in adjustable speed drives (ASDs), uninterruptible power supplies (UPSs), static var compensators, active filters, flexible ac transmission systems (FACTSs), and voltage compensators, which are only a few applications. For sinusoidal ac outputs, the magnitude, frequency, and phase should be controllable. According to the type of ac output waveform, these topologies can be considered as voltage-source inverters (VSIs), where the independently controlled ac output is a voltage waveform. These structures are the most widely used because they naturally behave as voltage. The problems with conventional multilevel inverters can be summarized as follows.

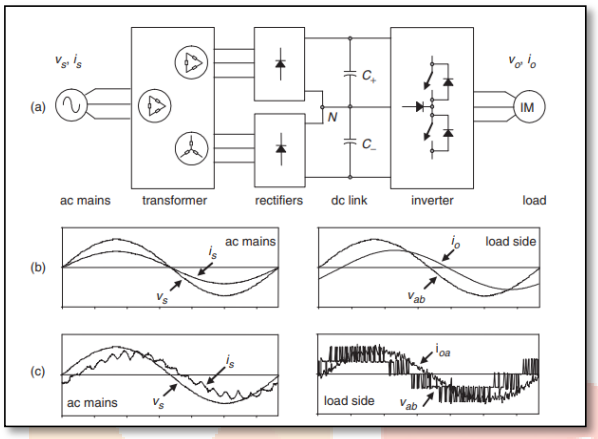

Fig 1

A three-level adjustable speed drive scheme and associated waveforms: (a) the electrical power conversion topology; (b) the ideal input (ac mains) and output (load) waveforms; and (c) the actual input (ac mains) and output (load) waveforms

Advantages of Multilevel Inverter:

The multilevel converter has several advantages, that is:

1. Common Mode Voltage:

The multilevel inverters produce common-mode voltage, reducing the stress of the motor and don't damage the motor.

2. Input Current:

Multilevel inverters can draw input current with low distortion

3. Switching Frequency:

The multilevel inverter can operate at both fundamental switching frequencies that are higher switching frequency and lower switching frequency. It should be noted that the lower switching frequency means lower switching loss and higher efficiency is achieved.

4. Reduced harmonic distortion:

Selective harmonic elimination technique along with the multi-level topology results the total harmonic distortion becomes low in the output waveform without using any filter circuit.

Types of Multilevel Inverter:

Multilevel inverters are three types.

- Diode clamped multilevel inverter
- Flying capacitors multilevel inverter
- Cascaded H- bridge multilevel inverter

a) Conventional topologies of Multilevel Inverters use a greater number of power switches. Its output voltage waveform may contain more harmonics.
b) It has been seen that with increase in number of output levels, the numbers of clamping diodes in Diode Clamped inverter and the storing capacitors in Flying-Capacitor's inverter increases.
c) The inverter control can be very complicated in Flying-Capacitor's inverter.
d) Cascaded inverter needs separate dc sources for real power conversion.

Table no 1. Comparison of Components Requirement per leg of 9-level MLI

Type of Components	Type of Converter (MLI)			
	Diode Clamped	Flying Capacitor	Cascaded H-Bridge	Hybrid CHBMLI
Main Switches	16	16	16	7
Main Diodes	16	16	16	10
Clamping Diodes	56	0	0	0
DC Bus Capacitors	8	8	0	2
Balancing capacitor	0	28	0	0
Isolated DC Sources	1	1	4	2
Total	97	69	36	21

From the analysis of requirement of components for Hybrid CHBMLI, it is now become possible to compare it with the requirement of components for conventional MLI. The comparison of components required for a 9-level MLI is given in the Table no 1. It is clear that our proposed topology requires less components than the conventional MLI.

III. PROPOSED METHOD

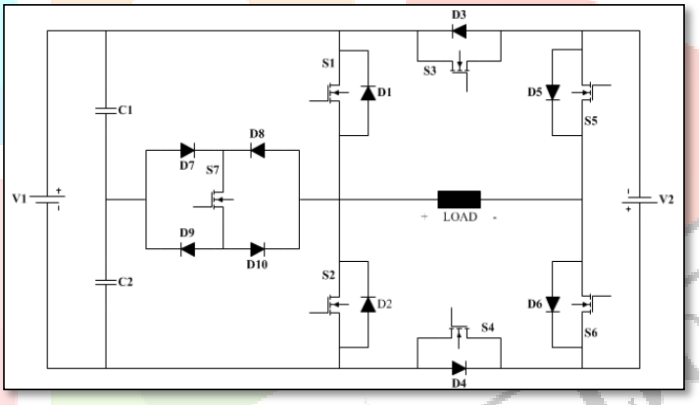

Fig 2. Circuit diagram

Above Diagram is the Circuit diagram of our 9-level inverter model with 7 switches as shown in fig 2.
The working principle of Hybrid CHBMLI can be explained simply with the help of the switching table. If the switch is in state "1" then it is considered that switch is conducting. Similarly, if the switch is in state "0" then it is considered that switch is not conducting. The Table below shows the switch states according to which the desired output voltage waveform is generated.

Topology of Hybrid CHBMLI
This topology contains two dc source, two capacitors, seven switches as shown in fig 2. This topology is a combination of T-Type single phase inverter and H-Bridge module with sub switches. This combination reduces no of switches and dc source.

Table no 2. Switching Table

Mode	Output Voltage	Switch State						
		S_1	S_2	S_3	S_4	S_5	S_6	S_7
0	0V	0	0	0	0	0	0	0
1	+24V	0	0	0	1	0	0	1
2	+48V	0	0	0	1	1	0	0
3	+72V	0	0	0	1	1	0	1
4	+96V	1	0	0	1	1	0	0
5	-24V	0	0	1	0	0	0	1
6	-48V	0	0	1	0	0	1	0
7	-72V	0	0	1	0	0	1	1
8	-96V	0	1	1	0	0	1	0

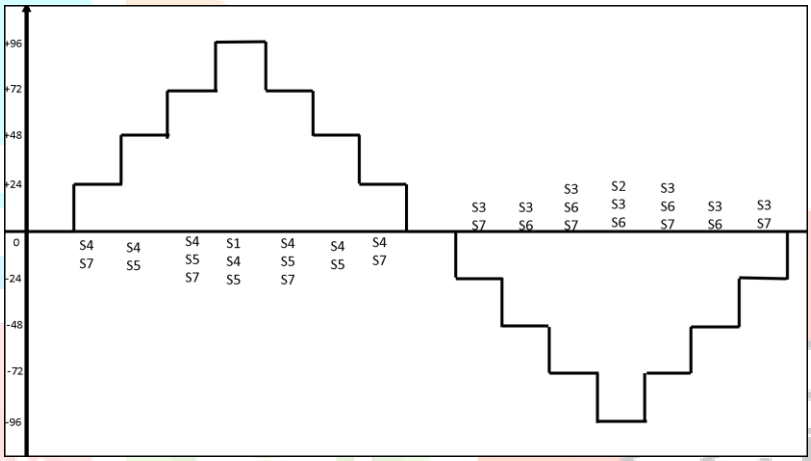

Fig 3 Expected Waveform

This is expected waveform we will getting after the doing complete simulation. X- axis is time and Y-axis is output voltage The inverter is symmetrical with two DC sources of magnitude 48V each. So, the peak output voltage will be of 96V

Objectives of Hybrid CHBMLI

- To have high quality output voltage with less THD.
- It must contain less number of power semiconductor switches and other components.
- It should have quite simple principle of operation.
- It should have implementable switching strategy.
- It should have low dv/dt stress on power semiconductor devices.

IV. MODES OF OPERATION

The operation of Hybrid CHBMLI is divided in to 8 different modes depending upon the output of the inverter. These 8 different operations are taken according to the 8 switching states in table no. 1 Different operational modes are shown further

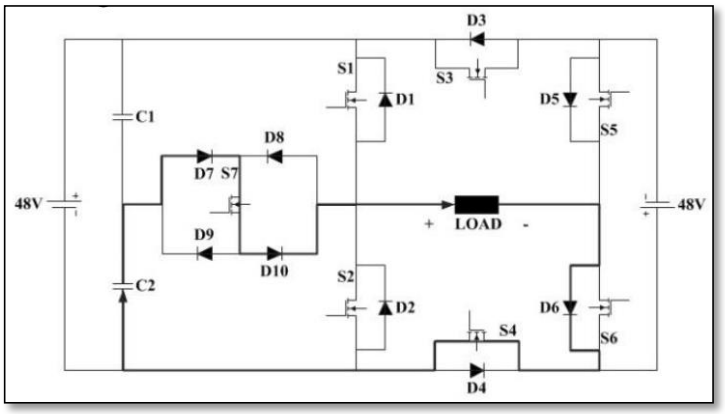

Fig 4. (Mode 1: Vo = +24V)

Mode 1: In this mode of operation capacitor C2 will act as voltage source. As seen in the Switching table switches S4 and S7 will be turned ON through appropriate gate pulses. Load current Io will flow through the path C2-D7-S7-D10- Load-D6-S4- C2. Operation will be similar for other modes according to the switch states shown in switching table.

Similarly, all other modes work on the same basis but, the only changes that takes place are different diodes, switches and capacitors work for different operation simultaneously to confirm the proper working of the circuit.

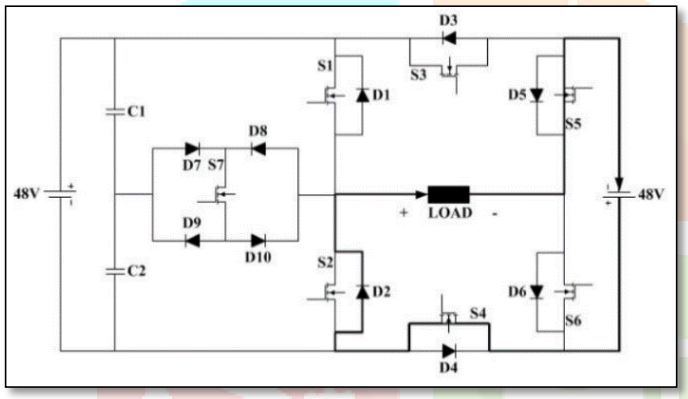

Fig 5. (Mode 2: Vo = +48V)

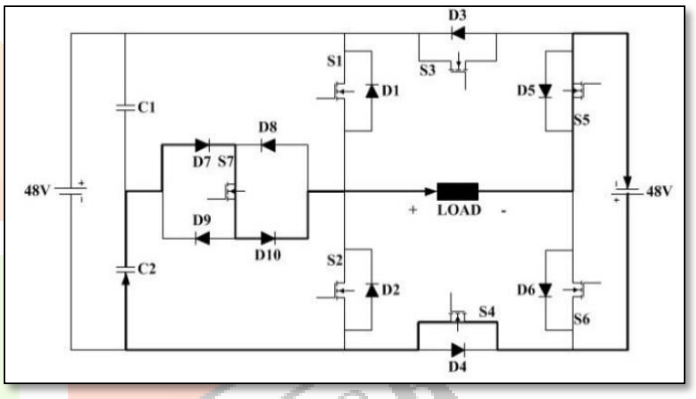

Fig 6. (Mode 3: Vo = +72V

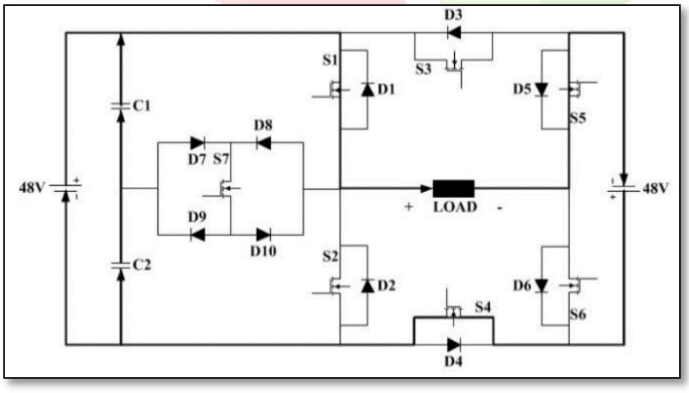

Fig 7. (Mode 4: Vo = +96V)

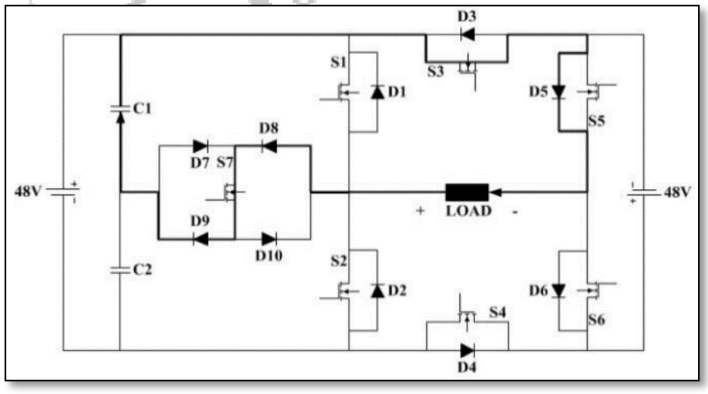

Fig 8. (Mode 5: Vo = -24V)

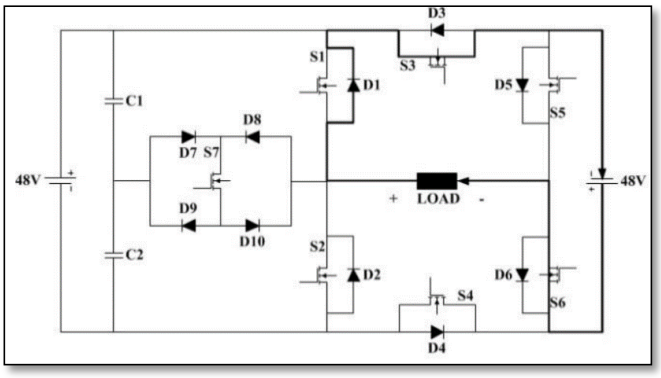

Fig 9. (Mode 6: Vo = -48V)

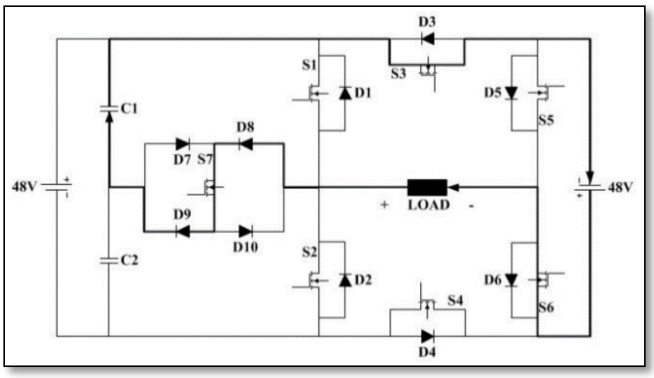

Fig 10. (Mode 7: Vo = -72V)

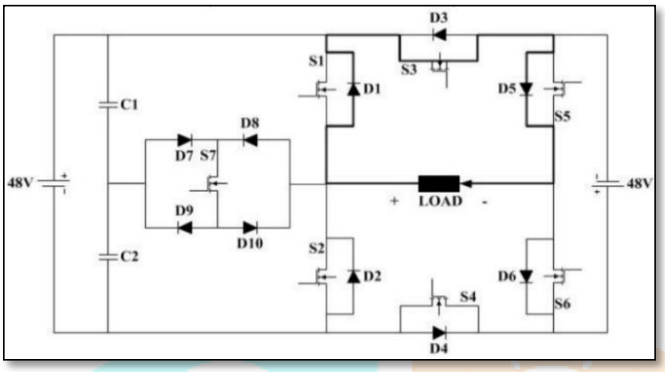

Fig 11. (Mode 8: Vo = -96V)

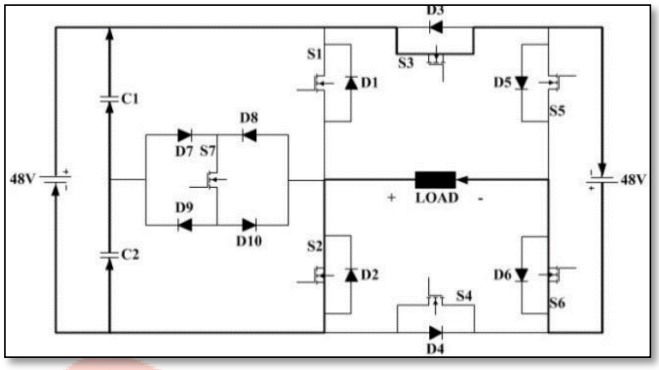

Fig 12. (Mode 0: Vo = 0V (S3 ON))

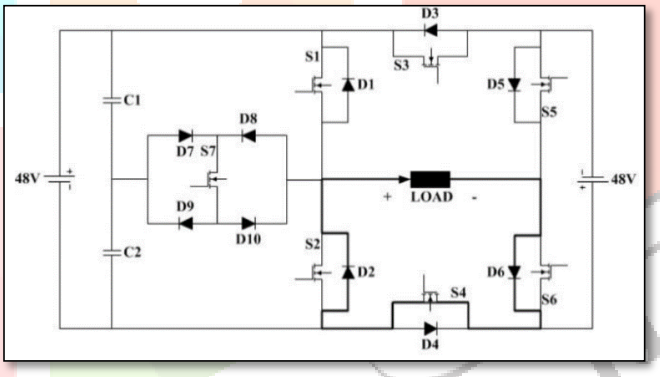

Fig 13. (Mode 0: Vo = 0V (S4 ON))

V. Simulink Results

Simulink models for gate pulse generation and power circuits are shown. Sine wave of fundamental frequency (50Hz) is compared with level shifted triangular carrier waves of 1 KHz frequency. The gate pulses are then applied to the respective switches of the power circuit.

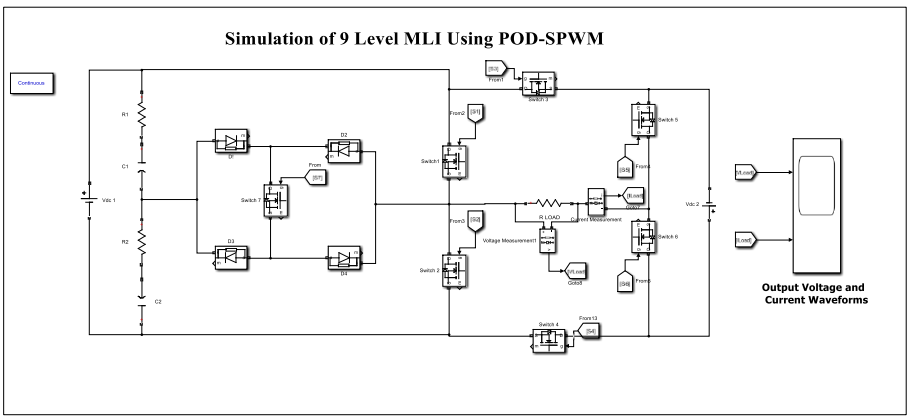

Fig 14. Power Circuit For R Load

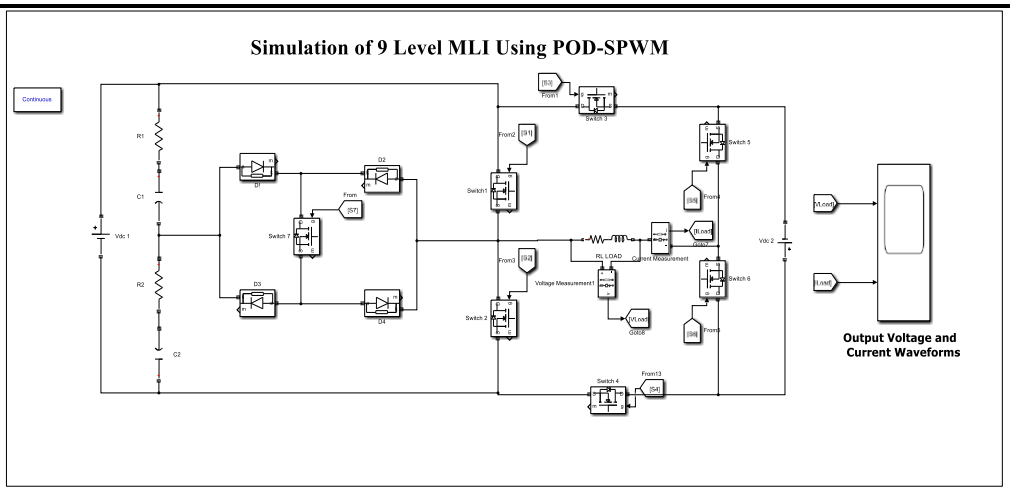

Fig 15. Power Circuit For RL Load

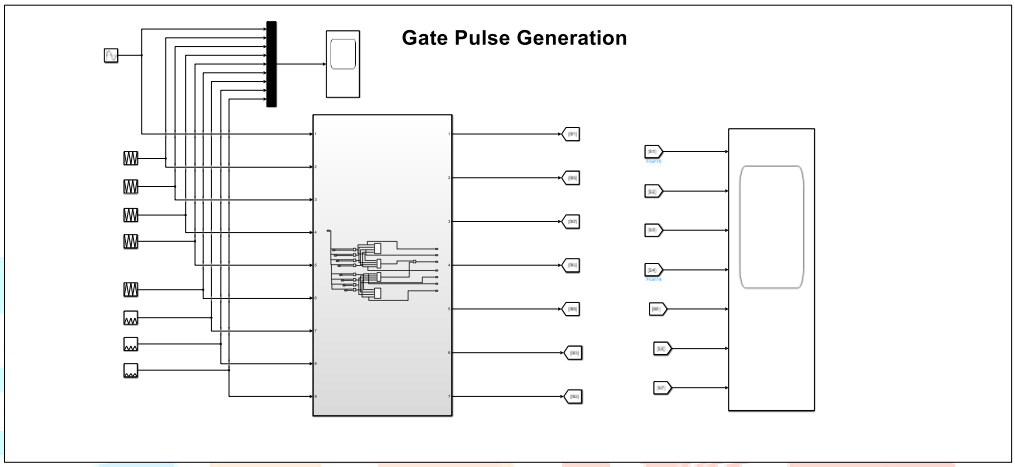

Fig 16. Gate Pulse Generation

The output waveform is optimized and has THD of 9.51% which is very less than in conventional MLIs. Simulation Parameters Simulation parameters given in Table no 2 are derived by referring the research papers [4, 9] and as per available rating of components which are required to make the hardware prototype of the Hybrid CHBMLI.

Table no 3. Simulation Parameters

Voltage Source - I (V1)	48 V
Voltage Source - II (V2)	48 V
Capacitor (C1 and C2)	4700 µF
Load Resistance	96 Ω
Modulation Frequency	50z

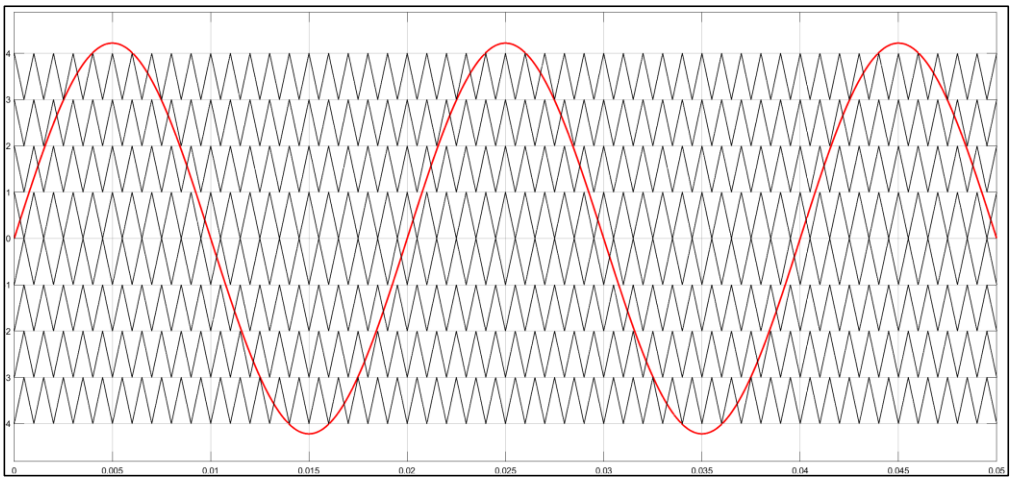

Fig 17. Comparison of Multiple Carrier Waves with Sine

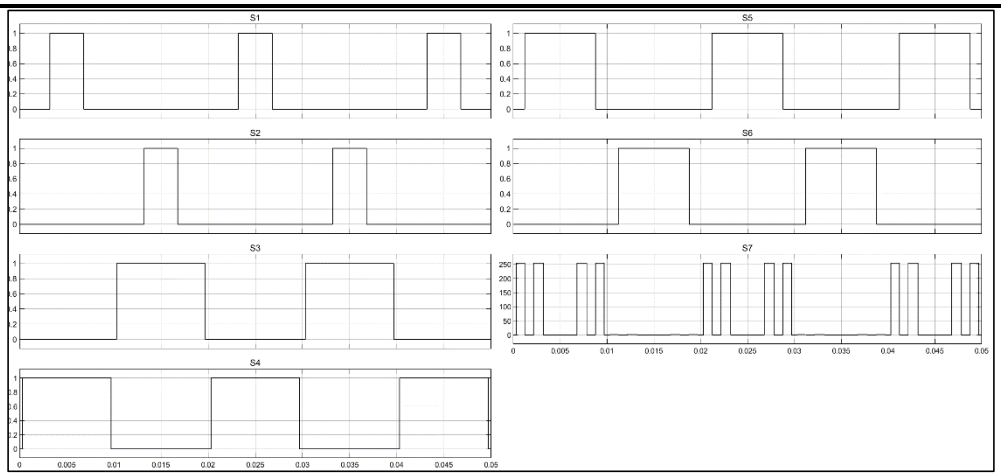

Fig 18. Gate Pulses

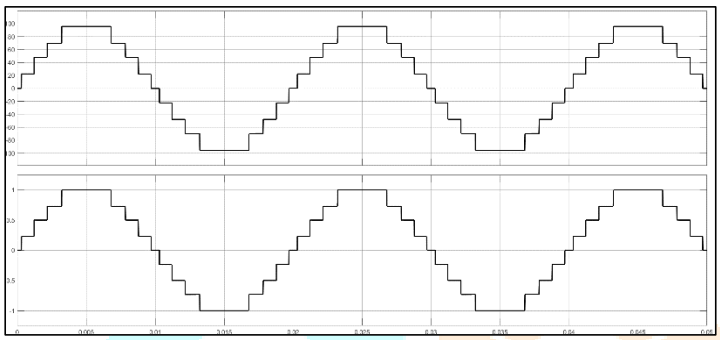

Fig 19. Output Voltage and Current Waveforms For R Load

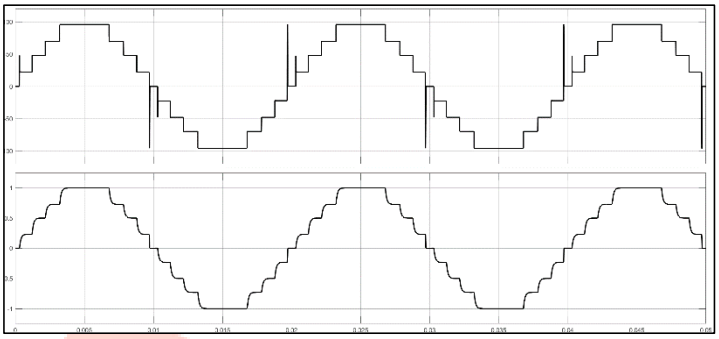

Fig 20. Output Voltage and Current Waveforms For RL Load

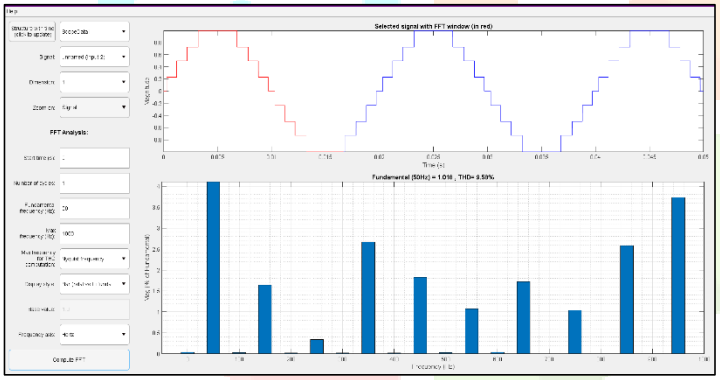

Fig 21. FFT Analysis for R Load

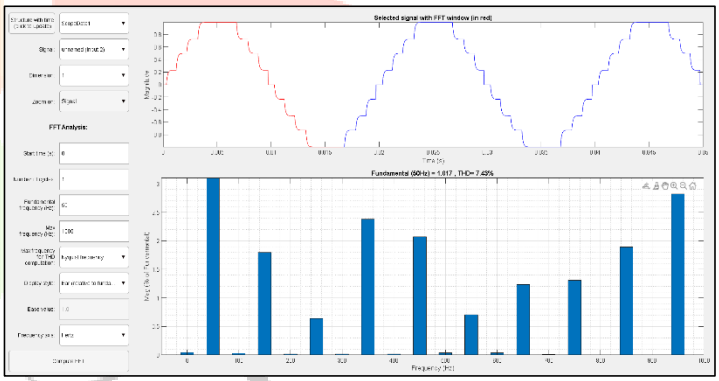

Fig 22. FFT Analysis for RL Load

VI. Conclusion

From the work done so far it can be concluded that, the proposed 9-level Hybrid CHBMLI requires a total of 21 components which is quite less than that of conventional MLIs. The harmonic content in the output of 9-level Hybrid CHBMLI is 9.58% for R load and 7.43% for RL load. which is almost 2% less than that of 9-level Cascaded H-Bridge MLI. The proposed modulation technique used here is POD SPWM technique which gives a proper 9 level output. There are total 7 switch used which operates on fundamental frequency due to which it ensures low switching losses.

References

[1] Ashish P. Patel Power Electronics Department, L. E. College, Morbi, Gujarat, India. “Design and Simulation of 9-Level Hybrid Cascaded H-Bridge Multilevel Inverter with Reduced Components”. 2018 IEEE. By performing various types of pulse width modulation techniques for Hybrid CHBMLI with the help of different modulation index the readings of THD were noted down. It shows that the POD PWM method is giving 11.03% THD with Modulation Index of 1 and hence best suited for the Hybrid CHBMLI.

[2] Shahina E P., Aravind K, Jarin T, “THD Reduction in Execution of a Nine Level Single Phase Inverter”. This paper proposed also presents a nine-level offset balanced inverter with decreased number components. The proposed technique is first actualized in MATLAB and Simulink software and then applied practically. A new multilevel inverter topology is studied which uses a smaller number of switches than the conventional inverter topology and hence the possibility of producing higher number of levels with same switches as in conventional topologies is made. The harmonic content is reduced by using a new Sine Property, which basically changes the step angle of each level so as to resemble to the sine waveform. The switching sequence multilevel inverter is designed to generate 7-Levels.

[3] Muhammad H. Rashid “Power Electronics Circiuts, Devices and Applications” 3rd Edition, Pearson Education.

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[6] Anjali, K. R., Padmasuresh, L., & Muthukumar, P. (2018). "Genetic algorithm based 15 level multilevel inverter with Selective Harmonic Elimination technique of PWM". Int. J. Eng. Tech no l, 7, 893-897. This paper proposes a nine-level balanced inverter with decreased number of switches and components. This proposed technique actualizes by utilizing MATLAB/Simulink. We know that MLI based topologies are expected to do a significant work for both high power and high or medium voltage applications. The proposed staggered inverter topology here accomplishes a high yield voltage waveform. The firm full scale complete consonant mutilation (THD) estimator is used to survey the possibility of the inverter yield voltage, which is the intensity of the improvement. Thus, the proposed framework here accomplishes the reasonableness of the nonappearance of channel with the lesser THD of diversion and exploratory outcomes.

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