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Design and Implementation of FIR Filter using Logic Optimization Techniques

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Abstract: In this fast growing technological world, there is a huge requirement for area and power efficient digital signal processing systems as they are portable, reliable and cost efficient. In many Digital Signal Processing systems, filtering is playing the key role to remove the noise in which Finite Impulse Response(FIR)filter is widely used. For an FIR filter, Adder and multiplier plays a prominent role. For effective area and improved speed applications, the FIR filter is designed by using Vedic multiplier with adder of different combinations of Logic gates and the fast Add-one and multiplexing CSLA adder with the modified full adder logic, and these are coded using Verilog HDL. The designed architectures of adders, multipliers and FIR filters using developed modules are simulated and synthesized in Xilinx VIVADO 2017.2 software.

Index Terms **- Finite Impulse Response, Vedic multiplier, Modified Logic Gates, FAM CSLA adder and Xilinx Vivado.**

I. INTRODUCTION

In this technology world, the DSP Processors has wide range of applications like communication systems and Mobile computing which requires highly Efficient hardware and Ultra-low power operations. Especially, Digital filter are widely used for computation, Signal Preconditioning, etc.,. digital Filters are mainly categorized into two types namely, Finite Impulse Response(FIR) and Infinite Impulse Response (IIR). However, the FIR filter are preferred over IIR filter for operations in DSP include Filtering, Convolution, and inner products due to its inherent stability, Linear Phase Response and the other advantage of an FIR filter is not having feedback[1].

An FIR filter is one of the basic block used in communication systems and the works on digital inputs. The filters are used to eliminate unnecessarily occurred signals.

An FIR filter can be expressed as:

$$y(n) = \sum_{k=0}^{n-1} h(n) * x(n-k)$$

y(n) = output of FIR filter
x(n) = input of FIR filter
h(n) = coefficients of FIR filter.

The Linear Time-Invariant (LTI) FIR filter can be expressed in z-domain as:

$$Y(z) = X(Z) * H(Z)$$

There are two forms of FIR filter they are: Direct form and transposed form. In this work, FIR filter is designed in transposed form because it is delay efficient and it doesn't need extra pipelining structure to get high through whereas direct form needs extra pipelining for high throughput and it is area efficient. The transposed FIR filter can be explained by multiplying an input with a given set of filter coefficients using multiplier and the result is stored in accumulator and this result and the previous step output are added using adder block. This process is done in every tap of a filter. The structure of this Transposed Direct Form FIR filter is as shown in Fig-1.

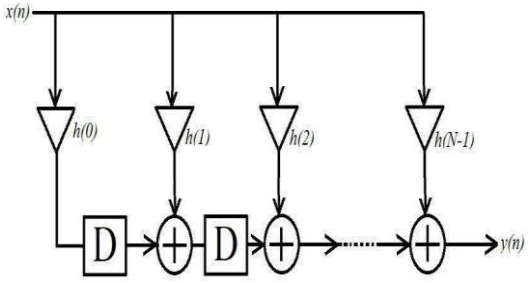

Fig-1:Transposed Direct Form FIR filter

Here, the filter architecture is simplifying in terms of Delay, Power consumption and complexity.
Section II deals with the components of FIR filter.
Section III deals with the simulation results for FIR Filter using logic optimization techniques.
Section IV deals with the performance results of FIR Filter.
Section V deals with the filter parameters performance comparison.

II. COMPONENTS FIR FILTER

In this section, the FIR filter has three basic blocks they are:

a. Delay element
b. Multiplier Block
c. Adder Block

The performance and the efficiency of the multiplier and adder has great impact on filter performance characteristics.

a. Delay Element:

A delay element is used to store delay coefficient of the filter. Here D flip-flop is used as delay element. Delay element is required since when the coefficients are given to the multiplier block a gap should be maintained so that there should not cause any traffic.

b. Multiplier Block:

A Vedic Multiplier is being used here to Multiply inputs and the filter coefficients[2][3]. A Vedic Multiplier is works on the principle of Urdhva Triyakbhyam (vertical and cross-wise) sutra, this sutra is used ancient multiplication. Generally, the Vedic Multiplier requires less number of steps to compute the value. So, this multiplier is faster and has less delay. By using this Multiplier, all multiplications are performed irrespective of its size.
The modified Vedic Multiplier is being used here, is designed using adders with the Modified Logic Gates. The modified Vedic Multiplier reduces the area and power consumption over existed Vedic Multiplier. The architecture for this Vedic Multiplier is shown in Fig-2.

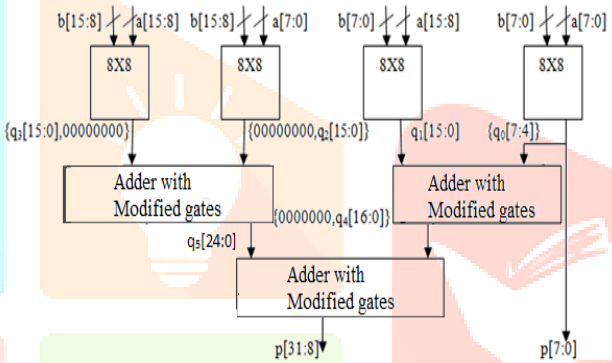

Fig-2:Architecture of Modified 16 – bit Vedic Multiplier

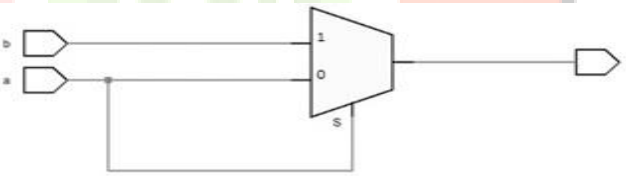

Fig-3: Modified AND gate

The Modified AND gate is designed by using a 2:1 multiplexer for which the inputs to the multiplexer are ‘a’ and ‘b’. Input ’a’ also acts as selection line for multiplexer and the obtained output is named as ‘y’is shown in Fig-3.

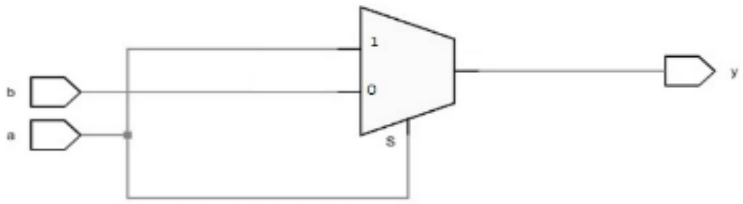

Fig-4: Modified OR gate

The Modified OR gate is designed by using a 2:1 multiplexer for which the inputs to the multiplexer are ‘a’ and ‘b’. Input ’a’ also acts as selection line for multiplexer and the obtained output is named as ‘y’is shown in Fig-4.

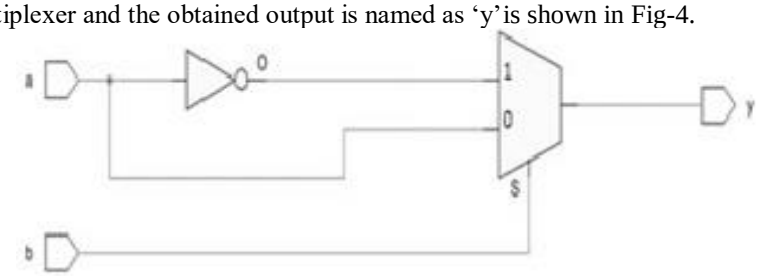

Fig-5: Modified XOR gate

The Modified XOR gate is designed by using a 2:1 multiplexer and a NOT gate for which the inputs to the multiplexer are 'a' and '~a'. Input 'b' acts as selection line for multiplexer and the obtained output is named as 'y' is shown in Fig-5.

c. Adder Block:

A Fast Add-one and Multiplexing Carry Select Adder (FAM CSLA) is being used here. The basic CSLA is not an area efficient area[4] is shown in Fig-6.

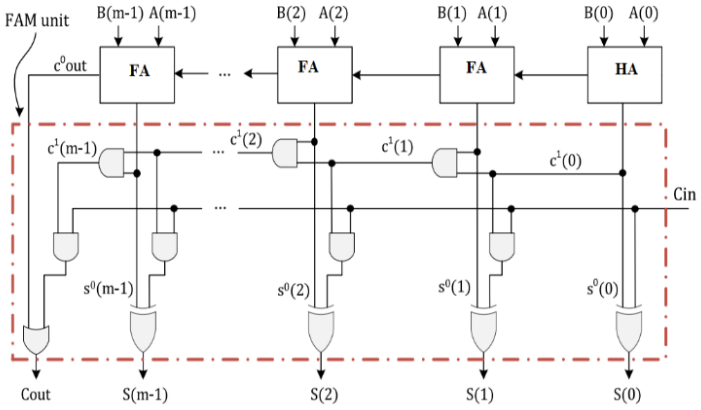

Fig-6: Fast Add-one and Multiplexing CSLA architecture

In this architecture, the full adder is replaced with two different full adder logics (i.e., full adder – 1 and full adder – 2)[5].

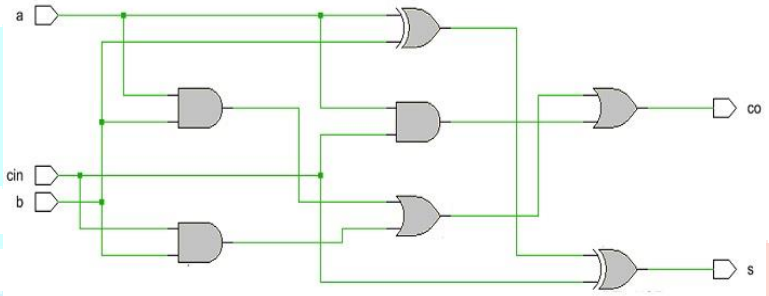

Fig-7: Full adder-1

The Fig-7 shows the architecture of the full adder which is coined as Full adder-1 used in the design of FAM CSLA, which the inputs are a,b and cin and the obtained outputs are s,cout.

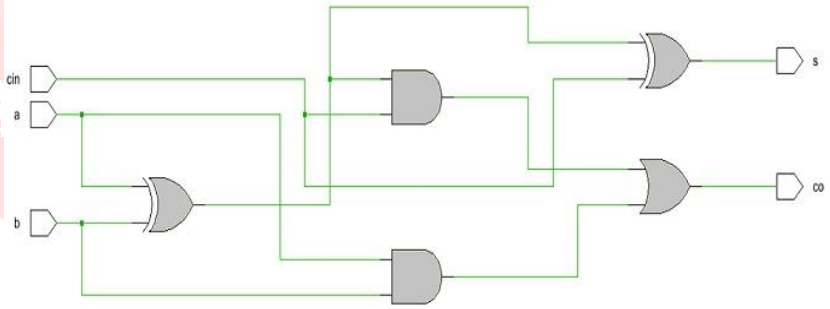

Fig-8: Full adder-2

The Fig-8 shows the architecture of the full adder which is coined as Full adder-2 used in the design of FAM CSLA, which the inputs are a,b and cin and the obtained outputs are s,cout.

The operation of FAM CSLA, is done using the add-one and MUX circuits. This combination leads to an efficient CSLA architecture in terms of speed.

The Vedic multiplier and FAM CSLA adder are used to increase the speed and to reduce power consumption of this filter.

III. SIMULATION RESULTS

The Xilinx Vivado 2017.2 software on an I5 processor with 8GB RAM and 64-bit operating system is used to Simulate and Synthesize the design of filter. A 4-Tap FIR Filter in various combinations are coded in Verilog HDL.

The inputs x[7:0] and the coefficients ho[7:0], h1[7:0], h2[7:0] and h3[7:0] are given to 4-tap FIR filter and the output is obtained as y[15:0] is shown in Fig-9.

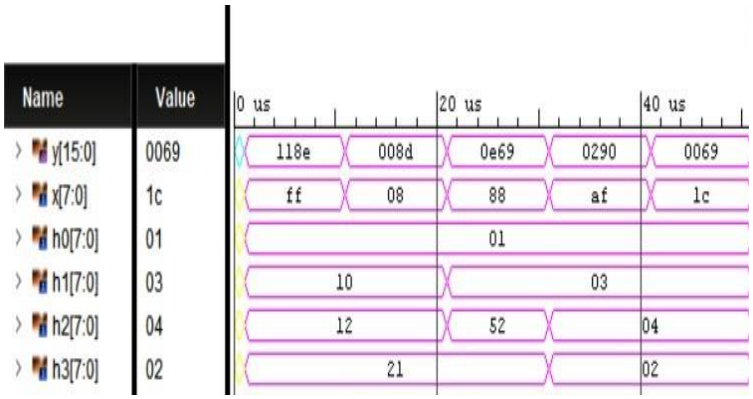

Fig-9:Simulation Results of 4-tap FIR Filter.

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IV. PERFORMANCE RESULTS

In this section performance analysis of FIR filter is reported by considering the performance metrics such as LUTs, power and delay.

The performance parameters for FIR Filter of modified full adder – 1 in FAM CSLA and using Vedic multiplier with modified logic gates is reported in Table-1.

Table-1: Parameters are reported for FIR Filter of Full adder – 1 in FAM CSLA and using Vedic multiplier with modified logic gates.

Gates	LUTs	DELAY (ns)		POWER (mw)
		Set Up	Hold	
And,Or, Ex-or	405	28.219	3.431	29.594
Modified And	402	28.358	3.379	29.538
Modified Or	412	26.595	3.248	28.538
Modified Exor	198	23.980	3.063	21.962
Modified And &Or	199	23.556	3.160	21.674
Modified And &Exor	198	23.980	3.063	21.962
Modified Or &Exor	198	23.980	3.063	21.962
Modified And, Or & Ex-or	198	23.980	3.063	21.962

The performance parameters for FIR Filter of modified full adder – 2 in FAM CSLA and using Vedic multiplier with modified logic gates is reported in Table-2.

Table-2:Parameters are reported for FIR Filter of Full adder – 2 in FAM CSLA and using Vedic multiplier with modified logic gates.

Gates	LUTs	DELAY (ns)		POWER (mw)
		Set Up	Hold	
And,Or, Ex-or	417	25.942	3.247	29.604
Modified And	430	27.620	3.318	30.218
Modified Or	417	27.078	3.134	28.594
Modified Exor	221	22.373	3.102	22.479
Modified And &Or	417	27.078	3.134	28.597
Modified And &Exor	221	22.373	3.102	22.479
Modified Or &Exor	221	22.373	3.102	22.479
Modified And, Or & Ex-or	221	22.373	3.102	22.479

V.COMPARISON RESULTS

The comparisons for for FIR Filter of modified full adder – 1 in FAM CSLA architecture and using Vedic multiplier with modified logic gates is shown in Fig-10.

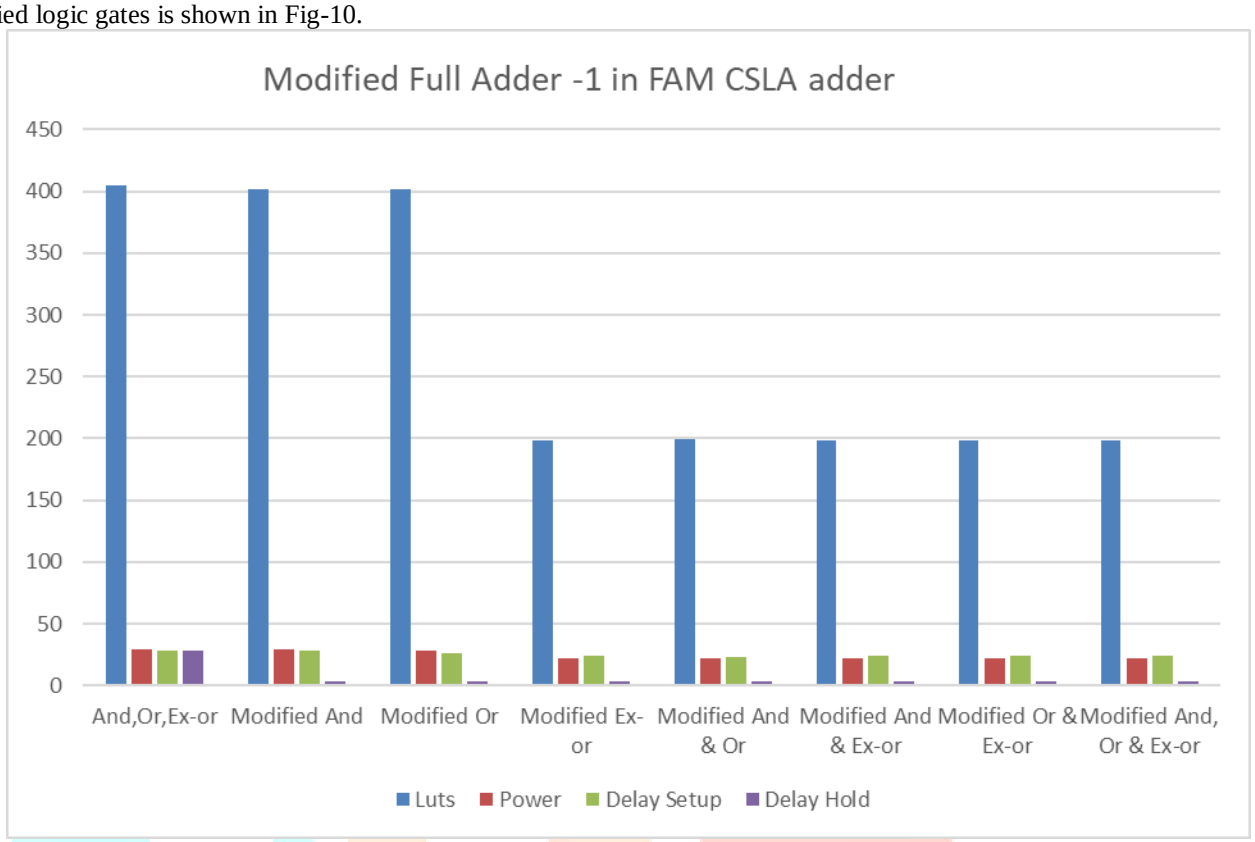

Fig-10: Comparison of performance parameters for FIR filter of modified full adder – 1 in FAM CSLA and using Vedic multiplier with different modified logic gates.

The comparisons for for FIR Filter of modified full adder – 2 in FAM CSLA and using Vedic multiplier with modified logic gates is shown in Fig-11.

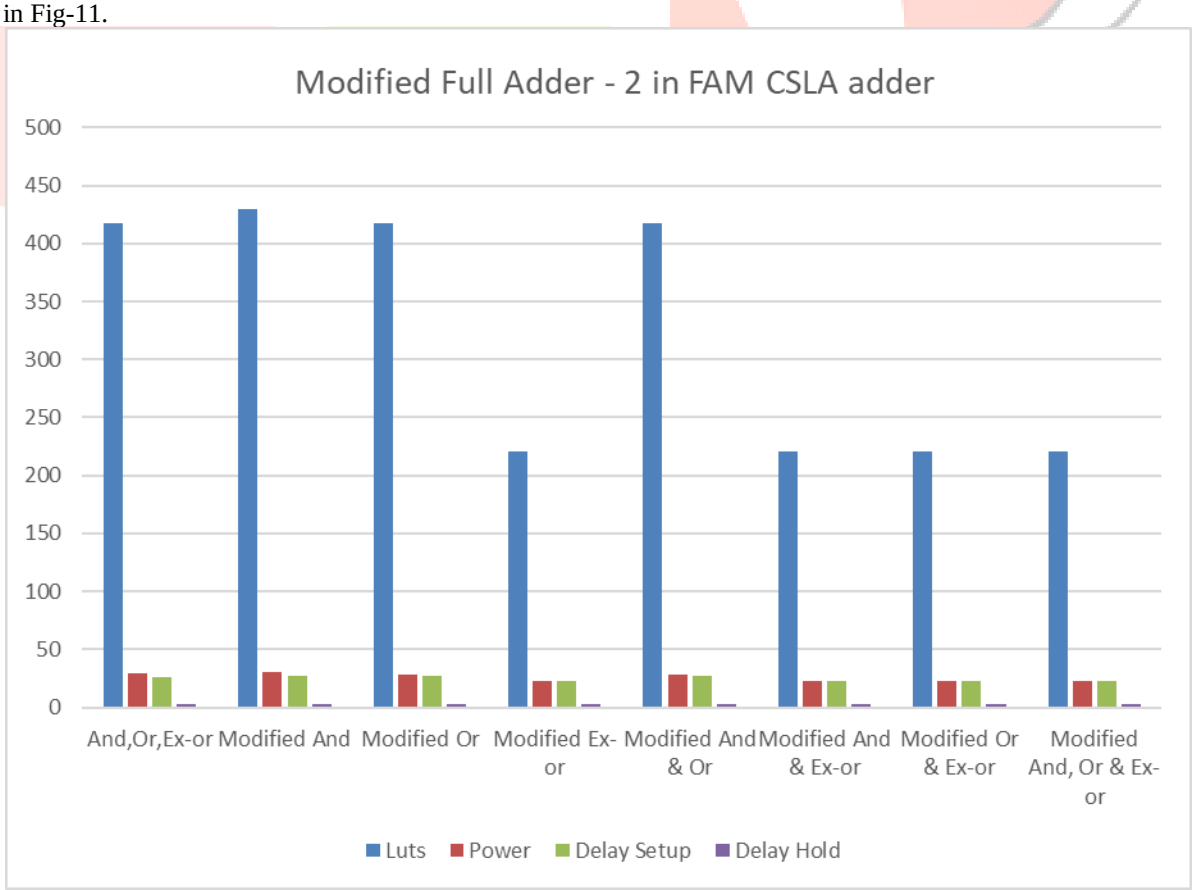

Fig-11: Comparison of performance parameters for FIR filter of modified full adder – 1 in FAM CSLA and using Vedic multiplier with different modified logic gates.

VI.CONCLUSION

In this text, the Verilog HDL language is used to design FIR filter modules and it's sub modules. The MATLAB software has been used for filter coefficients. As discussed, filter performance depends on multiplier and adder. Here the Vedic Multiplier is used to reduce area and power consumption. And the Fast Add-one and Multiplexing CSLA has less delay and more applications.by using these multiplier and adder an effective filter is designed. In short note, performance analysis for FIR filter is done by simulating and synthesizing in Xilinx Vivado 2017.2 software and the simulation results show that the FIR filter designed fully complies with design requirements. The performance of this filter are compared, from this result analysis, it has been concluded that VMMA design is carried out by using modified Exor gate, modified And & Exor gates, modified Or & Exor gate and modified And, Or & Exor gates alongside by changing full adder in a FAM CSLA adder architecture with modified full adder – 1 which reduces area and power. The designed filter will be helpful in real – time DSP applications. For future works, the proposed filter architecture can be implemented using different technology libraries to achieve the better enhancements under different conditions.

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